Interralated patents are pending

◆ FEATURES

- High accuracy, less than 0.1% error over a dynamic range of 3000:1
- High stability, less than 0.1% error in the output frequency fluctuation
- Measure the active power in the positive orientation and negative orientation, transform to fast pulse output(CF）
- Provide two current input for line and neutral current measurement
- Mesure instantaneous IRMS and VRMS over a dynamic range of 1500:1
- Provide SAG detection and Phase failure detection
- On-chip power supply detector
- On-chip anti-creep protection with the programmable threshold set
- Provide the pulse output with programmable frequency adjustment
- Provide the programmable gain adjustment and phase compensation
- Measure the power factor (PF）
- Provide a programmable interrupt request signal （/IRQ）
- Provide a SPI communication interface
- On-chip voltage reference of 2.5V
- Single 5V supply, 25mW（typical）

◆ DESCRIPTION

The BL6523B is a low cost, high accuracy, high stability, electrical energy measurement IC intended to single phase, multifucion applications.

The BL6523B incorporates three high accuracy Sigma-Delta ADC, voltage reference, power management and digital signal processing circuit using to calculates active energy, apparent energy, IRMS, VRMS etc.

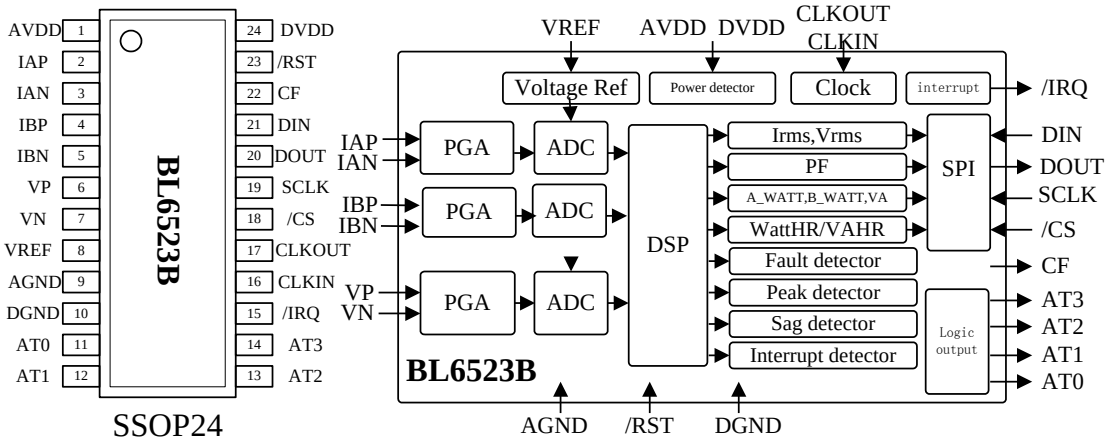
The BL6523B have two current input for line and neutral current measurement, when these currents differ by more than the programmable Fault threshold value(RMS or WATT), the BL6523B give the tamper indicator and can enable neutral current billing,

The BL6523B measures line voltage, current and calculates active, apparent energy, power factor, line frequency, detect sag, overvoltage, overcurrent, peak, reverse power, zero-crossing voltage.

The BL6523B provides access to on-chip meter registers via SPI communication interface.

The BL6523B provide all-digital domain offset compensation, gain adjustment, phase compensation (maximum ±2.54°adjustable）.

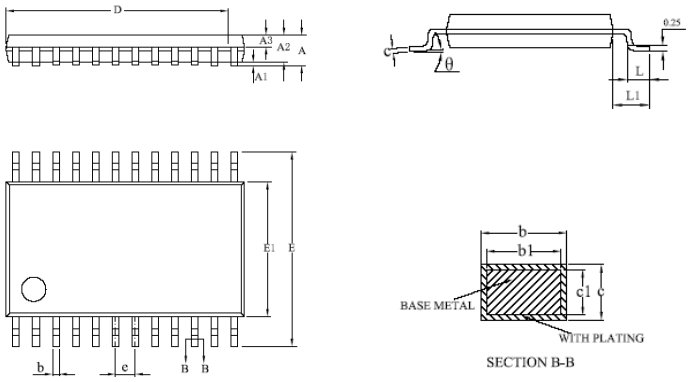
◆ BLOCK DIAGRAM



PIN DESCRIPTIONS（SSOP24）

Pin	Symbol	DESCRIPTIONS
1	AVDD	Power Supply (+5V). Provides the supply voltage for the circuitry. It should be maintained at 5 V±5% for specified operation.
2，3，4，5	IAP，IAN，IBP，IBN	Analog input for current channel, These inputs are fully differential voltage inputs with a maximum signal level of ±660 mV, Adjustable Gain.
6，7	VP，VN	Negative and Positive Inputs for Voltage Channel. These inputs provide a fully differential input pair. The maximum differential input voltage is ± 750 mV for specified operation.Adjustable Gain.
8	VREF	On-Chip Voltage Reference. The on-chip reference has a nominal value of 2.5V ± 8% and a typical temperature coefficient of 30ppm/℃. An external reference source may also be connected at this pin.
9	AGND	Ground Reference. Provides the ground reference for the circuitry.
10	DGND	Digital Ground
11，12，13，14	AT0，AT1，AT2，AT3	Programmable digital output. See AT_SEL register section. Default output:AT0=FAULT、AT1=REVP、AT2=ZX、AT3=nSAG。
15	/IRQ	Interrupt output.
16	CLKIN	Clock In. An external clock can be provided at this logic input, Alterrnatively, a crystal (3.58MHz) can be connected across this pin and pin17 to provide a clock source.
17	CLKOUT	Clock out. A crystal can be connected across this pin and Pin16 as described above to provide a clock source.
18	/CS	Chip select for SPI interface. This pin must be pulled low if using the SPIinterface.
19	SCLK	Serial clock input for the synchronous serial interface. All serial communication data are synchronized to the clock.
20	DOUT	Data output for SPI interface. Data is shifted out at this pin on the rising edge of SCLK. This output is normally in a high impedance state, unless it is driving data out to the serial data bus.
21	DIN	Data input for SPI interface. Data is shifted in at this pin on the rising edge of SCLK
22	CF	Calibration Frequency. The CF logic output gives instantaneous real power information. This output is intended to use for calibration purposes. The full-scale output frequency can be scaled by the value of WA_CFDIV register. When the power is low, the pulse width is equal to 90ms. When the power is high and the output period less than 180ms, the pulse width equals to half of the output period.
23	/RST	Reset Pin. Logic low on this pin will hold the ADCS and digital circuitry in a reset condition and clear internal registers.
24	DVDD	Digital Power Supply（+5V）,provides the supply voltage for the digital circuitry. It should be maintained at +4.75V~+5.25V for specified operation

◆ Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.85
A1	0.05	0.15	0.25
A2	1.55	1.75	1.95
A3	0.70	0.80	0.90
b	0.29	—	0.37
b1	0.28	0.30	0.33
c	0.15	—	0.20
c1	0.14	0.15	0.16
D	8.00	8.20	8.40
E	7.60	7.80	8.00
E1	5.10	5.30	5.50
e	0.65BSC		
L	0.75	0.90	1.05
L1	1.25BSC		
θ	0	—	8°

◆ ABSOLUTE MAXIMUM RATIONS

（T = 25 ℃）

Parameter	Symbol	Value	单位
Power Voltage AVDD、DVDD	AVDD、DVDD	-0.3 ~ +7	V
Analog Input Voltage to AGND	IAP、IBP、VP	-6 ~ +6	V
Digital Input Voltage to DGND	DIN、SCLK、/CS	-0.3 ~ VDD+0.3	V
Digital Output Voltage to DGND	CF、AT0、AT1、AT2、AT3 /IRQ、DOUT	-0.3 ~ VDD+0.3	V
Operating Temperature Range	Topr	-40 ~ +85	℃
Storage Temperature Range	Tstr	-55 ~ +150	℃
Power Dissipation（SSOP24）	P	80	mW

◆ Electronic Characteristic Patameter

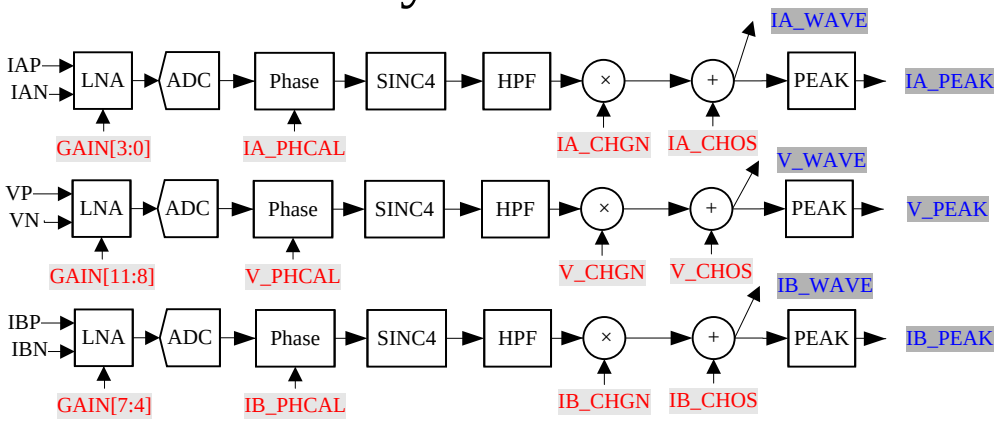
（AVDD = DVDD = 5V, AGND = DGND = 0V, CLKIN=3.58MHz, T=25℃）

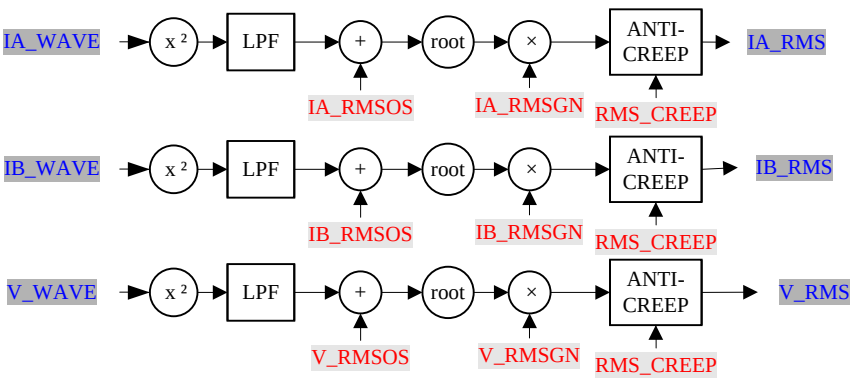
Parameter	Symbol	Test Condition	Measure Pin	Min Value	Typical Value	Max Value	Unit
Measure Error on Active Power	$WATT_{err}$	Over a dynamic range 3000:1	CF		0.1	0.3	%
Phase error when PF=0.8 Capacitive	PF08err	Current lead 37° （PF=0.8）				0.5	%
Phase error when PF=0.5Inductive	PF05err	Current lags 60° （PF=0.5）				0.5	%
AC PSRR	ACPSRR	IP/N=100mV			0.01		%

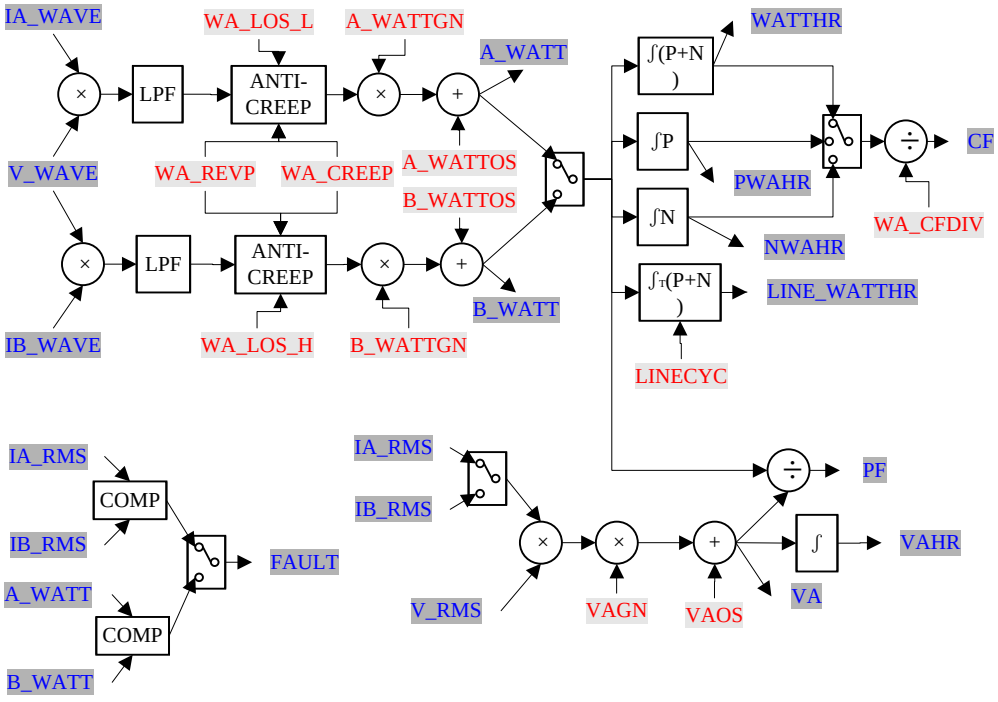
DC PSRR	DCPSRR	VP/N=100mV			0.1		%
Vrms measurement Error	VRMSerr	1500:1 input DR			0.3		%
Irms measurement Error	IRMSerr	1500:1 input DR			0.3		%
Maximum Input voltage						± 1200	mV
DC Input Voltage				370			kΩ
Input Signal Bandwidth		（-3dB）			14		kHz
Gain Error		External 2.5V reference		-4		+4	%
Gain Error match		External 2.5V reference		-1.5		+1.5	%
On-chip reference	Vref		VREF		2.5		V
Reference Error	Vreferr					± 200	mV
Temperature Coefficient	TempCoef				30		ppm/℃
Input High Voltage		DVDD=5V ± 5%		2.6			V
Input Low Voltage		DVDD=5V ± 5%				0.8	V
Output High Voltage		DVDD=5V ± 5%		4			V
Output Low Voltage		DVDD=5V ± 5%				1	V
Analog Power AVDD	VAVDD			4.75		5.25	V
Digital Power DVDD	VDVDD			4.75		5.25	V
AIDD	IAVDD	AVDD=5.25V			3		mA
DIDD	IDVDD	DVDD=5.25			2		mA

◆ THEORY OF OPERATION

BL6523B System Block







◆ Principle of Energy Measure

In energy measure, the power information varying with time is calculated by a direct multiplication of the voltage signal and the current signal. Assume that the current signal and the voltage signal are cosine functions, V,I are the peak values of the voltage signal and the current signal; the phase difference between the current signal and the voltage signal is expressed as Φ, Then the power is given as follows:

$$p(t) = V\cos(wt) \times I\cos(wt + \Phi)$$

If Φ=0 时:

$$p(t) = \frac{VI}{2}(1 + \cos(2wt))$$

If Φ≠0 时:

$$p(t) = V\cos(wt) \times I\cos(wt + \Phi)$$
$$= V\cos(wt) \times [I\cos(wt)\cos(\Phi) + \sin(wt)\sin(\Phi)]$$
$$= \frac{VI}{2}(1 + \cos(2wt))\cos(\Phi) + VI\cos(wt)\sin(wt)\sin(\Phi)$$
$$= \frac{VI}{2}(1 + \cos(2wt))\cos(\Phi) + \frac{VI}{2}\sin(2wt)\sin(\Phi)$$

p(t) is called as the instantaneous power signal. The ideal p(t) consists of the DC component and AC component whose frequency is 2ω. The DC component is called as the average active power.

The current signal and voltage signal is converted to digital signals by high-precsion ADCS, then through the drop sampling filter (SINC4), high-pass filter (HPF) filter out the high frequency noise and DC gain, get the required current and voltage sampling data.

Current sampling data multiplied by voltage sampling data gets instantaneous active power, then through the low pass filter (LPF), output average active power.

Current sampling data and voltage sampling data processed by square circuit, low-pass filter(LPF1), square root circuit, get the current RMS and voltage RMS.

Active power through a certain time integral, get active energy.

- **Front-end gain adjustment**

Every analog channel has a programmable gain amplifier (PGA), gain selection is achieved by the gain register (GAIN), the default value of the gain register (GAIN) is 000H.

Every 4-bit of the gain register used to select the current channel or voltage channel PGA. Gain[3:0] used to select Current A channel PGA,Gain[7:4] used to select Current B channel PGA, Gain[11:8] used to select Voltage channel PGA.

For example Gain [3:0]:

x000=1x
x001=2x
x010=4x
x011=8x
x100=16x
x101=24x
x110=32x
x111=32x

◆ **Phase compensation**

BL6523B provides the method of small phase error digital calibration. It will be a small time delay or advance into signal processing circuit in order to compensate for small phase error. Because this compensation should be promptly, so this method applies only to 0.1°~0.5° range of small phase error.

Phase calibration register(IA_PHCAL、IB_PHCAL、V_PHCAL) is a binary 8-bit register, corresponding to the compensation current A channel, current B channel and voltage channel phase. The default value is 00H. Bit[7] is enable bit, when Bit[7]＝0,disable compensation;Bit[7]＝1,enable compensation. Bit[6:0] used to adjust the delay time，1.1us/1LSB. With a line frequency of 50Hz, the resolution is 360°×（1/900KHz）×50Hz=0.02°, The adjustable range is 0°~2.54°.

◆ **Input channel offset calibration**

BL6523B contains the input channel offset calibration registers (IA_CHOS, IB_CHOS, V_CHOS), these registers are in 12-bit sign magnitude format, the default value is 000H. The offset may result from the analog input and the analog-digital conversion circuit itself.

◆ **Active power offset calibration**

BL6523B contains the active power offset calibration (A_WATTOS,B_WATTOS). Both registers are in 12-bit sign magnitude format, the default value is 000H. The offset can exist in the power calculations due to crosstalk between channels on the PCB and in the BL6523B. The active power offset calibration allows these offsets to be removed to increase the accuracy of the measurement at low input power levels.

$$ActivePower = ActivePower_0 + X\_\text{WATTOS}$$

◆ **Active power gain adjustment**

The gain registers (A_WATTGN, B_WATTGN) are used to adjust the active power measurement range. Both registers are in 12-bit sign magnitude format, the default value is 000H. The following formula shows how to adjust the output active power:

$$Output\ \ ActivePower = Active\ Power \times (1 + \frac{X\_WATTWG}{2^{12}})$$

The minimum value that can be write to the X_WATTGN register is 801H(HEX), which represents a gain adjustmen of -50%. The maximum value that can be write to the X_WATTGN register is 7FFH (HEX), which represents a gain adjustmen of +50%.

Similar gain calibration regisets are available for current channel A, current channel B and voltage channel (IA_CHGN, IB_CHGN, V_CHGN).

◆ **No-load threshold of active power**

BL6523B contains two no-load detection feature that eliminates meter creep. BL6523B can set the no-load threshold on the active power (WA_CREEP), this register is in 24-bit unsign magnitude format. The low 12-bit(WA_CREEP_L) is used to set the active power threshold value, When the absolute value of the input power signal is less than this threshold, the output active power is set to zero. This can make the active power register to 0 in no-load conditions, even a small noise signal input .

$$WATT = \begin{cases} 0 & , \ |WATT| < WA\_CREEP\_L \\ WATT, & |WATT| >= WA\_CREEP\_L \end{cases}$$

The high 12-bit of WA_CREEP register(WA_CREEP_H) is used to set the active power timer threshold value. The default value is 0xFFF. There have a internal TIME_CREEP register in BL6523B, when detect the CF pulse output , the TIME_CREEP register is set to the value of WA_CREEP_H. If not detected the CF pulse output, the TIME_CREEP register value decrease. If the TIME_CREEP register decrease to 0, there is still no CF signal output, the BL6523B produce a reset signal used to reset the internal energy accumulated register of CF pulse and reload the value of WA_CREEP_H to the TOME_CREEP register. The resolution of the WA_CREEP_H is 4.6s / LSB, so the maxium timing anti-creep time is about 5h13m.

MODE[6]=1 enable timing anti-creep function.

MODE[6]=0 disable timing anti-creep function.

- **Active power compensation of small signal**

BL6523B contains a small active power signal compensation register (WA_LOS), this register is in 12-bit sign magnitude format. The default value is 000H。

- **Reverse indicator threshold**

BL6523B contains a reverse indicator threshold register(WA_REVP), this register is in 12-bit unsigned magnitude format, When the input power signal is negative and the absolute value is greater than the power threshold， the BL6523B output the REVP indicator.

- **Active energy calculation**

The relationship between power and energy can be expressed as：

$$Power = \frac{dEnergy}{dt}$$

Conversely, energy is given as the integral of power.

$$Energy = \int Power \ dt$$

In BL6523B, the active power signals are accumulated in a 53 internal registers continuously to get active energy, Active energy register WATTHR [23:0] take out this internal register[52:29] as active energy output. This discrete time accumulation is equivalent to integration in continuous time.

$$E = \int p(t)dt = Lim_{T \to 0} \{ \sum_{n=0}^{\infty} P(nT) \times T \}$$

Where:

n is the discrete time-sample number; T is the sampling period; the sampling period of BL6523B is 1.1us.

The BL6523B include a interrupt (APEHF) that is triggered When the active energy register(WATTHR) is half full. If the enable APEHF bit in the interrupt mask register set to logic high, the / IRQ output Pin goes logic low.

The BL6523B include line cycle energy register(LINE_WATTHR). The number of cycles is

writen to the LINECYC register, the LSB of the LINECYC register is 0.1S. At the end of a line cycle accumulation cycle, the LINE_WATTHR regiseter is updated. The LINE_WATTHR register hold its current value until the end of the next line cycle period, when the content is replaced with the new reading. If a new value is written to the LINECYC register midway through a line cycle accumulation, the new value is not internally loaded until the end of a line cycle period.

- **Frequency output**

The BL6523B provides a energy-to-frequency conversion for calibration purpose. After initial calibration at manufacturing, the manufacturer or end customer is often required to verify the meter accuracy. One convenient way to do this is to provide an output frequency that is proportional to the active power. This output frequency provides a simple sigle-wire interface that can be optically isolated to interface to external calibration equipment.

BL6523B includes a programmable calibration frequency output PIN (CF). The digital-to-frequency converter is used to generate the pulse output. The pulse output (CF) stay high for 90ms if the pulse period is longer than 180ms. If the pulse period is shorter than 180ms, the duty cycle of de pulse output is 50%. The maximum output frequency with ac inputs at full scale and with WA_CFDIV=100H is approximately 0.5 kHz.

The BL6523B can set the CF frequency through the WA_CF_DIV register . The default value of the WA_CFDIV register is 001H (HEX). When set WA_CFDIV[x]=1, the CF frequency is $2^{(x-4)}*CF_{WA\_CFDIV=010H}$.

- **Root mean square measurement**

The rms is expressed mathematically as:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2(t)dt}$$

For time-sampled signals:

$$V_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} V^2(i)}$$

- **rms offset calibration**

BL6523B contains the rms offset calibration (IA_RMSOS, IB_RMSOS, V_RMSOS). These registers are in 12-bit sign magnitude format, the default value is 000H. The offset can exist in the rms calculations due to input noise that is intergrated in the dc component of square calculation. The rms offset calibration allows these offsets to be removed to increase the accuracy of the measurement at low input power levels.

$$I_{ARMS} = \sqrt{I_{ARMS0}^{\ 2} + IX\_RMSOS \times 2^{17}}$$

- **rms gain calibration**

The gain registers (IA_RMSGN, IB_RMSGN, V_RMSGN) are used to adjust the rms measurement range. Both registers are in 12-bit sign magnitude format, the default value is 000H. The following formula shows how to adjust the rms:

$$Output\ \ rms = rms \times (1 + \frac{X\_RMSGN}{2^{12}})$$

The minimum value that can be write to the X_RMSGN register is 801H(HEX), which represents a gain adjustment of -50%. The maximum value that can be write to the X_RMSGN register is 7FFH (HEX), which represents a gain adjustment of +50%.

- **No-load threshold of RMS**

BL6523B can set the no-load threshold on the RMS_CREEP register, this register is in 12-bit unsigned magnitude format. When the value of the RMS register is less than this threshold, the RMS register is set to zero. This can make the RMS register to 0 in no-load conditions, even a small noise signal input .

$$\mathrm{RMS}=\begin{cases} 0 & |RMS|<RMS\_CREEP\times 2\ \times 1.3655 \\ \mathrm{RMS}, & |RMS|>=RMS\_CREEP\times 2\ \times 1.3655 \end{cases}$$

- **Apparent Power and Apparent Energy Calculation**

In BL6523B, the apparent power is defined as the product of V_RMS and IX_RMS.

VA＝IX_RMS×V_RMS

The apparent energy is given as the intergral of the apparent power. The apparent power signals are accumulated in an internal 49-bit register, apparent energy register VAHR [23:0] take out this internal register [48:25] as apparent energy output. The BL6523B include a interrupt (VAPEHF) that is triggered When the apparent energy register(VAHR) is half full. If the enable VAPEHF bit in the interrupt mask register set to logic high, the / IRQ output Pin goes logic low.

- **Power Factor**

PF＝ (WATT/VA)

PF register is in 24-bit sign magnitude format. Power factor =(sign bit)*((PF[22]×2^－1）＋（PF[21]×2^－2）＋。。。), the register value of 0x7FFFFF(HEX) corresponds to a power factor value of 1, the register value of 0x800000(HEX) corresponds to a power factor of -1, the register value of 0x400000(HEX) corresponds to a power factor of 0.5.

◆ Operation Mode Select

- **Metering channel selection**

The default metering channel of BL6523B is channel A. the MODE[0] of MODE register is used to select the metering channel.

MODE[0]=0, the metering channel is channel A;

MODE[0]=1, the metering channel is channel B;

MODE[1]=0; disable auto channel select;

MODE[1]=1; enable auto channel select; when the chip detect the imbalance of two current channel, the chip select the bigger current channel as the metering channel.

- **High-pass filter selection**

In the analog-digital conversion circuit, the current and voltage channels have high-pass filters to eliminate the DC offset. The MODE[4:2] of MODE register is used to select high-pass filter.

MODE[2]=0, enable the high-pass filter of current channel A;

MODE[2]=1,disable the high-pass filter of current channel A;

MODE[3]=0, enable the high-pass filter of current channel B;
MODE[3]=1,disable the high-pass filter of current channel B;
MODE[4]=0, enable the high-pass filter of voltage channel;
MODE[4]=1,disable the high-pass filter of voltage channel;

- **MODE[7]=1**

When BL6523B measure AC signal, MODE[7] must be set to 1.

- **Energy accumulation mode selection**

The MODE[9:8] of the MODE regiset is used to select energy accumulation mode.
MODE[9:8]=00, absolute energy accumulation;
MODE[9:8]=01, positive-only energy accumulation;
MODE[9:8]=10, arithmetical energy accumulation;
MODE[9:8]=11, negative-only energy accumulation;;

- **The current imbalance judgment**

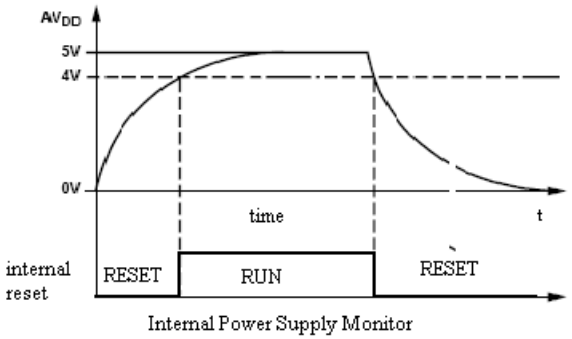
The BL6523B contains the detection of current imbalance. MODE[11:10] of the MODE register is used to set the current rms imbalance threshold. When the Line current rms and neutral current rms difference exceeds the threshold, the BL6523B give the FAULT indicator.

MODE[11]	MODE[10]	Threshold
0	0	12.5%(default)
0	1	6.25%
1	0	3.125%
1	1	10.1%

◆ Electric parameters monitor

- **Power Supply Monitor**

The BL6523B contains an on-chip power supply monitor. The analog supply (AVDD) is continuously monitored by the BL6523B. if the supply is less than 4V±5%, the BL6523B will be reset. This is useful to ensure correct device startup at power-up and power-down. The power supply monitor has built in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies. The power supply and decoupling for the part should be such that the ripple at AVDD does not exceed 5V±5% as specified for normal operation.



Internal Power Supply Monitor

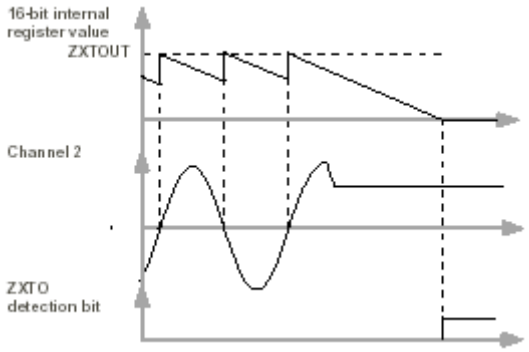
- **Zero-Crossing Detection**

The BL6523B includes a zero-crossing detection on voltage channel. The ZX output pin

goeshigh on positive-going edge of the voltage channel zero crossing.

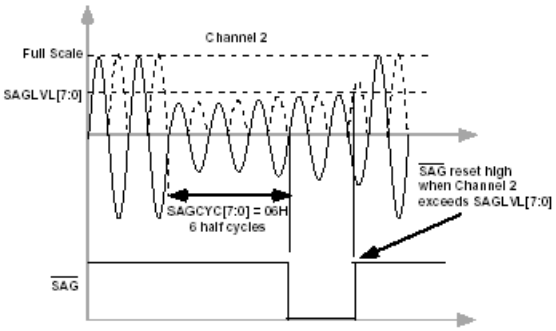
◆ **Zero-Crossing Timeout**

The BL6523B includes a zero-crossing timeout feature that is designed to detect when no zero crossings are obtained over a programmable time period. The duration of the zero-crossing timeout is programmed in the 16-bit ZXTOUT register. The value in the ZXTOUT register is decremented by 1LSB every 70.5us. if a zero-crossing is obtained, the ZXTOUT register is reloaded. If the ZXTOUT register reaches 0, a zero-crossing timeout event is issued. The maximum programmable timeout period is 4.369 secs. A interrupt is associated with the zero-crossing timeout feature. If enabled, a zero-crossing timeout event causes the external IRQ pin to go low.



◆ **Voltage Sag Detection**

The BL6523B includes a sag detection features that warns the user when the absolute value of the line voltage falls below the programmable threshold for a programmable number of half line cycles. The voltage sag feature is controlled by two registers: SAGLVL and SAGCYC. These registers control the sag voltage threshold and the sag period, respectively.



The 12-bit SAGLVL register contains the amplitude that the voltage channel must fall below before sag event occurs.The sag threshold is the number of half line cycles below which the voltage channel must remain before a sag condition occurs. Each LSB of the SAGCYC register corresponds to one half line cycle period. The default value is 0xFF(HEX). At 50Hz, the maximum sag cycle time is 2.55 seconds.

◆ **Peak Detection**

The BL6523B continuously records the maximum value of the current and voltage channels. The three registers that record the peak values on current channel A, current channel B, and the

voltage channel, respectively, are IAPEAK, IBPEAK, VPEAK.

◆ **Peak monitor**

The BL6523B include an overcurrent and overvoltage feature that detects whether the absolute value of the current or voltage waveform exceeds a programmable threshold. Three peak threshold register (IA_PKLVL, IB_PKLVL, V_PKLVL) are used to set the current or voltage channel peak threshold, respectively.

If the BL6523B detects an overvoltage condition, the PKV bit of the interrupt status register is set to 1. If the PKV bit of the interrupt mask register is enable, the IRQ output go low. The overcurrent detection feature works in the similar manner.

Interrupt

The BL6523B uses interrupt status register and interrupt mask register to manage interrupts. When an interrupt event occurs, the corresponding bit in the STATUS register is set to 1. If the enable bit for this interrupt, located in the MAK register is set to 0, the external IRQ pin is pulled to logic 0. The status bit located in the STATUS register is set when an interrupt event occurs, regardless of whether the external interrupt is enabled.

All interrupts are latched and require servicing to clear. To service the interrupt and return the IRQ pin to logic 1, the status bits must be cleared using the STATUS register. After completion of a read from the STATUS register, the IRQ pin returns to logic 1.the status bit can't be cleared after a read operation of STAUTS register, but can be writen 0 to the corresponding bit in the status register through the SPI interface clearing the status bit.

◆ SPI interface

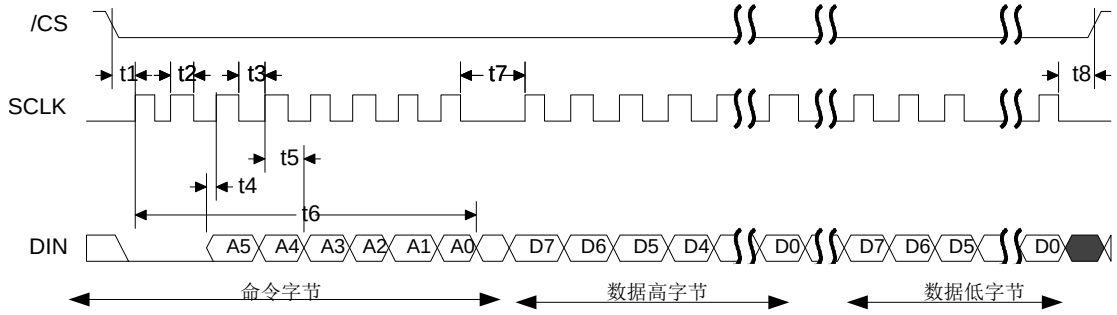
The SPI communication packet consists of an initial byte, The Bit [7:6] of this byte dictates whether a read or a write is being issued. The Bit [7:6] of this byte should be set to 00 for a read operation and to 01 for a write operation. The Bit [5:0] of this byte is the address of the register that is to be read from or written to. This byte should be transmitted MSB first. When this initial byte transmission is complete, the register data is either sent from the BL6523B on the DOUT pin (in the case of a read) or is written to the BL6523B DIN Pin by the external microcontroller (in the case of a write). All data is sent or received MSB first. The lenth of the data transfer is 24 bits long.

The serial peripheral interface of BL6523B uses four communication pins: SCLK, DIN, DOUT and /CS. The SPI communication operates in slave mode, a clock must be provided on the SCLK pin. This clock synchronizs all communication. The DIN pin is an input to the BL6523B; data is sampled by BL6523B on the rising edge of SCLK. The DOUT pin is an output from the BL6523B; data is shifted out on the rising edge of SCLK. The /CS (chip select) input must be driven low to initialize the communication and driven high at the end of the communication. Driving the /CS input high before the completion of a data transfer ends the communication.

◆ **SPI Write operation**

Serial write sequence is shown in the figure. The Bit[7:6] of the first bytes in DIN is 01, indicate a write operation. The Bit[5:0] of this byte indicate the address of register. The last three bytes is the data that will be writed to the register. The data written to the BL6523B should be

ready before the rising edge of SLCK. The SPI interface will shift the data in the BL6523B on the rising edge of SCLK.

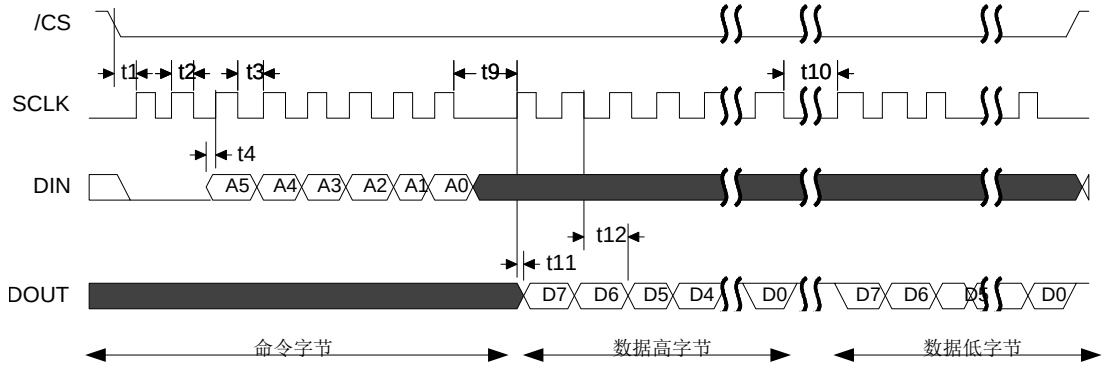


（DVDD＝5V± 5%，DGND＝0V，CLKIN＝3.58MHz XTAL，25℃）

		min	type	max	unit
t1	/CS to the rising edge of SCLK	5000			ns
t2	The high pulse width of SCLK	5000			ns
t3	The low pulse width of SCLK	5000			ns
t4	Data setup time before the rising edge of SCLK	3000			ns
t5	Data hold time after the rising edge of SCLK	2000			ns
t6	Transmission time between two bytes	80			us
t7	The minimum time interval between two bytes of data	5000			ns
t8	The minimu hold time of /CS after the falling edge of SCLK	5000			ns

◆ **SPI read operation**

Serial read sequence is shown in the figure. The Bit[7:6] of the first bytes in DIN is 00, indicate a read operation. The Bit[5:0] of this byte indicate the address of register. The data written to the BL6523B should be ready on DIN before the rising edge of SLCK. After the BL6523B receive the address of register, the BL6523B will shift out the data of the register on DOUT pin on the rising edge of SCLK.



（DVDD＝5V± 5%，DGND＝0V，CLKIN＝3.58MHz XTAL，25℃）

		min	type	max	unit
t9	The shortest interval from the End of the read command to the start of read data read	5000			ns
t10	The shortest interval between two bytes of data	5000			ns
t11	Data setup time after the rising edge of SCLK			10000	ns
t12	Data hold time after the falling edge of SCLK	5000			ns

◆ Register

◆ Register list

ADDRESS	REGISTER NAME	EXTERNAL R/W	INTERNAL R/W	BIT	DEFAULT	DESCRIPTION
ELECTRIC PARAMETERS REGISTER（INTERNAL WRITE）						
01H	IA_WAVE	R	W	24	0	Wave register of channel A
02H	IB_WAVE	R	W	24	0	Wave register of channel B
03H	V_WAVE	R	W	24	0	Wave register of Voltage
04H	LINE_ WATTHR	R	W	24	0	Line cycle energy register
05H	IA_RMS	R	W	24	0	Irms register(channel A)
06H	IB_RMS	R	W	24	0	Irms register(channel B)
07H	V_RMS	R	W	24	0	Vrms
08H	PF	R	W	24	0	Power Factor
09H	FREQ	R	W	24	0	Frequency register
0AH	A_WATT	R	W	24	0	Average active power of channel A
0BH	VA	R	W	24	0	Average apparent power
0CH	WATTHR	R	W	24	0	Active energy
0DH	VAHR	R	W	24	0	Apparent energy
0EH	PWAHR	R	W	24	0	Positive active energy
0FH	NWAHR	R	W	24	0	Negative active energy
10H	IA_PEAK	R	W	24	0	Current A Peak register
11H	IB_PEAK	R	W	24	0	Current B Peak register
12H	V_PEAK	R	W	24	0	Voltage Peak register
13H	B_WATT	R	W	24	0	Average active power of channel B
Calibration registers (External write，Except 3AH）						
14H	MODE	R/W	R	12	000H	Mode regiser,
15H	GAIN	R/W	R	12	000H	Channel Gain register
16H	FAULTLVL	R/W	R	12	044H	Current imbalance shielding threshold register
17H	WA_CREEP	R/W	R	24	FFF02BH	Active power no-load threshold register
18H	WA_REVP	R/W	R	12	087H	Reverse threshold register
19H	WA_CFDIV	R/W	R	12	001H	Active power CF frequency divider
1AH	A_WATTOS	R/W	R	12	0	Active power offset correction(current channel A)
1BH	B_WATTOS	R/W	R	12	0	Active power offset correction(current B)
1CH	A_WATTGN	R/W	R	12	0	Active power gain(current channel A)

1DH	B_WATTGN	R/W	R	12	0	Active power gain(current channel B)
1EH	IA_PHCAL	R/W	R	8	0	Phase calibration register(current channel A)(bit[7]is enable bit,2.2us/1LSB）
1FH	IB_PHCAL	R/W	R	8	0	Phase calibration register(current channel B)
20H	V_PHCAL	R/W	R	8	0	Phase calibration register(voltage channel)
21H	VAOS	R/W	R	12	0	Apparent Power Offset Calibration Register
22H	VAGN	R/W	R	12	0	Apparent power gain adjust register
23H	IA_RMSGN	R/W	R	12	0	Current A RMS gain adjust register
24H	IB_RMSGN	R/W	R	12	0	Current B RMS gain adjust register
25H	V_RMSGN	R/W	R	12	0	Voltage RMS gain adjust register
26H	IA_RMSOS	R/W	R	12	0	Current A RMS Offset Calibration register
27H	IB_RMSOS	R/W	R	12	0	Current B RMS Offset Calibration register
28H	V_RMSOS	R/W	R	12	0	Voltage RMS Offset Calibration register
29H	RMS_CREEP	R/W	R	12	0	RMS small signal threshold register
2AH	WA_LOS	R/W	R	24	0	Active-power offset Calibration register Bit[23:12] B channel; Bit[11:0] A channel;
2BH	IA_CHOS	R/W	R	12	0	Current A channel offset adjustment register，
2CH	IB_CHOS	R/W	R	12	0	Current B channel offset adjustment register
2DH	V_CHOS	R/W	R	12	0	Voltage channel offset adjustment register
2EH	IA_CHGN	R/W	R	12	0	Current A channel gain adjustment register
2FH	IB_CHGN	R/W	R	12	0	Current B channel gain adjustment register
30H	V_CHGN	R/W	R	12	0	Voltage channel gain adjustment register
31H	LINECYC	R/W	R	12	000H	Line energy accumulation cycles register
32H	ZXTOUT	R/W	R	16	FFFFH	Zero-crossing timeout
33H	SAGCYC	R/W	R	8	FFH	Sag period
34H	SAGLVL	R/W	R	12	0	Sag voltage level
35H	IA_PKLVL	R/W	R	12	FFFH	Current peak threshold (current channel A)

36H	IB_PKLVL	R/W	R	12	FFFH	Current peak threshold (current channel B)
37H	V_PKLVL	R/W	R	12	FFFH	Voltage peak threshold
38H	AT_SEL	R/W	R	16	0	Logic output selection
39H	MASK	R/W	R	12	0	Interrupt mask register,
3AH	STATUS	R	W	12	0	Interrupt state register
Special register						
3BH	READ	R	R	24	0	Contains the data from the last read operation of SPI
3CH	WRITE	R	R	24	0	Contains the data from the last write operation of SPI
3DH	CHKSUM	R	R	24	0x0121 F2H	Checksum。The sum of register 14H~39H
3EH	WRPROT	R/W	R	8	0	Write protection register. Write 55H, it means that allows write to writable register。

Electric Parameters Registers

Waveform Register (IA_WAVE,IB_WAVE,V_WAVE)

Waveform Register of Current(IA_WAVE) Addr：01H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
Sign bit	I_WAVE22	I_WAVE21	I_WAVE20…3	I_WAVE2	I_WAVE1	I_WAVE0

Waveform Register of Current(IB_WAVE) Addr：02H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
Sign bit	I_WAVE22	I_WAVE21	I_WAVE20…3	I_WAVE2	I_WAVE1	I_WAVE0

Waveform Register of voltage(V_WAVE) Addr：03H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
Sign bit	V_WAVE22	V_WAVE21	V_WAVE20…3	V_WAVE2	V_WAVE1	V_WAVE0

Note: These registers have 24-bit complement registers, bit 23 is sign bit. The update speed of waveform register is 14 KHz.

Line Cycle Energy Register (LINE_WATTHR)

Line Cycle Active Energy Register of (LINE_WATTHR) Addr：04H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
L_AHR23	L_AHR22	L_AHR21	L_AHR20…3	L_AHR2	L_AHR1	L_AHR0

Note: This registers accumulate energy over (LINECYC+1)*0.1 second. The update speed of these registers is (LINECYC+1)*0.1 second. By using the line cycle energy accumulation mode, the energy calibration can be greatly simplified, and the time required to calibrate the meter can be significantly reduced. The accumulation time is specified in the LINECYC register.

RMS Register (IA_RMS, IB_RMS and V_RMS)

Irms register of Current(IA_RMS) Addr：05H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
RMS23	RMS22	RMS21	RMS20…3	RMS2	RMS1	RMS0

Irms register of Current(IB_RMS) Addr：06H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
RMS23	RMS22	RMS21	RMS20…3	RMS2	RMS1	RMS0

Vrms register (V_RMS) Addr：07H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
RMS23	RMS22	RMS21	RMS20…3	RMS2	RMS1	RMS0

Note: RMS value is 24-bit unsigned data. The registers updating frequency is 10Hz.

Power Factor Register (PF)

Power Factor Register(PF) Addr：08H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PF23	PF22	PF21	PF20…3	PF2	PF1	PF0

Note: PF23 is the sign bit. 24 bit complement register.

If PF23=0 then $PF = PF\_Reg/2^{23}$

If PF23=1 then $PF = (PF\_Reg - 2^{24})/2^{23}$

Frequency Register (FREQ)

Frequency Register(FREQ) Addr：09H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
FREQ23	FREQ22	FREQ21	FREQ20…3	FREQ2	FREQ1	FREQ0

Note: this register is the period value of the line in voltage channel.

If an 3.579545MHz crystal is used, the voltage frequency=$\frac{87.3906\times3579545}{FREQ\_Reg}$

Active Power Register (A_WATT and B_WATT)

Average active power (A_WATT) Addr：0AH			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
Sign bit	WATT22	WATT21	WATT20…3	WATT2	WATT1	WATT0

Average active power (B_WATT) Addr：	Type: Read	Default: 000000H

13H						
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
Sign bit	WATT22	WATT21	WATT20…3	WATT2	WATT1	WATT0

Note: these registers are set as binary complement. The MSB is sign bit. Register updated frequency is 2.5Hz.

Assume the data in register is WATT0, then the AP for calculation is:

If WATT0<2^23, AP=WATT0;

If WATT0>=2^23, AP=WATT0-2^24;

Assume the displayed active power is P, and conversion coefficiency is Kp, then

P=AP/Kp;

Where Kp is calculated at PF=1.0, Un, Ib.

Apparent Power Register (VA)

Average apparent power register(VA) Addr：0BH			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
VA23	VA22	VA21	VA20…3	VA2	VA1	VA0

Note: The coefficient of apparent power is equal to active power coefficient.

Energy Registers（WATTHR,PWAHR,NWAHR,VAHR）

Active Energy Register(WATTHR) Addr：0CH			Type: Read		Default：000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
WTTHR23	WATTHR22	WATTHR21	WATTHR20…3	WATTHR2	WATTHR1	WATTHR0

Apparent Energy Register(VAHR) Addr：0DH			Type: Read		Default：000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
VAHR23	VAHR 22	VAHR21	VAHR20…3	VAHR2	VAHR1	VAHR0

Positive Active Energy Register(PWAHR) Addr：0EH			Type: Read		Default：000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PWAHR23	PWAHR22	PWAHR21	PWAHR20…3	PWAHR2	PWAHR1	PWAHR0

Negative Active Energy Register(NWAHR) Addr：0FH			Type: Read		Default：000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
NWAHR23	NWAHR22	NWAHR21	NWAHR20…3	NWAHR2	NWAHR1	NWAHR0

Note: these registers cannot be clear after read.

Peak Register (IA_PEAK, IB_PEAK and V_PEAK)

Current A peak register(IA_PEAK) Addr：10H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PEAK23	PEAK22	PEAK21	PEAK20…3	PEAK2	PEAK1	PEAK0

Current A peak register(IB_PEAK) Addr：11H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PEAK23	PEAK22	PEAK21	PEAK20…3	PEAK2	PEAK1	PEAK0

Voltage peak register(V_PEAK) Addr：12H			Type: Read		Default: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PEAK23	PEAK22	PEAK21	PEAK20…3	PEAK2	PEAK1	PEAK0

Note: the register updating frequency is 50Hz.

Calibration Registers

MODE Register (MODE)

MODE Register(MODE) Addr：14H				Type：R/W		Default： 000H	
				Bit11	Bit10	Bit9	Bit8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Bit location	Bit mnemonic	Default value	Description
0	WATT_SEL	0	The channel selection of Energy accumulation and CF output. MODE [0] =0, Current A channel. MODE [0] =1, Current B channel.
1	AUTO_SEL	0	Enable/disable Anti-tampering Mode MODE [1] =0, disable auto-switch channel. MODE [1] =1, enable auto-switch channel. When the Line and Neutral Current differ by more than the Fault_SEL threshold, the IC will auto-switch to the channel of the larger power.
2	A_HPF_SEL	0	Enable/disable the high-pass filter of current channel A MODE [2] =0, When measure AC signal input. MODE [2] =1, When measure DC signal input.
3	B_HPF_SEL	0	Enable/disable the high-pass filter of current channel B
4	V_HPF_SEL	0	Enable/disable the high-pass filter of voltage channel.
5	COMP_SEL	0	Anti-tampering MODE =0, anti-tampering mode of RMS, =1, anti-tampering mode of active power.
6	ANTICREEP	0	Anti-Creep Mode

	_SEL		=0, anti-creep mode of active power threshold, =1, anti-creep mode of active power threshold and time-creep.
7			**This bit must be set to 1**
8,9	CF_ADD_SEL	00	CF output mode for active power MODE[9:8]=00, absolute energy pulse output; MODE[9:8]=01, positive-only energy pulse output; MODE[9:8]=10, arithmetical energy pulse output; MODE[9:8]=11, negative-only energy pulse output;
10, 11	FAULT_SEL	00	These bits configure the L and N Line power difference threshold in anti-tampering mode

Mode[11]	Mode[10]	Threshold
0	0	12.5%
0	1	6.25%
1	0	3.125%
1	1	10.16%

Channel Gain Register (GAIN)

Channel Gain Register(Gain) Addr：15H		Type：R/W	Default：000H
Bit[11]~Bit[8]	Bit[7]~Bit[4]	Bit[3]~Bit[0]	
Voltage channel PGA Gain	Current channel B PGA Gain	Current channel B PGA Gain	

Bit	Description
11~8	Voltage PGA Gain, default value is ‘0’

Bit[11]	Bit[10]	Bit[9]	Bit[8]	PGA Gain
×	0	0	0	1
×	0	0	1	2
×	0	1	0	4
×	0	1	1	8
×	1	0	0	16
×	1	0	1	24
×	1	1	0	32

7~4	Current channel B PGA Gain, default value is ‘0’

Bit[7]	Bit[6]	Bit[5]	Bit[4]	PGA Gain
×	0	0	0	1
×	0	0	1	2
×	0	1	0	4
×	0	1	1	8
×	1	0	0	16
×	1	0	1	24
×	1	1	0	32

3~0	Current channel A PGA Gain, default value is ‘0’

Bit[3]	Bit[2]	Bit[1]	Bit[0]	PGA Gain
×	0	0	0	1
×	0	0	1	2
×	0	1	0	4
×	0	1	1	8
×	1	0	0	16
×	1	0	1	24
×	1	1	0	32

Imbalance Threshold Register (FAULTLVL)

Active Power Noload threshold(FAULTLVL) Addr：16H			Type：R/W		Default：044H	
Bit11	Bit10	Bit9	…	Bit2	Bit1	Bit0

When the value of the RMS/WATT is less than this threshold, the fault detection can't work.
FAULTLVL=RMS_reg/256 or FAULTLVL=WATT_reg/256.

Noload Threshold Register (WA_CREEP)

Active Power Noload threshold(WA_CREEP) Addr：17H			Type：R/W		Default：FFF02BH	
Bit23	Bit22	Bit21	…	Bit14	Bit13	Bit12
Bit11	Bit10	Bit9	…	Bit2	Bit1	Bit0

Bit[23:12] is used to set time-creep threshold. 1LSB=4.6 second.
Bit[11:0] is used to set active power noload threshold. When the absolute value of the input power signal is less than this threshold, the output active power is set to zero. This can make in no-load conditions, even a small noise signal output to the active register is 0.
One LSB in the WA_CREEP [11:0] register is equivalent to 0.366 LSBs in the WATT register.
Example: the value of WATT register is 249F0H (150000) (100%Un, 100%Ib), the starting current of the meter is 0.4%Ib. the No-Load threshold value of active power can be set to 0.2%Ib*Un. (150000*0.2%=300), the value of WA_CREEP[11:0] is 300*0.366≈110(6EH)

Reverse Noload Threshold Register (WA_REVP)

Reverse Noload threshold(WA_REVP) Addr：18H			Type：R/W		Default：087H	
Bit11	Bit10	Bit9	…	Bit2	Bit1	Bit0

WA_REVP=WATT_reg/(32*1.3655)
When the value of X_WATT register is less than this threshold, the REVP bit of the Status register don't update and set to 0.
Note: this register only affects the status register.

CF Frequency Divider Register (WA_CFDIV)

CF output divider(WA_CFDIV) Addr：19H			Type：R/W		Default：001H	
Bit11	Bit10	Bit9	…	Bit2	Bit1	Bit0

At maximum signal level ±660mV（467mV rms）				
	Typical value			
CFDIV register(30H)	The frequency of CF（Hz）	WATT register	IA_RMS register	V_RMS register
1(001H)	1.95	6500000	5650000	5650000
2(002H)	3.91			
4(004H)	7.81			
8(008H)	15.63			
16(010H)	31.25			
32(020H)	62.50			
64(040H)	125.00			
128(080H)	250.00			
256(0100H)	500.00			

Active Power Offset Register (A_WATTOS, B_WATTOS)

Active power offset of channel A (A_WATTOS) Addr：1AH		Type：R/W	Default：000H
Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

Active power offset of channel B (B_WATTOS) Addr：1BH		Type：R/W	Default：000H
Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

Complement, Bit [11] is the sign bit. Power offset compensation in small power.

Assume in small power condition (5%In, PF=1.0), error of the energy meter is Err, the data of x_WATT register is WATT_Data.

If Err<0, then x_WATTOS=int ((WATT_Data*(-Err)/1.3655));

If Err<0, then x_WATTOS=int((WATT_Data*(-Err)/1.3655))+4096;

Active Power Gain Register (A_WATTGN, B_WATTGN)

Active power gain of channel A(A_WATTGN) Addr：1CH		Type：R/W	Default：000H
Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

Active power gain of channel B(B_WATTGN) Addr：1DH		Type：R/W	Default：000H
Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

Complement, Bit [11] is the sign bit.

Output WATT_Reg=Active Power $*\frac{\text{X\_WATTGN}}{2^{12}}$

Phase Calibration Registers (IA_PHCAL,IB_PHCAL,V_ PHCAL)

PHCAL Register(IA_PHCAL) Addr：1EH			Type：R/W			Default：00H	
Enable bit	Phase compensaton of current channel A						
D7	D6	D5	D4	D3	D2	D1	D0

PHCAL Register(IB_PHCAL) Addr：1FH			Type：R/W			Default：00H	
Enable bit	Phase compensaton of current channel B						
D7	D6	D5	D4	D3	D2	D1	D0

PHCAL Register(V_PHCAL) Addr：20H			Type：R/W			Default：00H	
Enable bit	Phase compensaton of voltage channel						
D7	D6	D5	D4	D3	D2	D1	D0

Bit[7] is enable bit, when Bit[7]＝0,disable compensation; Bit[7]＝1,enable compensation. Bit[6:0] used to adjust the delay time， 1.1us/1LSB. With a line frequency of 50Hz, the resolution is 360°×（1/900KHz）×50Hz=0.02°, The adjustable range is 0°~2.54°.

1LSB of register may cause the accuracy Error change 0.0605%.

If Error>=0, write the adjust value to Phase compensation of current channel.

If Error<0, write the adjust Value to Phase compensation of voltage channel.

The value=int (|Err|/0.0605) +127.

Apparent power offset Register (VA_OS)

Apperant power offset (VAOS) Addr：21H	Type：R/W	Default：000H
Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

Complement, Bit [11] is the sign bit.

VA=VA0+VAOS.

Apparent Power Gain Register (VAGN)

Apparent power gain (VAGN) Addr：22H	Type：R/W	Default： 000H
Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

Complement, Bit [11] is the sign bit.

Output VA_reg=VA0 $*$ $(1+\frac{VAGN}{2^{12}})$

RMS Gain Register (IA_RMSGN, IB_RMSGN and V_RMSGN)

RMS gain of current A(IA_RMSGN) Addr：23H	Type：R/W	Default：000H
Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

RMS gain of current B(IB_RMSGN) Addr：24H	Type：R/W	Default：000H
Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

RMS gain of voltage(V_RMSGN) Addr：25H		Type：R/W	Default：000H
Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

Complement, Bit [11] is the sign bit.

Output x_RMS_reg=X_RMS0 $*$ $(1+\frac{\text{X\_RMSGN}}{2^{12}})$

RMS Offset Registers (IA_RMSOS, IB_RMSOS, V_RMSOS)

RMS offset of current A(IA_RMSOS) Addr：26H		Type：R/W	Default：000H
Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

RMS offset of current B(IB_RMSOS) Addr：27H		Type：R/W	Default：000H
Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

RMS offset of voltage(V_RMSOS) Addr：28H		Type：R/W	Default：000H
Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

Complement, Bit [11] is the sign bit.

IX_RMS=$\sqrt{\text{IX\_RMS0}^2+\text{IX\_RMSOS}*2^{17}}$

RMS Noload Threshold Register (RMS_CREEP)

RMS Noload threshold(RMS_CREEP) Addr：29H		Type：R/W	Default：000H
Bit11	Bit10～8	Bit7～4	Bit3～0

$$\text{RMS}=\begin{cases}0 & RMS<RMS\_CREEP\times 2\ \times 1.3655\\ \text{RMS}, & RMS=RMS\_CREEP\times 2\ \times 1.3655\end{cases}$$

Please refer to chapter “No-load threshold of RMS”

Small signal compensation of Active power (WA_LOS)

These two registers do not need change. Keep the default value.

Channel Offset Registers (IA_CHOS, IB_CHOS, V_CHOS)

These two registers do not need change. Keep the default value.

Calibration Gain Register (IA_CHGN, IB_CHGN, V_CHGN)

Calibration gain of current A (IA_CHGN) Addr：2EH	Type：R/W	Default：000H

Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

Calibration gain of current B (IB_CHGN) Addr：2FH		Type：R/W	Default：000H
Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

Calibration gain of Voltage (V_CHGN) Addr：30H		Type：R/W	Default：000H
Bit11(sign bit)	Bit10～8	Bit7～4	Bit3～0

Complement, Bit [11] is the sign bit.

L line gain calibration is performed when PF=1.0 and the current is In.

Assume the error output of the calibration bench is Err.

If Err <0, then GN=int $(2^{12} \times \frac{-Err}{1+Err})$

If Err>=0, then GN=int $(2^{12} + 2^{12} \times \frac{-Err}{1_{Err}})$

The Err can be calibrated when the Err range is -33.3%~+99.9%

The GN value can be set to 2EH or 30H register.

Line Energy Accumulation Cycle Register (LINECYC)

Line Energy Cycle(LINECY) Addr：31H				Type：R/W	Default：000H	
Bit11	Bit10	Bit9	…	Bit2	Bit1	Bit0

Note: set the LINE_WATTHR, LINE_VARHR.LINE_VAHR update period. The LSB of the LINECYC register is 0.1S. At the end of a line cycle accumulation cycle, the LINE_WATTHR register is updated. The LINE_WATTHR register hold its current value until the end of the next line cycle period, when the content is replaced with the new reading. If a new value is written to the LINECYC register midway through a line cycle accumulation, the new value is not internally loaded until the end of a line cycle period.

Zero-Crossing TimeOut Register (ZXTOUT)

Zero-Crossing TimeOut(ZXTOUT) Addr：32H		Type：R/W	Default：FFFFH
Bit15～12	Bit11～8	Bit7～4	Bit3～0

70.5uS/LSB.

Please refer to chapter “Electric parameters monitor”

SAG Detection Register (SAGCYC, SAGLVL)

(SAGCYC) Addr：33H				Type：R/W		Default：FFH	
D7	D6	D5	D4	D3	D2	D1	D0

10mS/LSB.

(SAGLVL) Addr：34H	Type：R/W	Default：FFH

Bit11	Bit10～8	Bit7～4	Bit3～0

The value compare with V_RMS [23:12].

Please refer to chapter "Electric parameters monitor"

Peak Detection Register (IA_PKLVL, IB_PKLVL,V_PKLVL)

Current A peak level(IA_PKLVL) Addr：35H		Type：R/W	Default：000H
Bit11	Bit10～8	Bit7～4	Bit3～0

Current B peak level(V_PKLVL) Addr：36H		Type：R/W	Default：000H
Bit11	Bit10～8	Bit7～4	Bit3～0

Voltage peak level(V_PKLVL) Addr：37H		Type：R/W	Default：000H
Bit11	Bit10～8	Bit7～4	Bit3～0

Please refer to chapter "Electric parameters monitor"

Logic output control register(ATT_SEL)

(ATT_SEL) Addr：38H		Type：R/W	Default：0000H
Bit15~12	Bit11～8	Bit7～4	Bit3～0
AT3	AT2	AT1	AT0

The BL6523B contains four logic output pin(AT0~AT3) that can output some measurement states. The AT_SEL register is used to set the AT0~AT3 pin output, AT_SEL [3：0] corresponds to AT0; AT_SEL[7：4] corresponds to AT1; AT_SEL[11：8] corresponds to AT2; AT_SEL[15：12] corresponds to AT3. The default value of AT_SEL register is 0x0000, the default output is AT0=FAULT, AT1=REVP, AT2=ZX, AT3=nSAG.

BIT[3:0]	ATX OUTPUT	DEFAULT	DESCRIPTION
0000			AT0=FAULT、AT1=REVP、AT2=ZX、AT3=nSAG
0001	nSAG	0	Sag event has occurred
0010	ZXTO	0	Indicates that zero crossing has been missing on the voltage channel for the length of time specified in the ZXTOUT register
0011	ZX	0	Voltage channel zero crossing
0100	PKIA	0	Current channel A peak has exceeded IAPKLVL
0101	PKIB	0	Current channel B peak has exceeded IBPKLVL
0110	PKV	0	Voltage peak has exceeded VPKLVL
0111	REVP	0	Sign of active power has changed to negative
1000	APEHF	0	Active energy register(WATTR) is half full
1001	VAPEHF	0	Apparent energy register(VAHR) is half full
1010	FAULT	0	Fault=1 indicates the imbalance in two channels rms, the difference is greater than the FAULTLVL
1011	CHSEL	0	0 indicates measureing power with channel A; 1 indicates measureing power with channel B;

其余	Reversed	0	Reserved

Interrupt Mask Register(MASK)

Interrupt Mask Register(MASK) Addr：39H			Type:R/W		Default:000H
D11	D10	D9	D8…D2	D1	D0

BITS	INTERRUP NAME	DEFAULT	DESCRIPTION
0	SAG	0	Enable the interrupt that sag event has occurred
1	ZXTO	0	Enable the interrupt of ZXTO
2	ZX	0	Enable the interrupt of ZX
3	PKIA	0	Enable the interrupt of PAIA
4	PKIB	0	Enable the interrupt of PKIB
5	PKV	0	Enable the interrupt of PKV
6	REVP	0	Enable the interrupt of REVP
7	APEHF	0	Enable the interrupt of APEHF
8	VAPEHF	0	Enable the interrupt of VAPEHF
9	FAULT	0	Enable the interrupt of FAULT
10	CHSEL	0	Enable the interrupt of CHSEL
Others	Reversed	0	Reversed

Interrupt Status Register

Interrupt Status Register(STATUS) Addr：3AH			Type:Read		Default:000H
D11	D10	D9	D8…D2	D1	D0

BIT LOCATION	INTERRUPT FLAG	DEFAULT	DESCRIPTION
0	SAG	0	Indicates that an interrupt was caused by a Sag event
1	ZXTO	0	Indicates that zero crossing has been missing on the voltage channel for the length of time specified in the ZXTOUT register
2	ZX	0	Voltage channel zero crossing
3	PKIA	0	Current channel A peak has exceeded I_PKLVL
4	PKIB	0	Current channel B peak has exceeded I_PKLVL
5	PKV	0	Voltage peak has exceeded V_PKILVL
6	REVP	0	Indicates the active power has gone from positive to negative(instantaneous power)
7	APEHF	0	Indicates that an interrupt was caused because

			WATTHR register is more than half full
8	VAPEHF	0	Indicates that an interrupt was caused because WAHR register is more than half full
9	FAULT	0	Indicates the Line and Neutral signal imbalance
10	CHSEL	0	Indicates the channel of CF output
11	VREF_LOW	0	Indicates that the reference voltage is lower than 2V

Read/Write Register (Read/Write)

Read Register(READ) Addr：3BH			Type：R		默认值：000000H	
Bit23	Bit22	Bit21	…	Bit2	Bit1	Bit0

Write Register(WRITE) Addr：3CH			Type：R		默认值：000000H	
Bit23	Bit22	Bit21	…	Bit2	Bit1	Bit0

Note: these register store the data that is just read or written through the UART interface.

Checksum Register (CHKSUM)

Checksum Register(CHKSUM) Addr：3DH			Type：R		默认值：0121F2H	
Bit23	Bit22	Bit21	…	Bit2	Bit1	Bit0

Note: this register is the sum of register 14H~39H Value. If the value of these register changed, the CHKSUM will be written the new value automatically.

Write Protection Register (WRPROT)

Write Protection Register(WRPROT) Addr：3EH			Type：R		默认值：00H	
Bit7	Bit6	Bit5	…	Bit2	Bit1	Bit0

Note: when the calibration registers of BL6523GX can be written after only the 55H is written to this register.