NCP1392B, NCP1392D

High-Voltage Half-Bridge Driver with Inbuilt Oscillator

The NCP1392B/D is a self−oscillating high voltage MOSFET driver primarily tailored for the applications using half bridge topology. Due to its proprietary high−voltage technology, the driver accepts bulk voltages up to 600 V. Operating frequency of the driver can be adjusted from 25 kHz to 480 kHz using a single resistor. Adjustable Brown−out protection assures correct bulk voltage operating range. An internal 100 ms or 12.6 ms PFC delay timer guarantee that the main downstream converter will be turned on in the time the bulk voltage is fully stabilized. The device provides fixed dead time which helps lowering the shoot−through current.

Features

- Wide Operating Frequency Range − from 25 kHz to 480 kHz
- Minimum frequency adjust accuracy ±3%
- Fixed Dead Time − 0.6 μs or 0.3 μs
- Adjustable Brown−out Protection for a Simple PFC Association
- 100 ms or 12.6 ms PFC Delay Timer
- Non−latched Enable Input
- Internal 16 V V_{CC} Clamp
- Low Startup Current of 50 μA
- 1 A / 0.5 A Peak Current Sink / Source Drive Capability
- Operation up to 600 V Bulk Voltage
- Internal Temperature Shutdown
- SOIC−8 Package
- These are Pb−Free Devices

Typical Applications

- Flat Panel Display Power Converters
- Low Cost Resonant SMPS
- High Power AC/DC Adapters for Notebooks
- Offline Battery Chargers
- Lamp Ballasts

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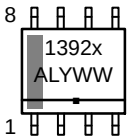
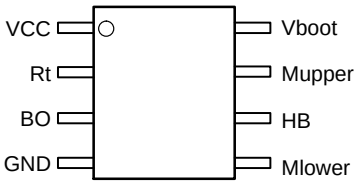
SOIC−8
CASE 751

MARKING DIAGRAMS



1392x	= Specific Device Code x = B or D
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

PINOUT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NCP1392BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1392DDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

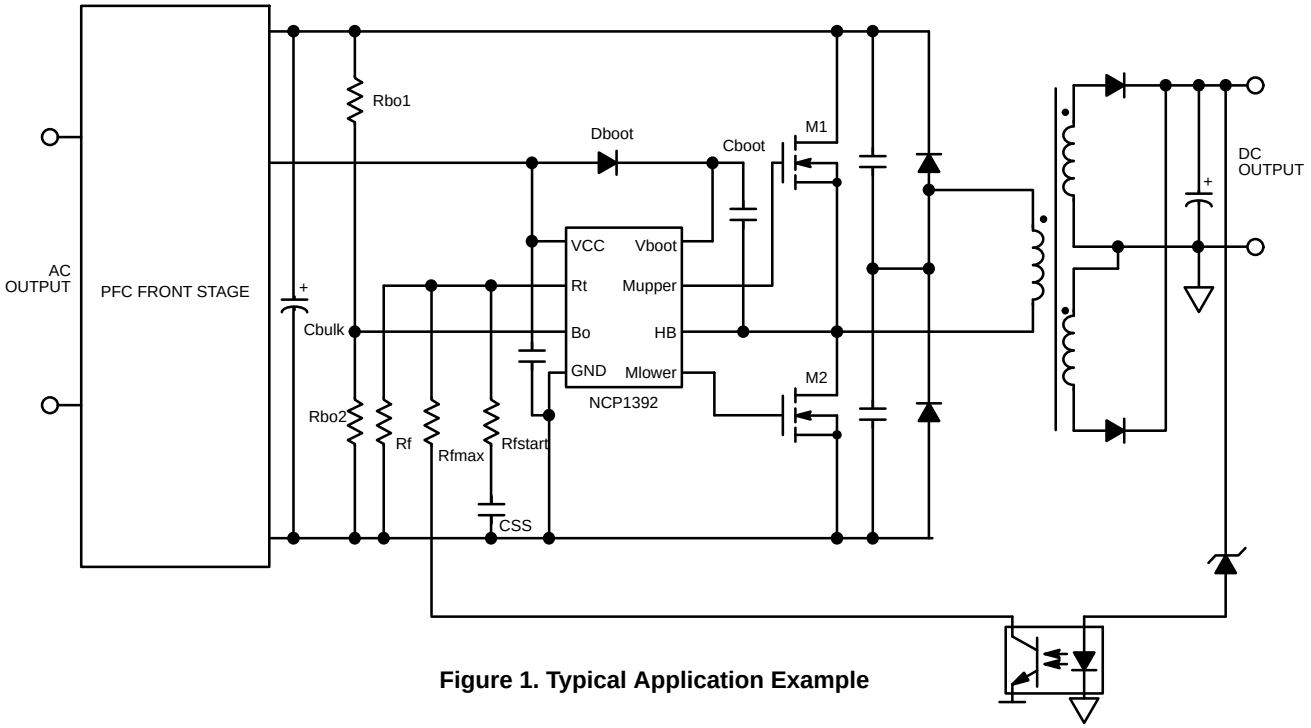


Figure 1. Typical Application Example

PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Function	Pin Description
1	V_{CC}	Supplies the Driver	The driver accepts up to 16 V (given by internal zener clamp)
2	Rt	Timing Resistor	Connecting a resistor between this pin and GND, sets the operating frequency
3	BO	Brown−Out/Enable Input	Brown−Out function detects low input voltage conditions. Enable Input, when brought above Vref_EN, stops the driver. Operation is then restored (without any delay) when BO pin voltage drops by EN_Hyste below Vref_EN.
4	GND	IC Ground	
5	Mlower	Low−Side Driver Output	Drives the lower side MOSFET
6	HB	Half−Bridge Connection	Connects to the half−bridge output
7	Mupper	High−Side Driver Output	Drives the higher side MOSFET
8	Vboot	Bootstrap Pin	The floating supply terminal for the upper stage

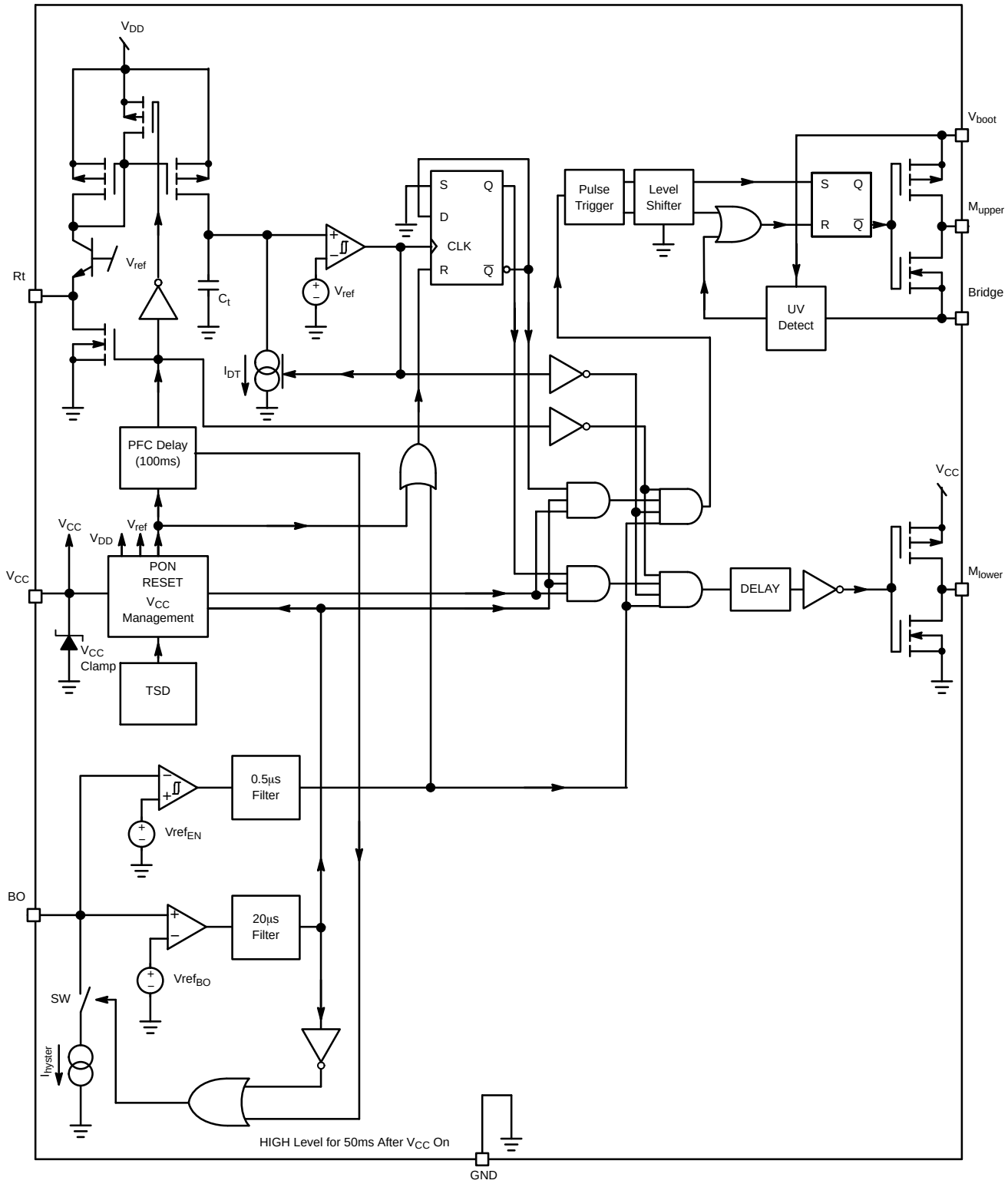


Figure 2. Internal Circuit Architecture (B Version)

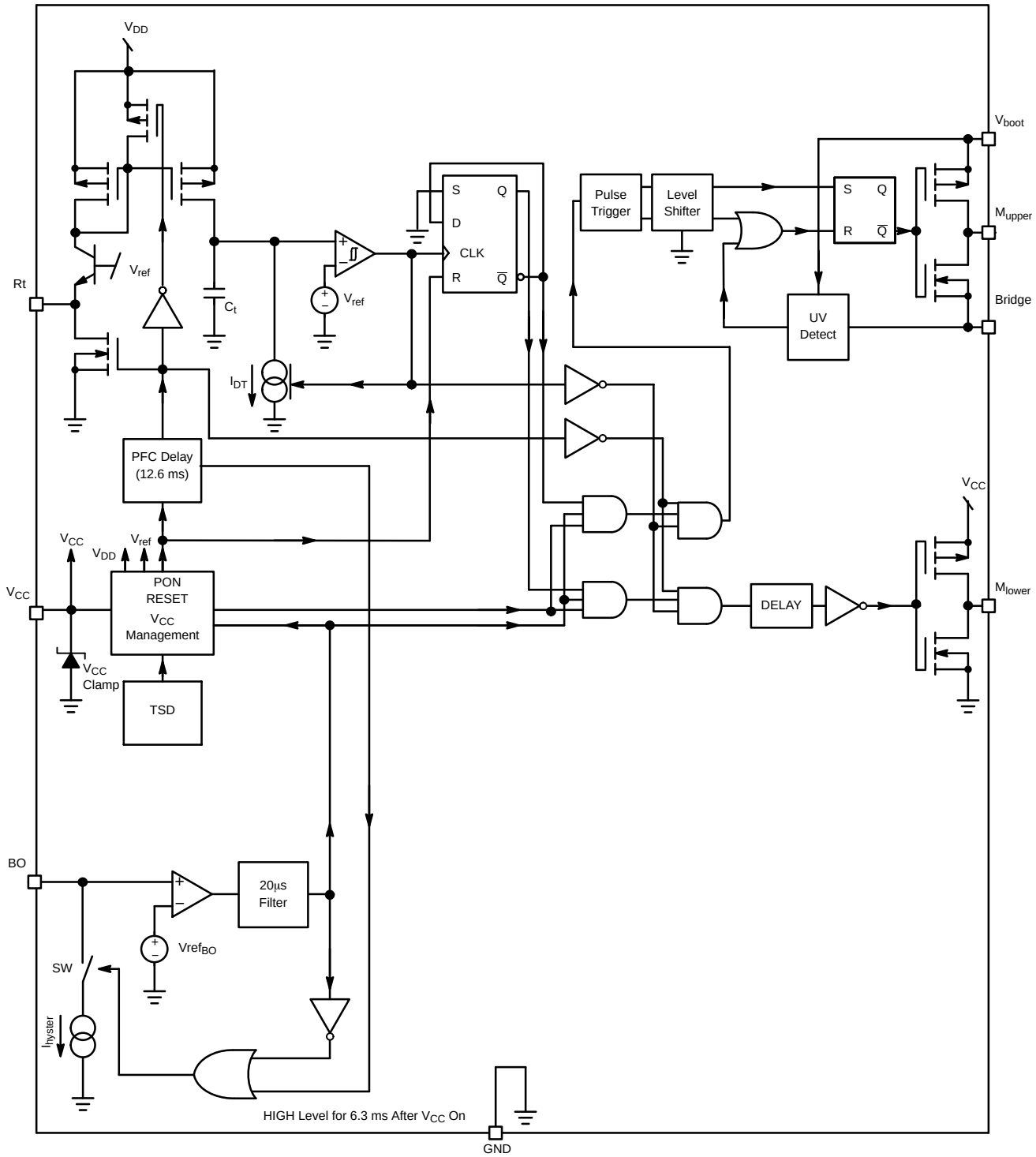


Figure 3. Internal Circuit Architecture (D Version)

MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
Vbridge	High Voltage Bridge Pin − Pin 6	−1 to +600	V
Vboot − Vbridge	Floating Supply Voltage	0 to 20	V
VDRV_HI	High−Side Output Voltage	Vbridge − 0.3 to Vboot + 0.3	V
VDRV_LO	Low−Side Output Voltage	−0.3 to V_{CC} +0.3	V
dVbridge/dt	Allowable Output Slew Rate	±50	V/ns
I_{CC}	Maximum Current that Can Flow into V_{CC} Pin (Pin 1), (Note 1)	20	mA
V_Rt	Rt Pin Voltage	−0.3 to 5	V
	Maximum Voltage, All Pins (Except Pins 4 and 5)	−0.3 to 10	V
$R_{\theta JA}$	Thermal Resistance Junction−to−Air, IC Soldered on 50 mm^2 Cooper 35 μm	178	°C/W
$R_{\theta JA}$	Thermal Resistance Junction−to−Air, IC Soldered on 200 mm^2 Cooper 35 μm	147	°C/W
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, Human Body Model (All Pins Except HV Pins 6, 7 and 8)	2.0	kV
	ESD Capability, Human Body Model (HV Pins 6, 7 and 8)	1.5	kV
	ESD Capability, Machine Model	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains internal zener clamp connected between V_{CC} and GND terminals. Current flowing into the V_{CC} pin has to be limited by an external resistor when device is supplied from supply which voltage is higher than VCC_{clamp} (16 V typically). The I_{CC} parameter is specified for VBO = 0 V.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V, unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
SUPPLY SECTION						
Turn−On Threshold Level, V_{CC} Going Up	1	VCC_{ON}	10	11	12	V
Minimum Operating Voltage after Turn−On	1	VCC_{min}	8	9	10	V
Startup Voltage on the Floating Section	1	$Vboot_{ON}$	7.8	8.8	9.8	V
Cutoff Voltage on the Floating Section,	1	$Vboot_{min}$	7	8	9	V
V_{CC} Level at which the Internal Logic gets Reset	1	VCC_{reset}	−	6.5	−	V
Startup Current, V_{CC} < VCC_{ON}, 0°C ≤ T_{amb} ≤ +125°C	1	I_{CC}	−	−	50	μA
Startup Current, V_{CC} < VCC_{ON}, −40°C ≤ T_{amb} < 0°C	1	I_{CC}	−	−	65	μA
Internal IC Consumption, No Output Load on Pins 8/7 − 5/4, Fsw = 100 kHz	1	$I_{CC}1$	−	2.2	−	mA
Internal IC Consumption, 1 nF Output Load on Pins 8/7 − 5/4, Fsw = 100 kHz	1	$I_{CC}2$	−	3.4	−	mA
Consumption in Fault Mode (Drivers Disabled, V_{CC} > $V_{CC(min)}$, R_T = 3.5 kΩ)	1	$I_{CC}3$	−	2.56	−	mA
Consumption During PFC Delay Period, 0°C ≤ T_{amb} ≤ +125°C		$I_{CC}4$	−	−	400	μA
Consumption During PFC Delay Period, −40°C ≤ T_{amb} < 0°C		$I_{CC}4$	−	−	470	μA
Internal IC Consumption, No Output Load on Pin 8/7 F_{SW} = 100 kHz	8	I_{boot1}	−	0.3	−	mA
Internal IC Consumption, 1 nF Load on Pin 8/7 F_{SW} = 100 kHz	8	I_{boot2}	−	1.44	−	mA
Consumption in Fault Mode (Drivers Disabled, V_{boot} > $Vboot_{min}$)	8	I_{boot3}	−	0.1	−	mA
V_{CC} Zener Clamp Voltage @ 20 mA	1	VCC_{clamp}	15.4	16	17.5	V
INTERNAL OSCILLATOR						
Minimum Switching Frequency (R_t = 35 kΩ on Pin 2 for D_T = 600 ns, R_t = 70 kΩ on Pin 2 for D_T = 300 ns)	2	F_{SW} min	24.25	25	25.75	kHz
Maximum Switching Frequency (B Version), R_t = 3.5 kΩ on Pin 2, D_T = 600 ns	2	F_{SW} maxB	208	245	282	kHz
Maximum Switching Frequency (D Version), R_t = 3.5 kΩ on Pin 2, D_T = 300 ns	2	F_{SW} maxD	408	480	552	kHz
Reference Voltage for all Current Generations	2	V_{ref} RT	3.33	3.5	3.67	V
Internal Resistance Discharging $C_{soft-start}$	2	$Rt_{discharge}$	−	500	−	Ω
Operating Duty Cycle Symmetry	5, 7	DC	48	50	52	%

NOTE: Maximum capacitance directly connected to Pin 2 must be under 100 pF.

DRIVE OUTPUT						
Output Voltage Rise Time @ CL = 1 nF, 10−90% of Output Signal	5, 7	T_r	−	40	−	ns
Output Voltage Fall Time @ CL = 1 nF, 10−90% of Output Signal	5, 7	T_f	−	20	−	ns
Source Resistance	5, 7	R_{OH}	−	12	−	Ω
Sink Resistance	5, 7	R_{OL}	−	5	−	Ω
Deadtime (B Version)	5,7	T_{deadB}	540	610	720	ns
Deadtime (D Version)	5,7	T_{deadD}	260	305	360	ns
Leakage Current on High Voltage Pins to GND (600 Vdc)	6,7,8	IHV_{Leak}	−	−	5	μA
PROTECTION						
Brown−Out Input Bias Current	3	IBO_{bias}	−	0.01	−	μA
Brown−Out Level	3	VBO	0.95	1	1.05	V
Hysteresis Current, V_{pin3} < VBO	3	IBO	15.6	18.2	20.7	μA
Reference Voltage for EN Input (B Version)	3	V_{ref} EN	1.9	2	2.1	V
EN Comparator (not available in D Version)	−	V_{ref} EN_D	−	−	−	V
Enable Comparator Hysteresis	3	EN_Hyste	−	100	−	mV

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V, unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
PROTECTION						
Propagation Delay Before Drivers are Stopped	3	EN_Delay	−	0.5	−	μs
Delay Before Any Driver Restart (B Version)	−	PFC Delay	−	100	−	ms
Delay Before Any Driver Restart (D Version)	−	PFC Delay	−	12.6	−	ms
Temperature Shutdown	−	TSD	140	−	−	°C
Hysteresis	−	TSDhyste	−	30	−	°C
Brown Out discharge time (B Version) (Note 2)	−	BOdisch	−	50	−	ms
Brown Out discharge time (D Version) (Note 2)	−	BOdisch	−	6.3	−	ms

2. Guaranteed by design.

TYPICAL CHARACTERISTICS

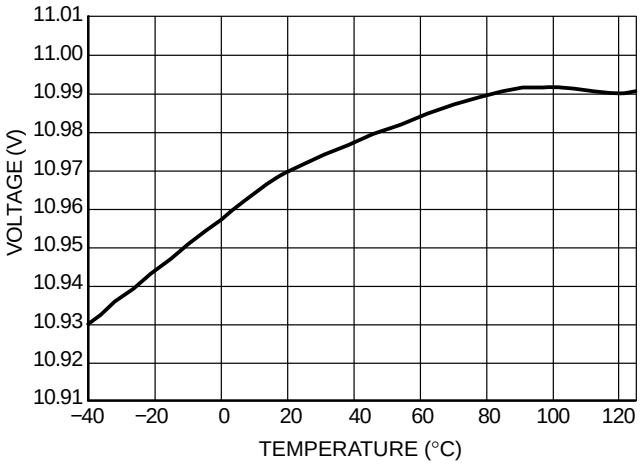


Figure 4. V_{CCon}

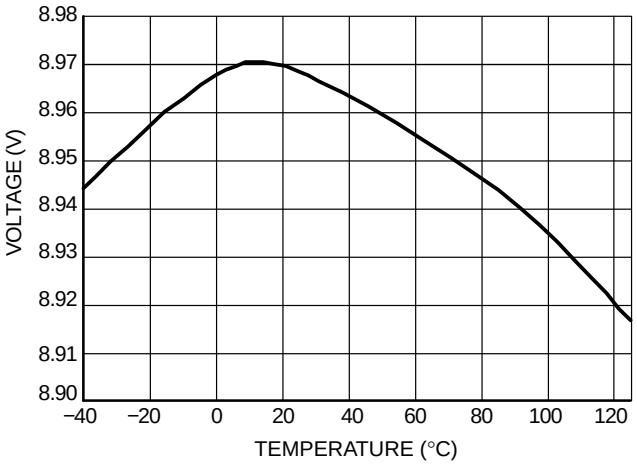


Figure 5. V_{CCmin}

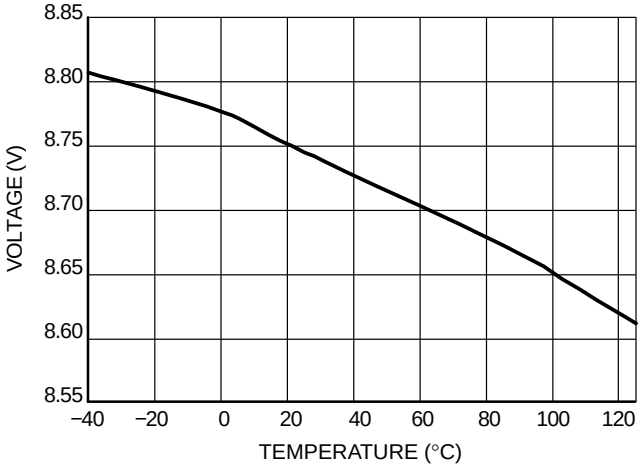


Figure 6. V_{BOOTon}

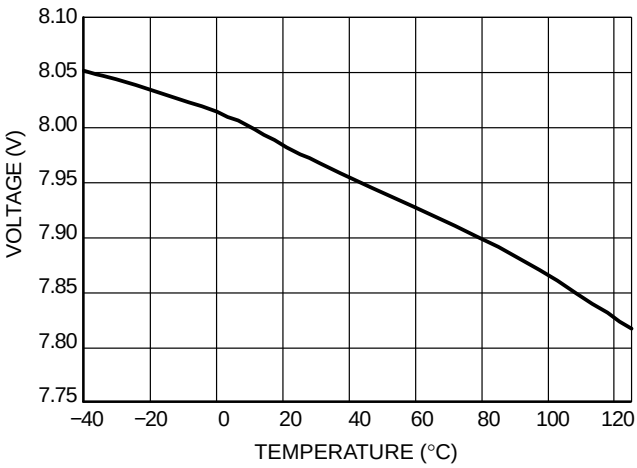


Figure 7. $V_{BOOTmin}$

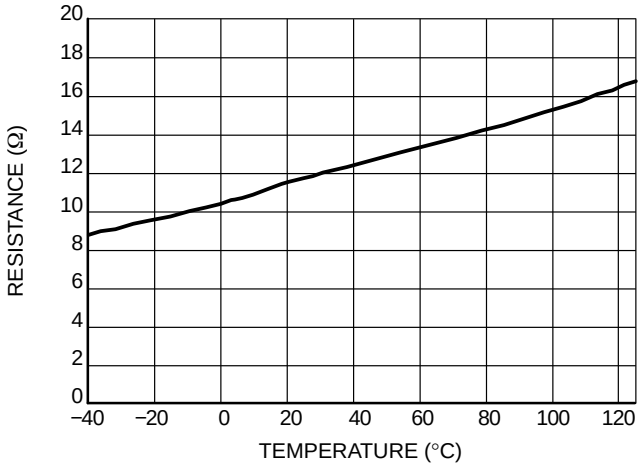


Figure 8. R_{OH}

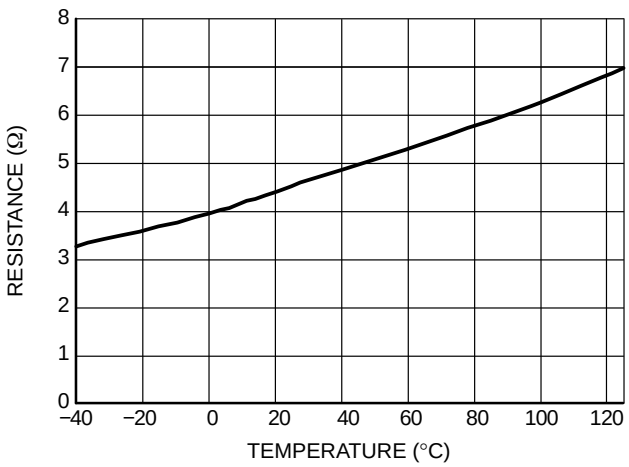


Figure 9. R_{OL}

TYPICAL CHARACTERISTICS

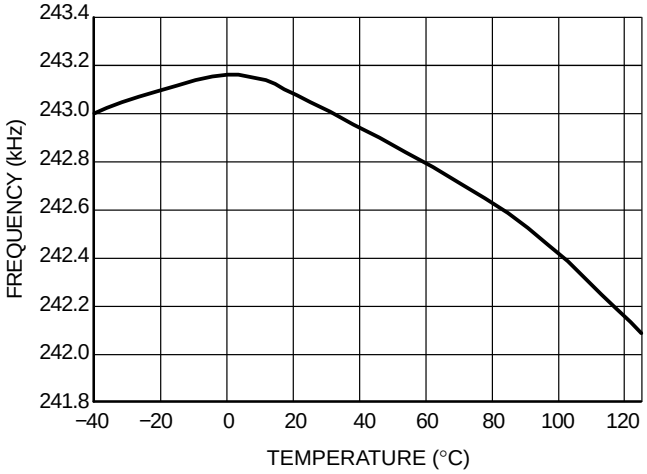


Figure 10. F_{SWmax} (B Version)

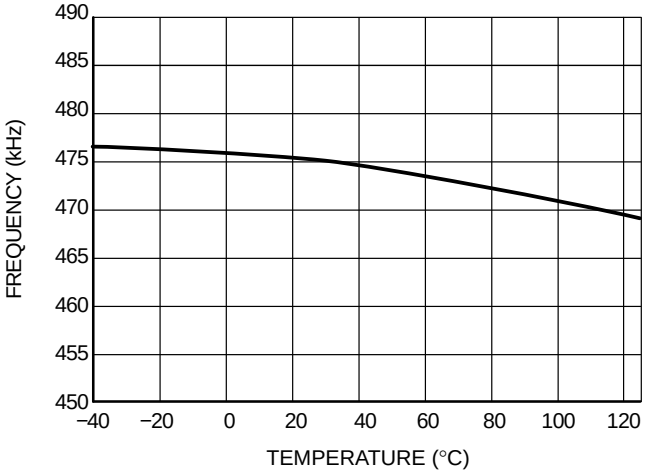


Figure 11. F_{SWmax} (D Version)

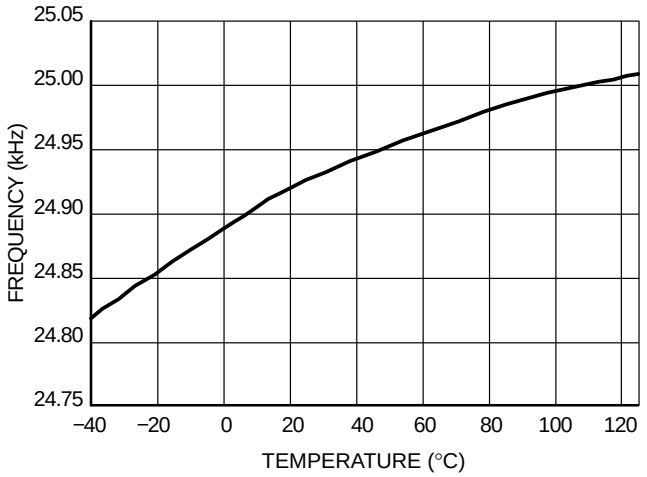


Figure 12. F_{SWmin} (B Version)

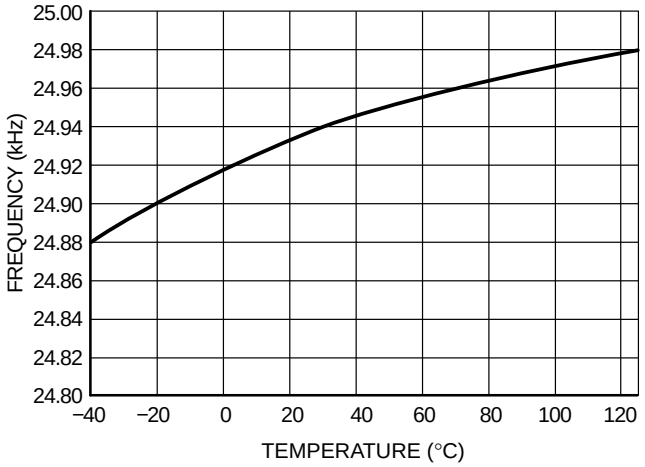


Figure 13. F_{SWmin} (D Version)

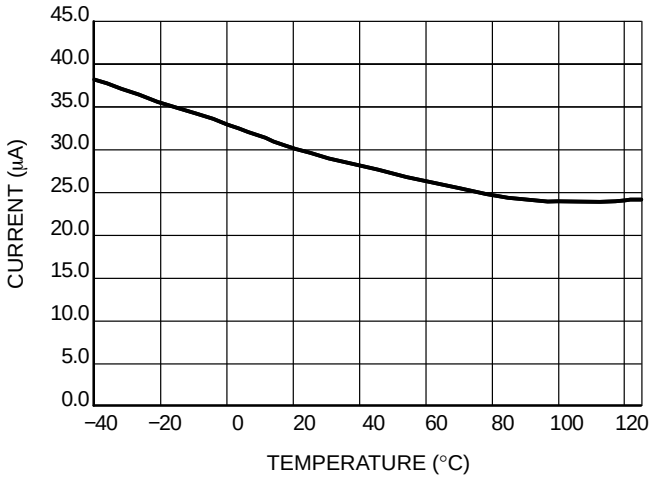


Figure 14. $I_{CC\_startup}$

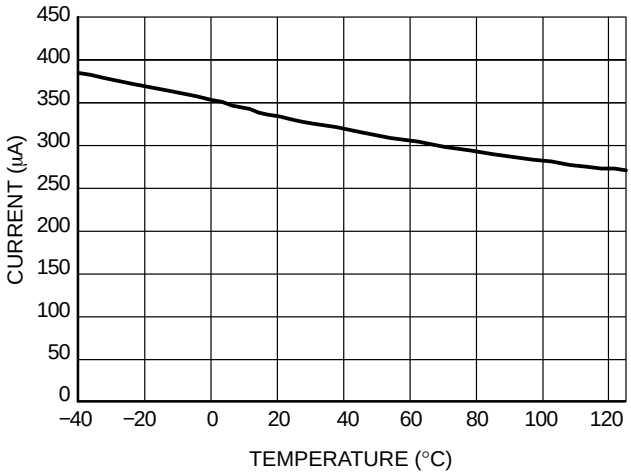


Figure 15. I_{CC4}

TYPICAL CHARACTERISTICS

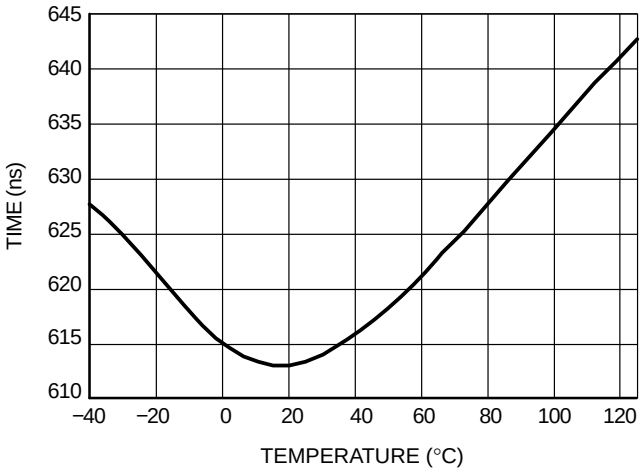


Figure 16. T_{dead} (B Version)

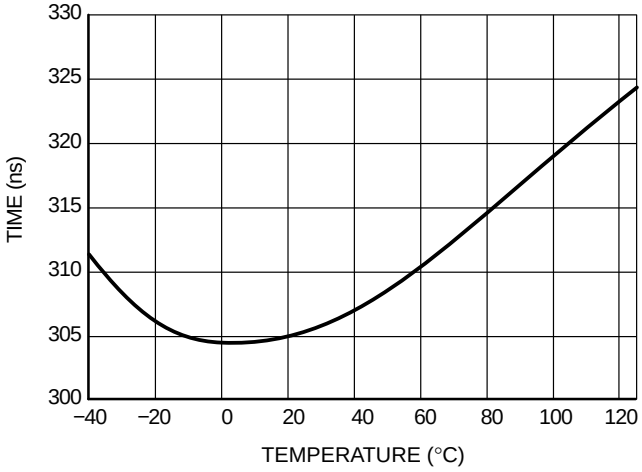


Figure 17. T_{dead} (D Version)

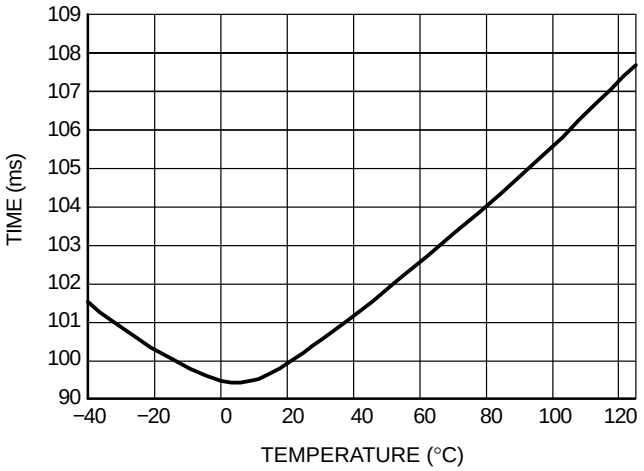


Figure 18. PFC_{delay} (B Version)

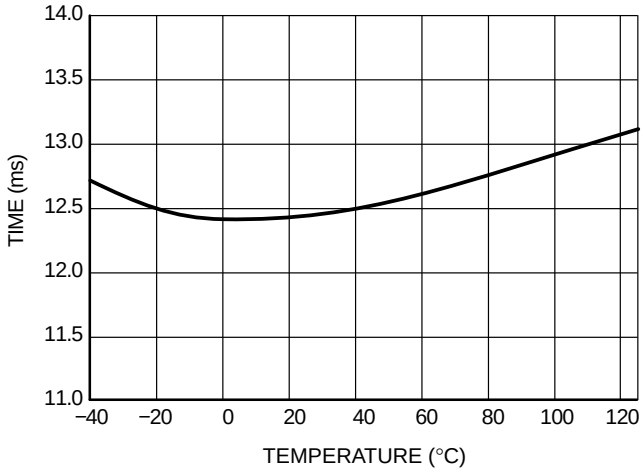


Figure 19. PFC_{delay} (D Version)

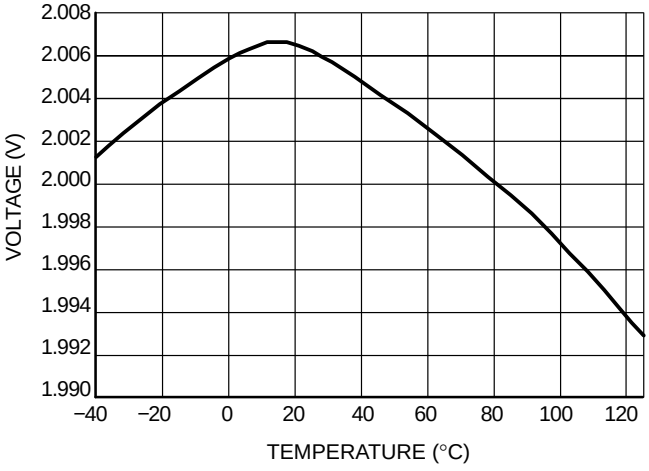


Figure 20. V_{ref_EN}

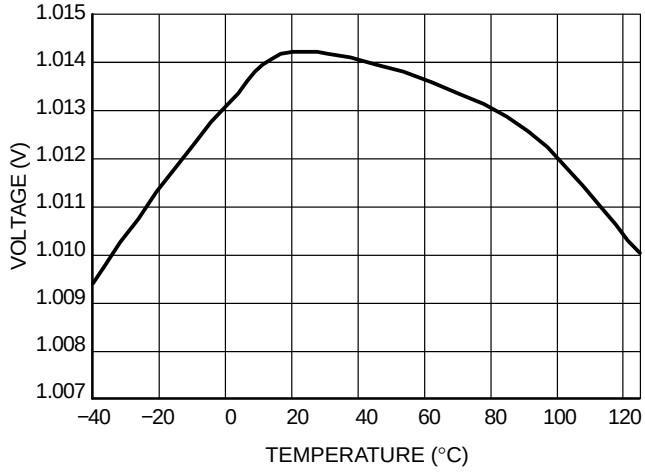


Figure 21. V_{BO}

TYPICAL CHARACTERISTICS

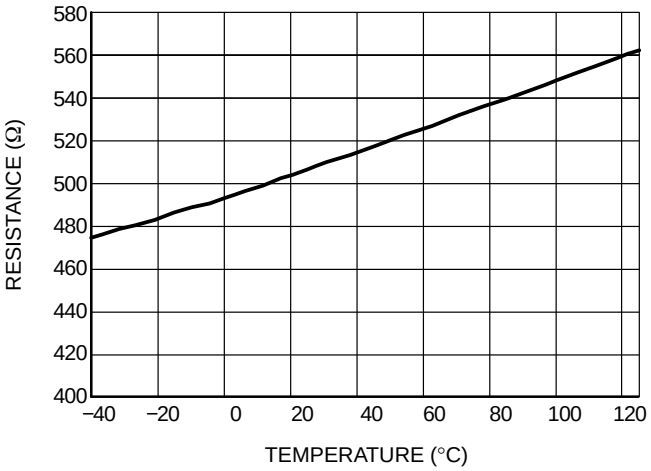


Figure 22. $R_{t\_discharge}$

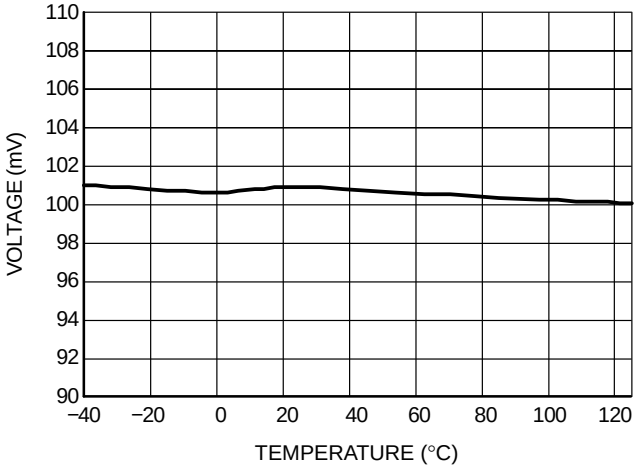


Figure 23. EN_{hyste}

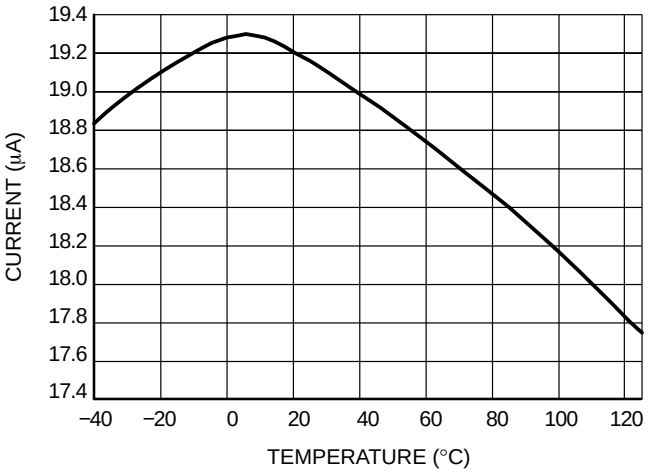


Figure 24. I_{BO}

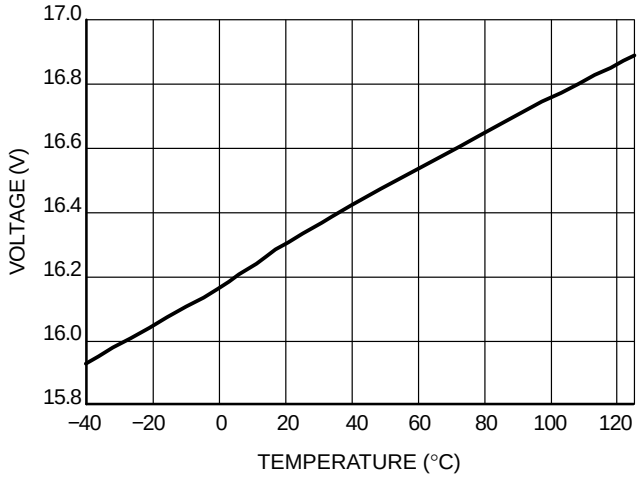


Figure 25. V_{CC_clamp}

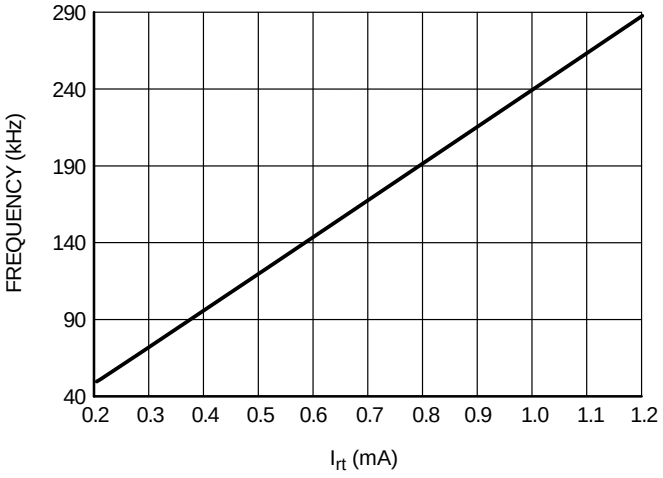


Figure 26. I_{rt} and Appropriate Frequency (B Version)

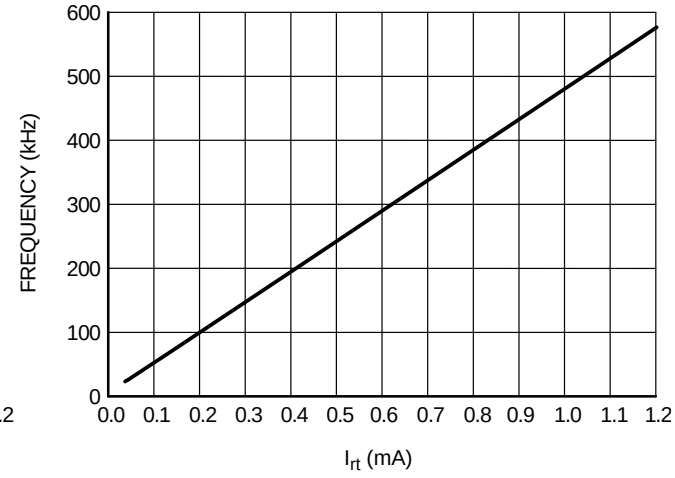


Figure 27. I_{rt} and Appropriate Frequency (D Version)

APPLICATION INFORMATION

The NCP1392 is primarily intended to drive low cost half bridge applications and especially resonant half bridge applications. The IC includes several features that help the designer to cope with resonant SPMS design. All features are described thereafter:

- **Wide Operating Frequency Range**: The internal current controlled oscillator is capable to operate over wide frequency range. Minimum frequency accuracy is ±3%.
- **Fixed Dead−Time**: The internal dead−time helping to fight with cross conduction between the upper and lower power transistors. Three versions with different dead time values are available to cover wide range of applications.
- **PFC Timer**: Fixed delay is placed to IC operation whenever the driver restarts (VCC_{ON} or BO_OK detect events). This delay assures that the bulk voltage will be stabilized in the time the driver provides pulses on the outputs. Another benefit of this delay is that the soft start capacitor will be full discharged before any restart.
- **Brown−Out Detection**: The BO input monitors bulk voltage level via resistor divider and thus assures that the application is working only for wanted bulk voltage band. The BO input sinks current of 18.2 μA until the $Vref_{BO}$ threshold is reached. Designer can thus adjust the bulk voltage hysteresis according to the application needs.
- **Non−Latched Enable Input**: The enable comparator input is connected in parallel to the BO terminal to allow the designer stop the output drivers when needed. There is no PFC delay when enable input is released so skip mode for resonant SMPS applications and dimming for light ballast applications are possible.
- **Internal V_{CC} Clamp**: The internal zener clamp offers a way to prepare passive voltage regulator to maintain V_{CC} voltage at 16 V in case the controller is supplied from unregulated power supply or from bulk capacitor.
- **Low Startup Current**: This device features maximum startup current of 50 μA which allows the designer to use high value startup resistor for applications when driver is supplied from the auxiliary winding. Power dissipation of startup resistor is thus significantly reduced.

Current Controlled Oscillator

The current controlled oscillator features a high−speed circuitry allowing operation from 50 kHz up to 960 kHz. However, as a division by two internally creates the two Q and $\overline{Q}$ outputs, the final effective signal on output Mlower and Mupper switches in half frequency range. The VCO is configured in such a way that if the current that flows out from the Rt pin increases, the switching frequency also goes up. Figure 28 shows the architecture of this oscillator.

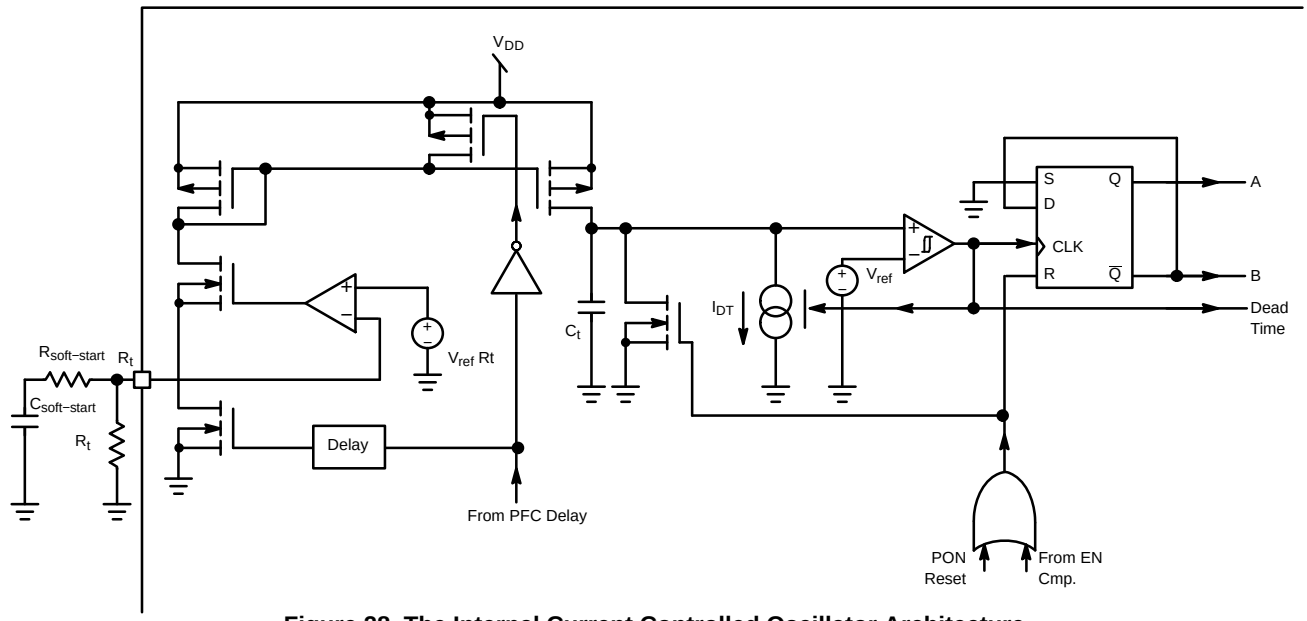


Figure 28. The Internal Current Controlled Oscillator Architecture

The internal timing capacitor Ct is charged by current which is proportional to the current flowing out from the Rt pin. The discharging current I_{DT} is applied when voltage on this capacitor reaches 2.5 V. The output drivers are disabled during discharge period so the dead time length is given by the discharge current sink capability. Discharge sink is disabled when voltage on the timing capacitor reaches zero and charging cycle starts again. The charging current and thus also whole oscillator is disabled during the PFC delay period to keep the IC consumption below 400 μA.

This is valuable for applications that are supplied from auxiliary winding and V_{CC} capacitor is supposed to provide energy during PFC delay period.

For the resonant applications and light ballast applications it is necessary to adjust minimum operating frequency with high accuracy. The designer also needs to limit maximum operating and startup frequency. All these parameters can be adjusted using few external components connected to the Rt pin as depicted in Figure 29.

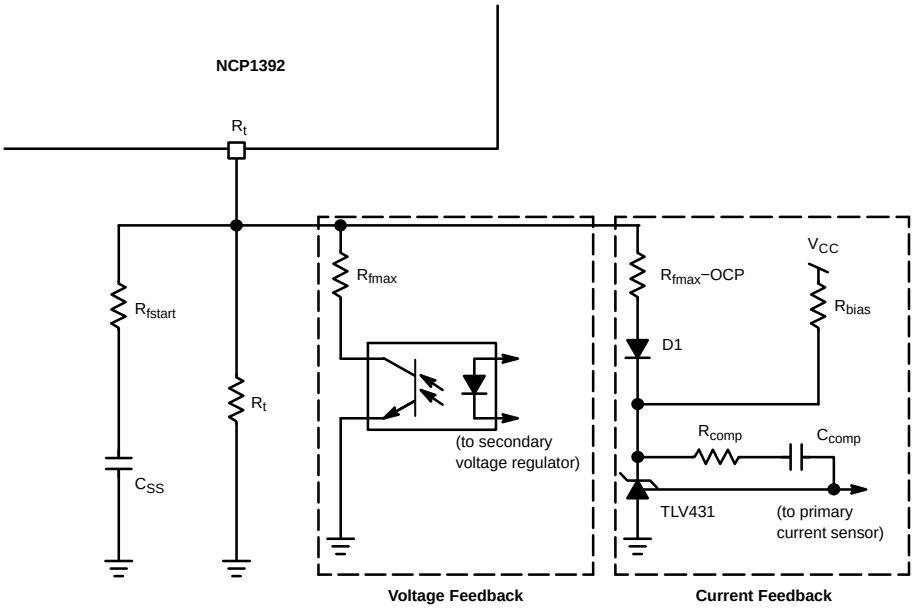


Figure 29. Typical Rt Pin Connection

The minimum switching frequency is given by the Rt resistor value. This frequency is reached if there is no optocoupler or current feedback action and soft start period has been already finished. The maximum switching frequency excursion is limited by the Rf_{max} selection. Note that the F_{max} value is influenced by the optocoupler saturation voltage value. Resistor Rfstart together with capacitor C_{SS} prepares the soft start period after PFC timer elapses. The Rt pin is grounded via an internal switch during the PFC delay period to assure that the soft start capacitor will be fully discharged via Rfstart resistor.

There is a possibility to connect other control loops (like current control loop) to the Rt pin. The only one limitation lies in the Rt pin reference voltage which is $Vref_{Rt}$ = 3.5 V. Used regulator has to be capable to work with voltage lower than $Vref_{Rt}$.

The TLV431 shunt regulator is used in the example from figure 4 to prepare current feedback loop. Diode D1 is used to enable regulator biasing via resistor Rbias. Total saturation voltage of this solution is 1.25 + 0.6 = 1.85 V for room temperature. Shottky diode will further decrease saturation voltage. Rf_{max} − OCP resistor value, limits the maximum frequency that can be pushed by this regulation loop. This parameter is not temperature stable because of the D1 temperature drift.

Brown−Out Protection

The Brown−Out circuitry (BO) offers a way to protect the application from low DC input voltages. Below a given level, the controller blocks the output pulses, above it, it authorizes them. The internal circuitry, depicted by Figure 30, offers a way to observe the high−voltage (HV) rail.

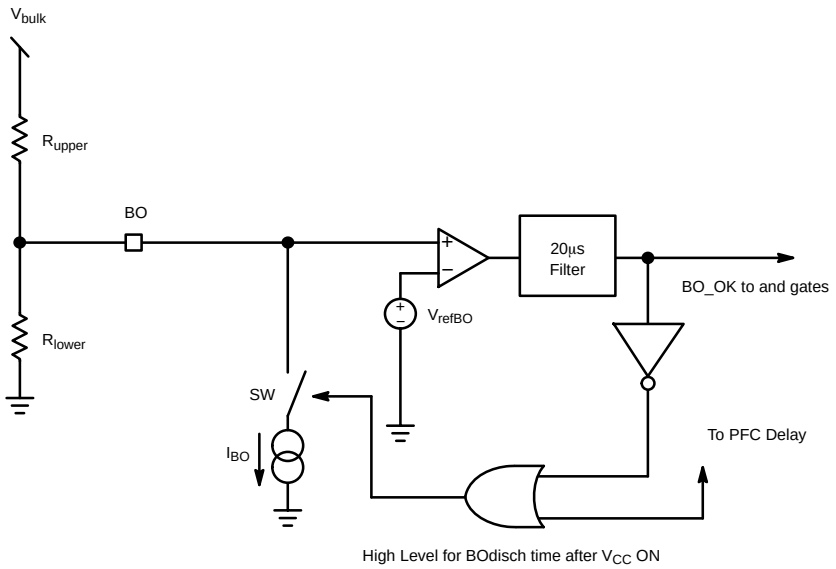


Figure 30. The internal Brown−Out Configuration with an Offset Current Sink

A resistive divider made of R_{upper} and R_{lower}, brings a portion of the HV rail on Pin 3. Below the turn−on level, the 18.2 μA current sink (IBO) is on. Therefore, the turn−on level is higher than the level given by the division ratio brought by the resistive divider. To the contrary, when the internal BO_OK signal is high (PFC timer runs or Mlower and Mupper pulse), the I_{BO} sink is deactivated. As a result, it becomes possible to select the turn−on and turn−off levels via a few lines of algebra:

IBO is on

$$Vref_{BO} = V_{bulk1} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} - I_{BO} \cdot \left(\frac{R_{lower} \cdot R_{upper}}{R_{lower} + R_{upper}} \right) \quad \text{(eq. 1)}$$

IBO is off

$$Vref_{BO} = V_{bulk2} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} \quad \text{(eq. 2)}$$

We can extract R_{lower} from Equation 2 and plug it into Equation 1, then solve for R_{upper}:

$$R_{lower} = Vref_{BO} \cdot \frac{V_{bulk1} - V_{bulk2}}{I_{BO} \cdot \left(V_{bulk2} - Vref_{BO}\right)} \quad \text{(eq. 3)}$$

$$R_{upper} = R_{lower} \cdot \frac{V_{bulk2} - Vref_{BO}}{Vref_{BO}} \quad \text{(eq. 4)}$$

If we decide to turn−on our converter for V_{bulk1} equals 350 V and turn it off for V_{bulk2} equals 250 V, then for I_{BO} = 18.2 μA and $Vref_{BO}$ = 1.0 V we obtain:

R_{upper} = 5.494 MΩ

R_{lower} = 22.066 kΩ

The bridge power dissipation is 400^2 / 5.517 MΩ = 29 mW when front−end PFC stage delivers 400 V. Figure 31 simulation result confirms our calculations.

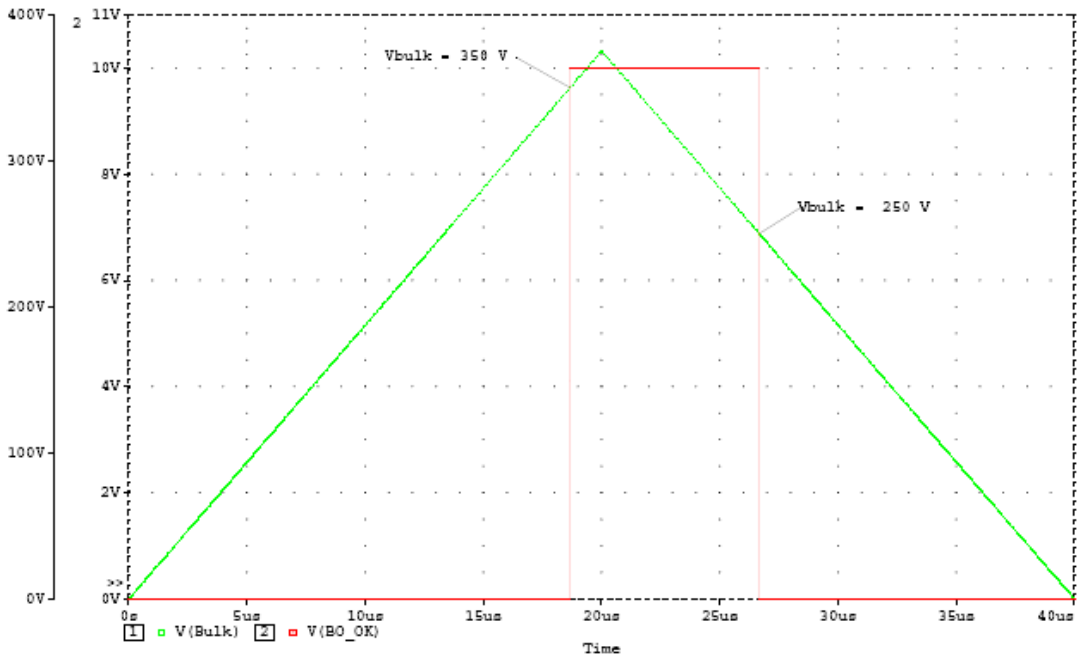


Figure 31. Simulation Results for 350/250 ON/OFF Brown−Out Levels

The IBO current sink is turned ON for BOdisch time after any controller restart to let the BO input voltage stabilize (there can be connected big capacitor to the BO input and the IBO is only 18.2 μA so it will take some time to discharge). Once the BOdisch time one shoot pulse ends the BO comparator is supposed to either hold the I_{BO} sink turned ON (if the bulk voltage level is not sufficient) or let it turned OFF (if the bulk voltage is higher than V_{bulk1}).

See Figures 10 − 13 for better understanding on how the BO input works.

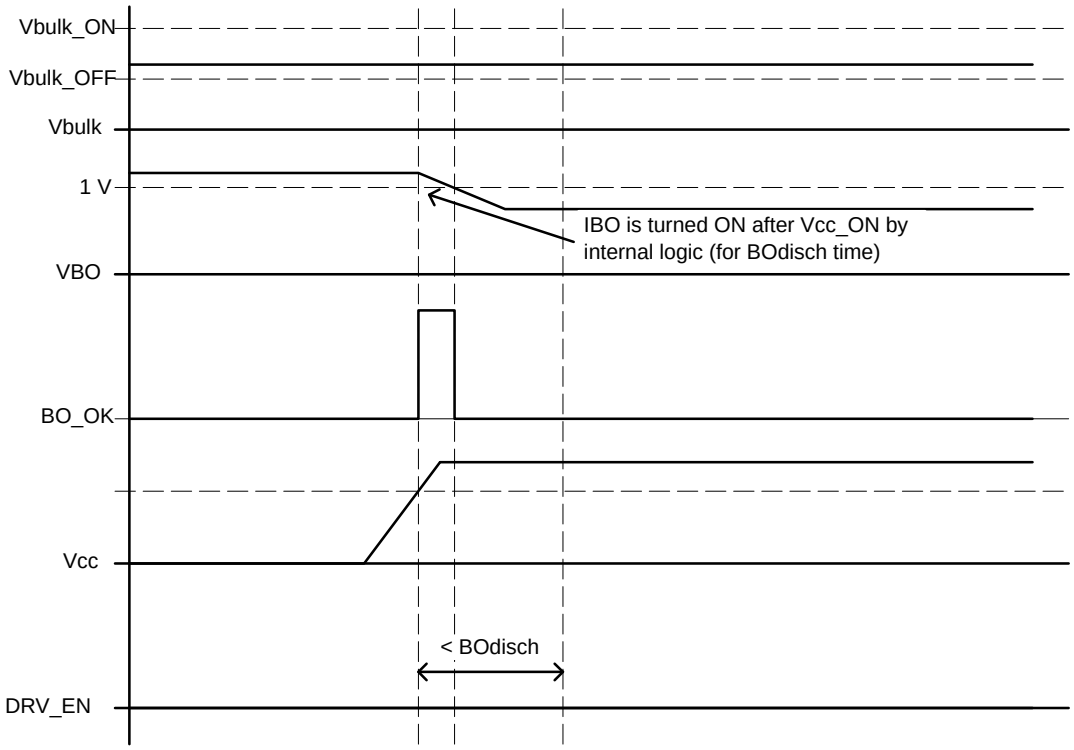


Figure 32. BO Input Functionality − V_{bulk2} < V_{bulk} < V_{bulk1}

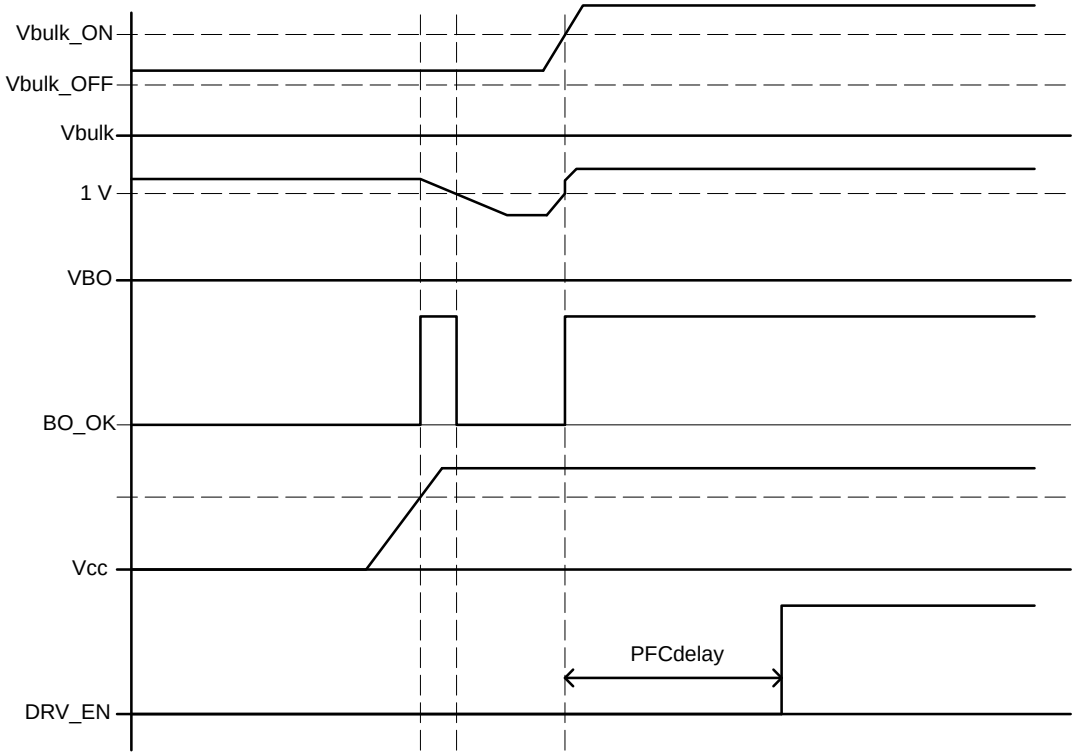


Figure 33. BO Input Functionality $-V_{bulk2} < V_{bulk} < V_{bulk1}$, PFC Start Follows

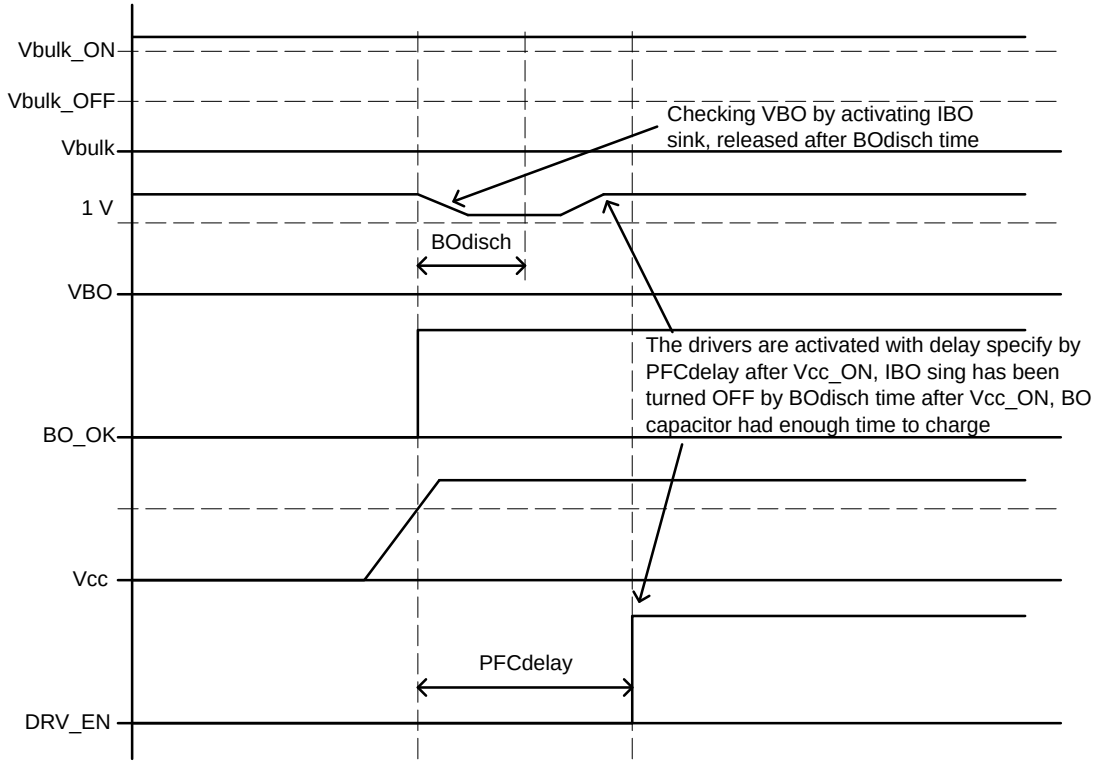


Figure 34. BO Input Functionality − $V_{bulk} > V_{bulk1}$

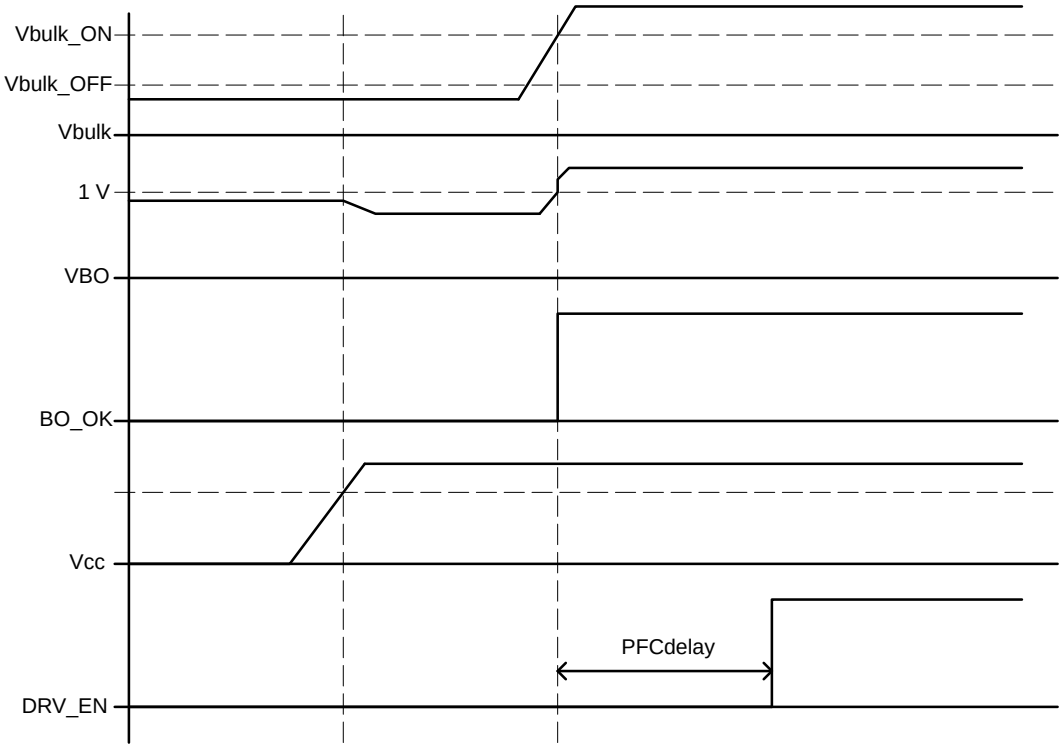


Figure 35. BO Input Functionality − $V_{bulk} < V_{bulk2}$, PFC Start Follows

Non−Latched Enable Input (B Version only)

The non−latched input stops output drivers immediately the BO terminal voltage grows above 2 V threshold. The enable comparator features 100 mV hysteresis so the BO terminal has to go down below 1.9 V to recover IC operation. This input offers other features to the NCP1392 like dimming function for lamp ballasts (Figure 36) or skip mode capability for resonant converters (Figures 37 and 39).

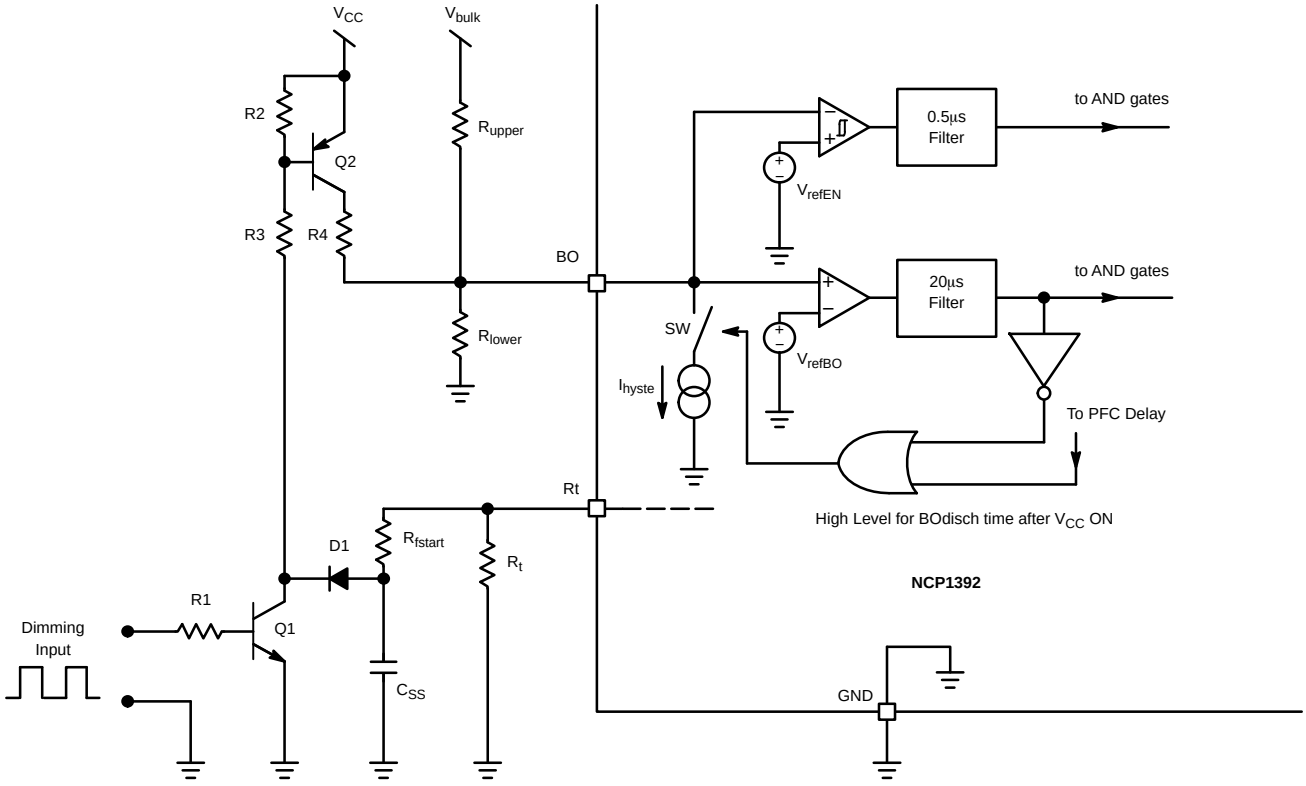


Figure 36. Dimming Feature Implementation Using Nonlatched Input on BO Terminal

The dimming feature can be easily aid to the ballast application by adding two bipolar transistors (Figure 14). Transistor Q2 pullup BO input when dimming signal is high. In the same time the Q1 discharges soft start capacitor via diode D1. Ballast application is enabled (including soft−start phase) when dimming signal becomes low again.

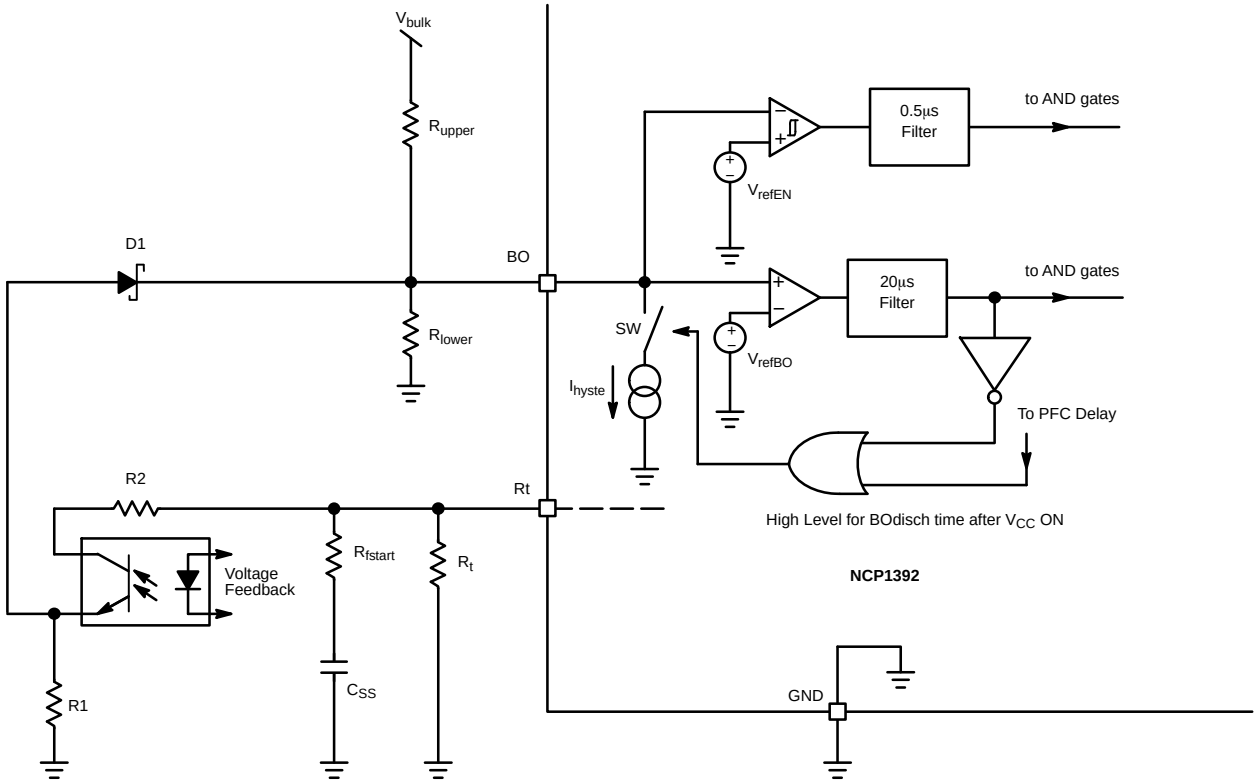


Figure 37. Skip Mode Feature Implementation (Temperature Dependent, Cost Effective)

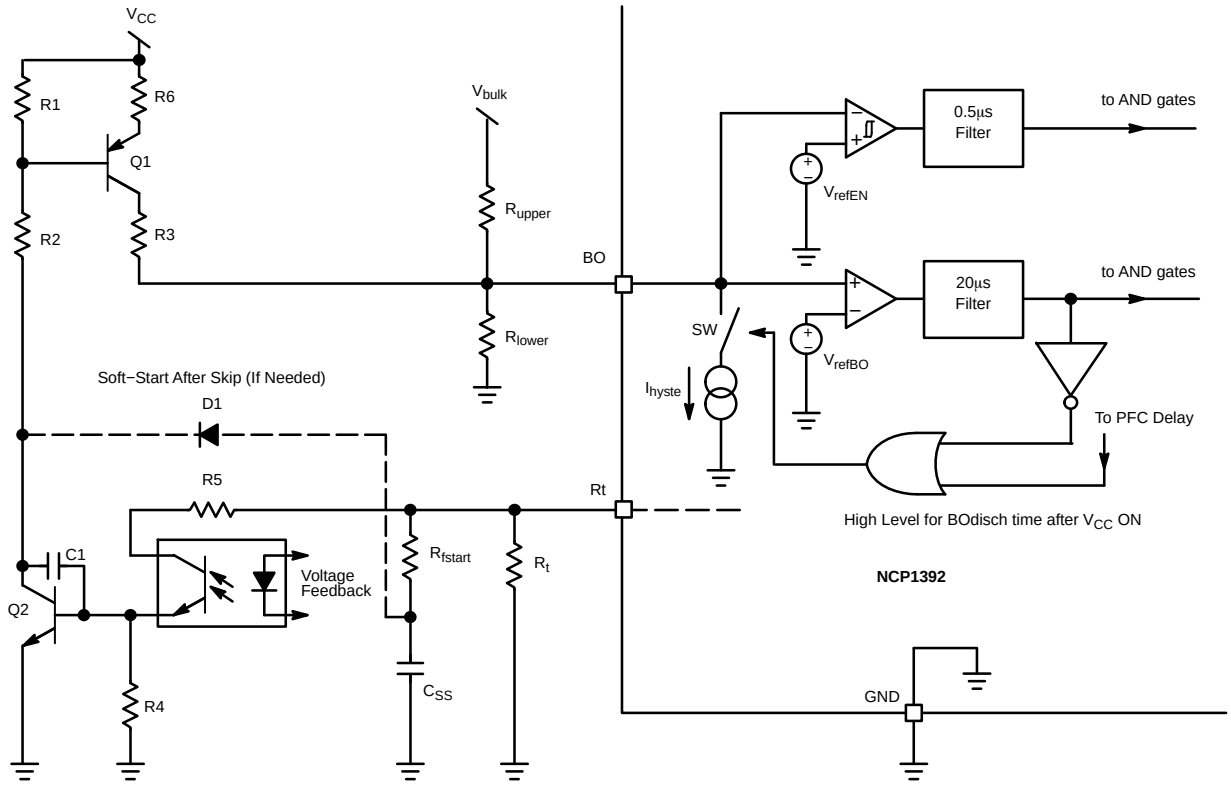


Figure 38. Skip Mode with Transistor Feature Implementation (Temperature Dependent, Cost Effective)

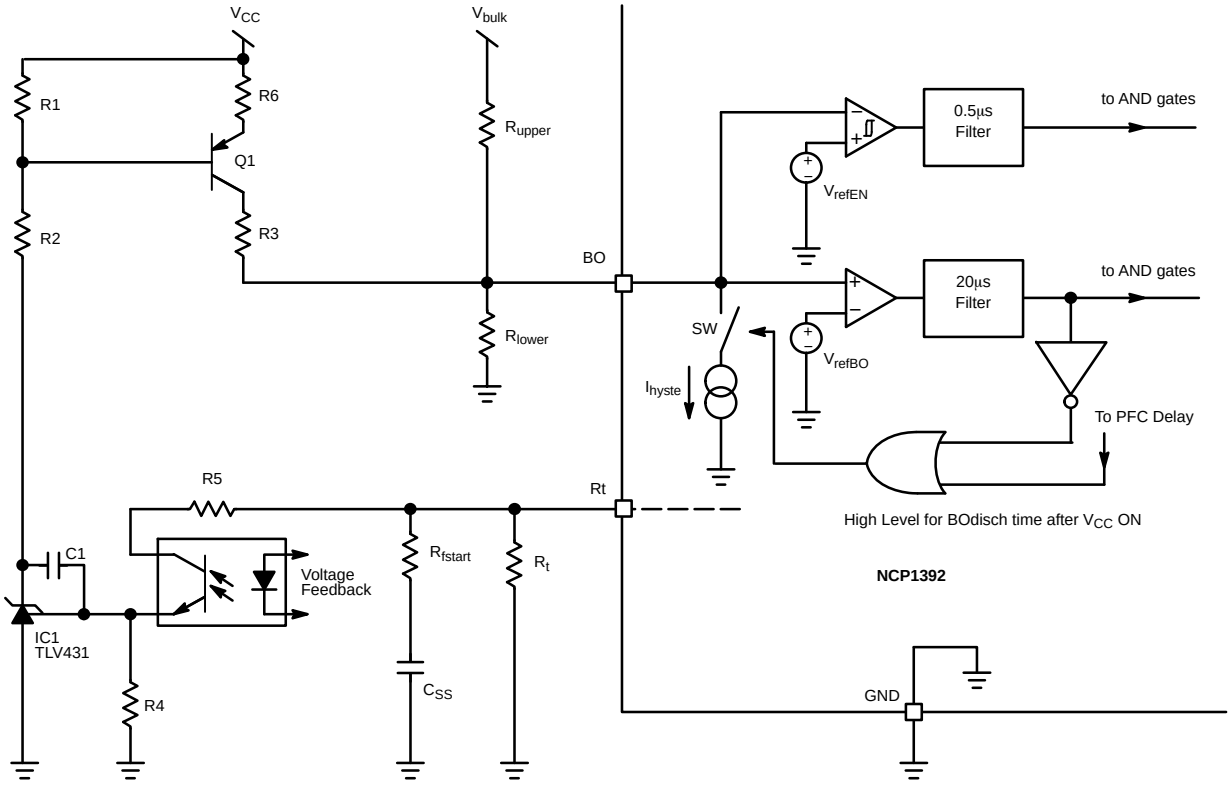


Figure 39. Skip Mode Feature Implementation (Better Accuracy)

Figures 37 and 39 shows skip mode feature implementation using NCP1392 driver. Voltage across resistor R1 (R4) increases when converter enters light load conditions. The enable comparator is triggered when voltage across R1 is higher than Vref EN + Vf(D1) for connection from Figure 37 (voltage across R4 is higher than 1.24 V for connection from figure 16). IC then prevents outputs from pulsing until BO terminal voltage decreases below 1.92 V.

Note that enable comparator serves also as an automatic overvoltage protection. When bulk voltage is too high, the enable input is triggered via BO divider.

Following equations can be used for easy calculations of devices connected to Rt pin:

Minimum frequency:

$$R_t = \frac{3.5 \cdot k}{Frequency - q} \quad \text{(eq. 5)}$$

Maximum frequency where soft−start begins:

$$R_{fstart} = \frac{3.5 \cdot k \cdot R_t}{Frequency \cdot R_t - R_t \cdot q - 3.5 \cdot k} \quad \text{(eq. 6)}$$

The soft−start duration is set by Css capacitor:

$$C_{SS} = \frac{SS_{duration}}{R_{fstart} \cdot 5} \quad \text{(eq. 7)}$$

A resistor to set maximum frequency, if the optocoupler is fully conductive is calculated by the following equation:

$$R_{(R4+R5)} = -\frac{\left(-3.5 + V_{ce\_sat}\right) \cdot k \cdot R_t}{Frequency \cdot R_t - R_t \cdot q - 3.5 \cdot k + k \cdot V_{ce\_sat}} \quad \text{(eq. 8)}$$

The constants in the equations are as follows:

Version B: $k = 244.4 \cdot 10^6$, $q = 0.555 \cdot 10^3$

Version D: $k = 478.9 \cdot 10^6$, $q = 1.053 \cdot 10^3$

The High−Voltage Driver

Figure 40 shows the internal architecture of the high−voltage section. The device incorporates an upper UVLO circuitry that makes sure enough V_{gs} is available for the upper side MOSFET. The V_{CC} for floating driver section is provided by C_{boot} capacitor that is refilled by external bootstrap diode.

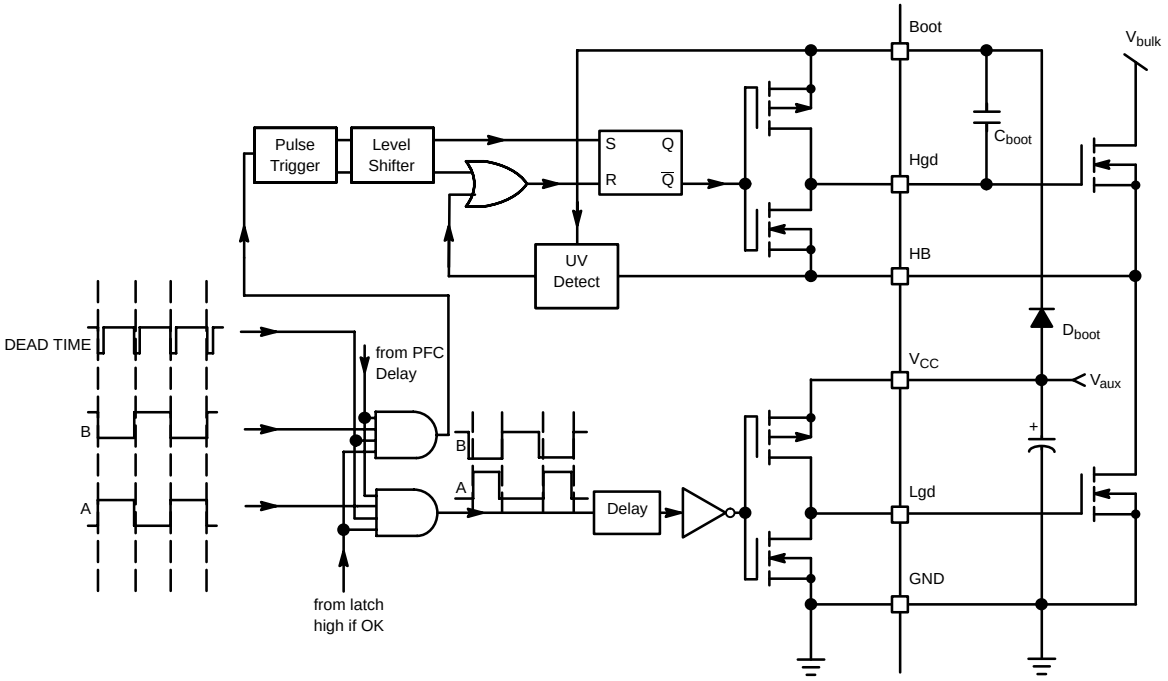


Figure 40. The Internal High−Voltage Section of the NCP1392

The A and B outputs are delivered by the internal logic, as depicted in block diagram. This logic is constructed in such a way that the Mlower driver starts to pulse firs after any driver restart. The bootstrap capacitor is thus charged during first pulse. A delay is inserted in the lower rail to ensure good matching between these propagating signals. As stated in the maximum rating section, the floating portion can go up to 600 Vdc and makes the IC perfectly suitable for offline applications featuring a 400 V PFC front−end stage.

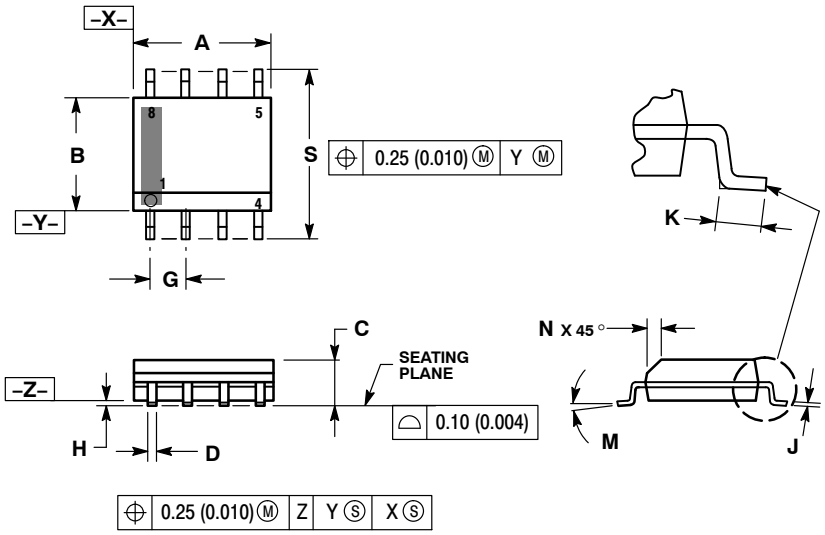
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

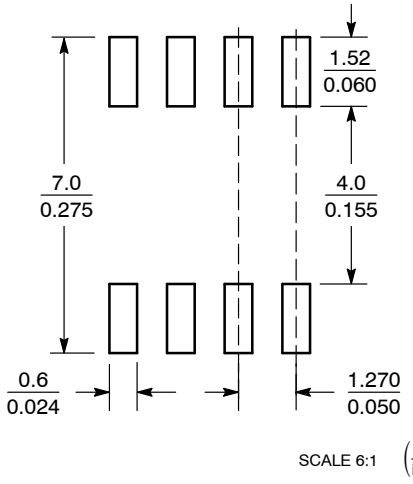
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

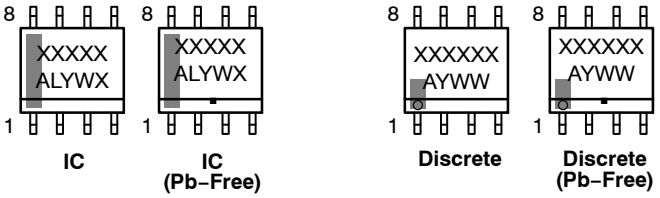
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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