MJH11017, MJH11019, MJH11021 (PNP) MJH11018, MJH11020, MJH11022 (NPN)

Complementary Darlington Silicon Power Transistors

These devices are designed for use as general purpose amplifiers, low frequency switching and motor control applications.

Features

- High DC Current Gain @ 10 Adc — h_{FE} = 400 Min (All Types)
- Collector−Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 150 Vdc (Min) — MJH11018, 17
  = 200 Vdc (Min) — MJH11020, 19
  = 250 Vdc (Min) — MJH11022, 21
- Low Collector−Emitter Saturation Voltage
  $V_{CE(sat)}$ = 1.2 V (Typ) @ I_C = 5.0 A
  = 1.8 V (Typ) @ I_C = 10 A
- Monolithic Construction
- These are Pb−Free Devices

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage MJH11018, MJH11017 MJH11020, MJH11019 MJH11022, MJH11021	V_{CEO}	 150 200 250	Vdc
Collector−Base Voltage MJH11018, MJH11017 MJH11020, MJH11019 MJH11022, MJH11021	V_{CB}	 150 200 250	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C	15 30	Adc
Base Current	I_B	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.83	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

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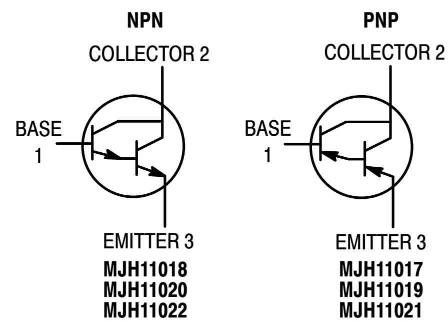
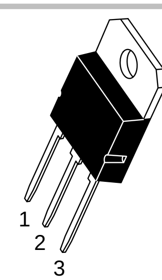
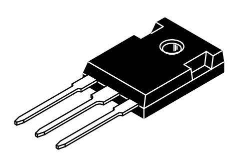
15 AMPERE DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS 150−250 VOLTS, 150 WATTS





SOT−93 (TO−218) CASE 340D STYLE 1



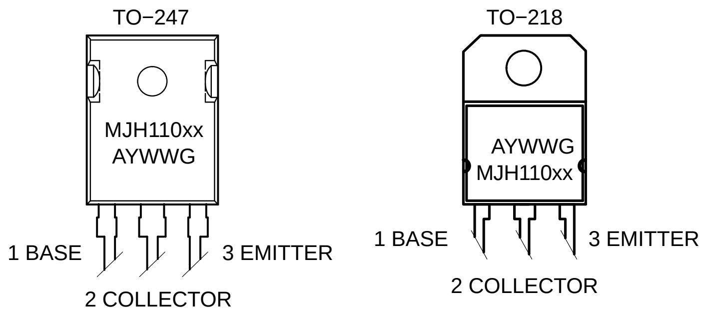
TO−247 CASE 340L STYLE 3

NOTE: Effective June 2012 this device will be available only in the TO−247 package. Reference FPCN# 16827.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MARKING DIAGRAMS



A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package
MJH110xx = Device Code
xx = 17, 19, 21, 18, 20, 22

ORDERING INFORMATION

Device Order Number	Package Type	Shipping
MJH11017G	TO−218 (Pb−Free)	30 Units / Rail
MJH11018G	TO−218 (Pb−Free)	30 Units / Rail
MJH11019G	TO−218 (Pb−Free)	30 Units / Rail
MJH11020G	TO−218 (Pb−Free)	30 Units / Rail
MJH11021G	TO−218 (Pb−Free)	30 Units / Rail
MJH11022G	TO−218 (Pb−Free)	30 Units / Rail
MJH11017G	TO−247 (Pb−Free)	30 Units / Rail
MJH11018G	TO−247 (Pb−Free)	30 Units / Rail
MJH11019G	TO−247 (Pb−Free)	30 Units / Rail
MJH11020G	TO−247 (Pb−Free)	30 Units / Rail
MJH11021G	TO−247 (Pb−Free)	30 Units / Rail
MJH11022G	TO−247 (Pb−Free)	30 Units / Rail

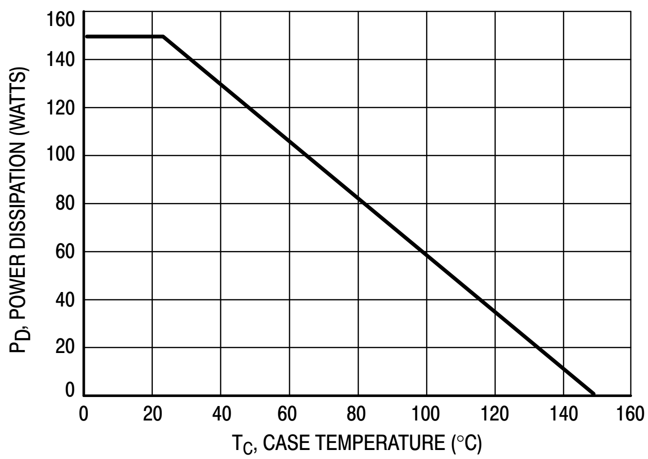


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 2) (I_C = 0.1 Adc, I_B = 0)	 MJH11017, MJH11018 MJH11019, MJH11020 MJH11021, MJH11022	$V_{CEO(sus)}$	 150 200 250	 – – –	Vdc
Collector Cutoff Current (V_{CE} = 75 Vdc, I_B = 0) (V_{CE} = 100 Vdc, I_B = 0) (V_{CE} = 125 Vdc, I_B = 0)	 MJH11017, MJH11018 MJH11019, MJH11020 MJH11021, MJH11022	I_{CEO}	 – – –	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_J = 150°C)		I_{CEV}	 – –	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (Note 2)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 15 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	 400 100	 15,000 –	–
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 100 mA) (I_C = 15 Adc, I_B = 150 mA)		$V_{CE(sat)}$	 – –	 2.5 4.0	Vdc
Base−Emitter On Voltage (I_C = 10 A, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
Base−Emitter Saturation Voltage (I_C = 15 Adc, I_B = 150 mA)		$V_{BE(sat)}$	–	3.8	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain Bandwidth Product (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		f_T	3.0	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJH11018, MJH11020, MJH11022 MJH11017, MJH11019, MJH11021	C_{ob}	– –	400 600	pF
Small−Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	75	–	–

SWITCHING CHARACTERISTICS

Characteristic		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	(V_{CC} = 100 V, I_C = 10 A, I_B = 100 mA $V_{BE(off)}$ = 5.0 V) (See Figure 2)	t_d	150	75	ns
Rise Time		t_r	1.2	0.5	µs
Storage Time		t_s	4.4	2.7	µs
Fall Time		t_f	2.5	2.5	µs

2. Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2.0%.

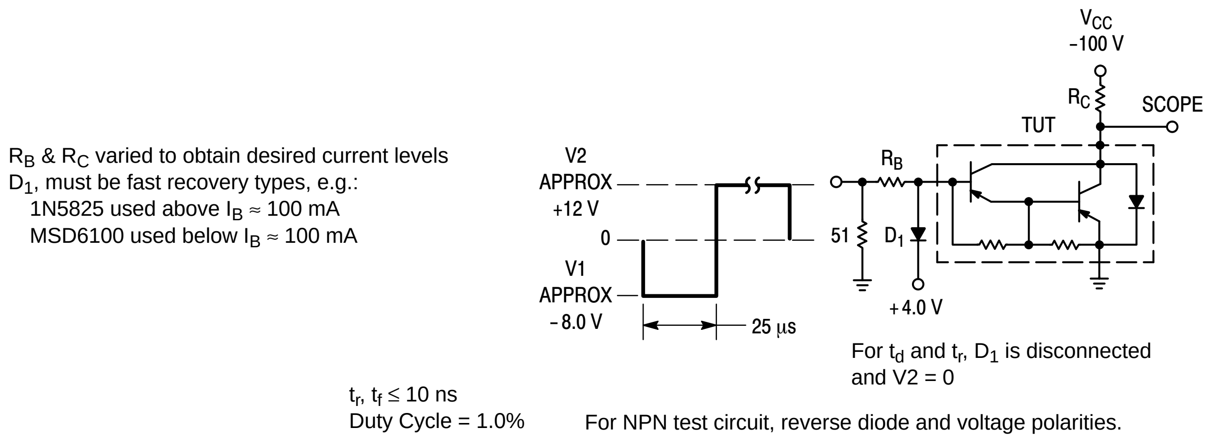


Figure 2. Switching Times Test Circuit

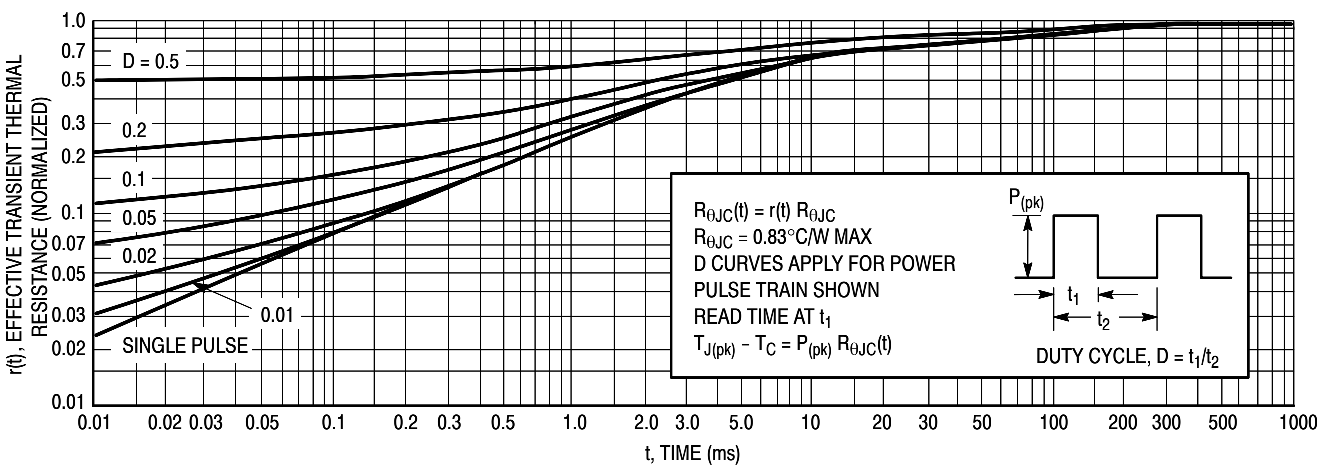


Figure 3. Thermal Response

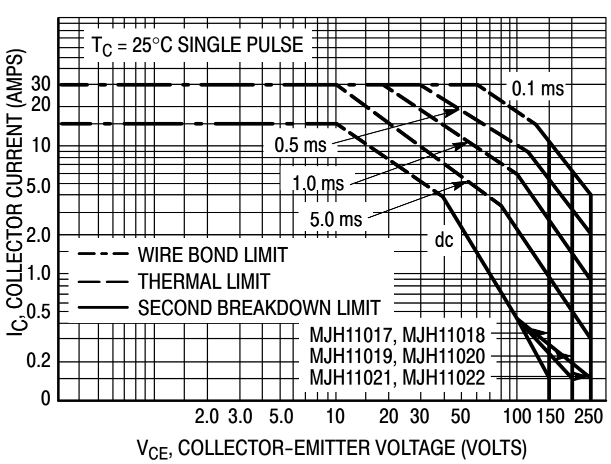


Figure 4. Maximum Rated Forward Bias Safe Operating Area (FBSOA)

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

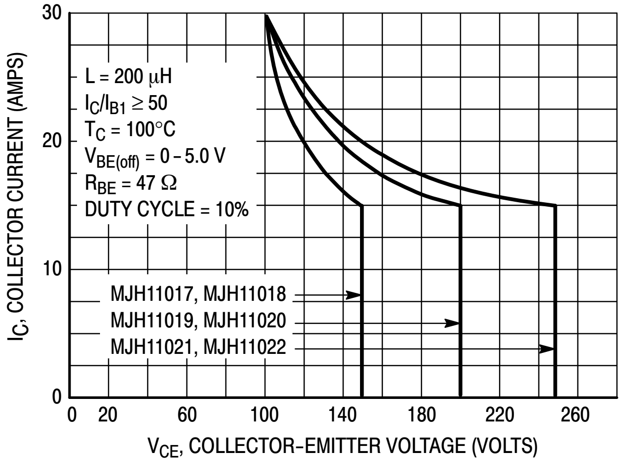
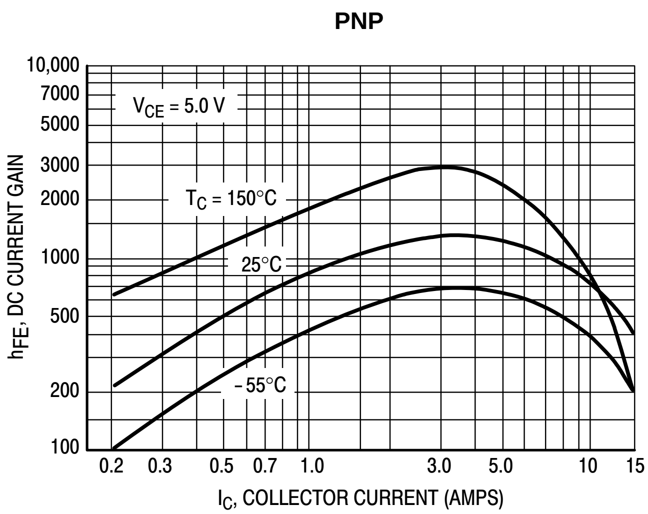


Figure 5. Maximum Rated Reverse Bias Safe Operating Area (RBSOA)

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives RBSOA characteristics.



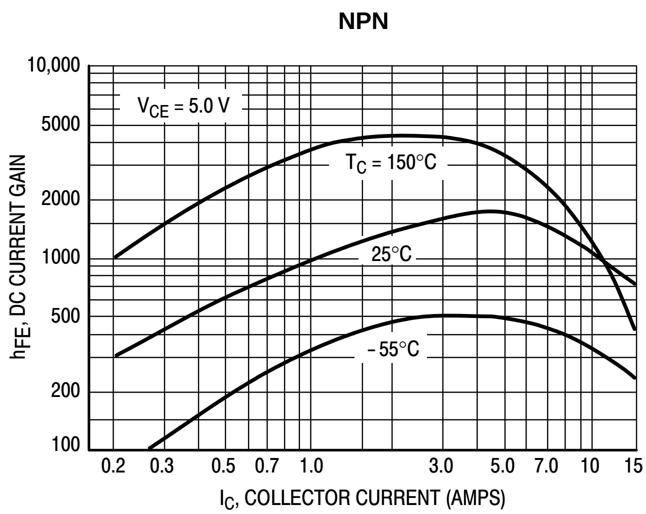
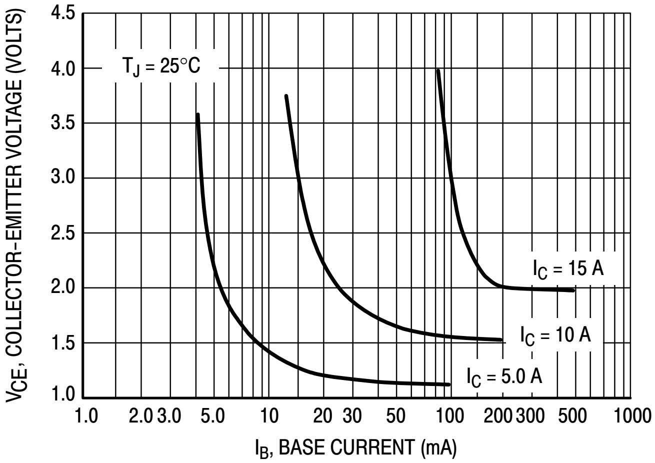


Figure 6. DC Current Gain

PNP



NPN

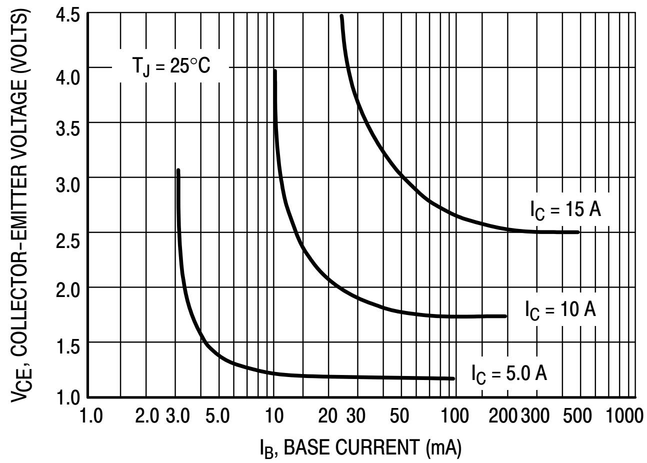
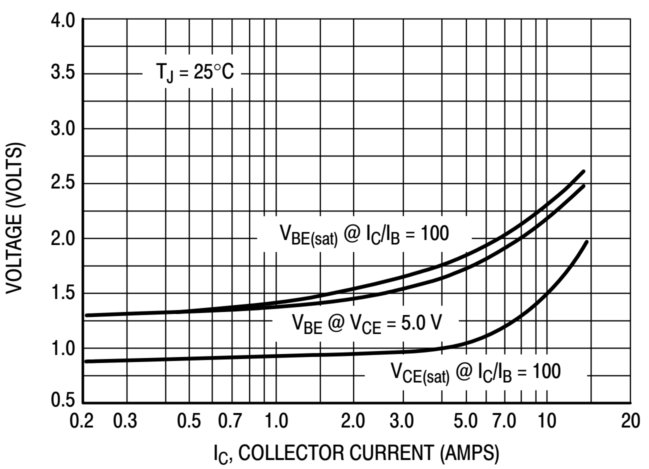


Figure 7. Collector Saturation Region

PNP



NPN

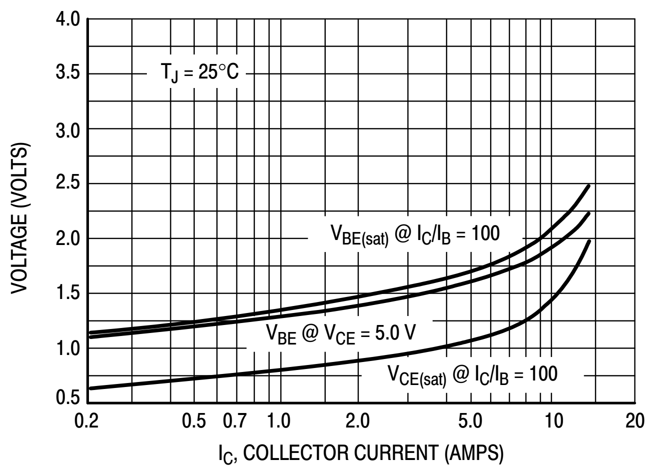
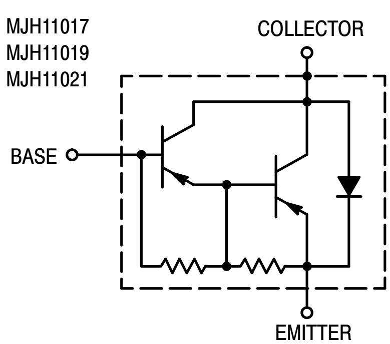


Figure 8. "On" Voltages

PNP



NPN

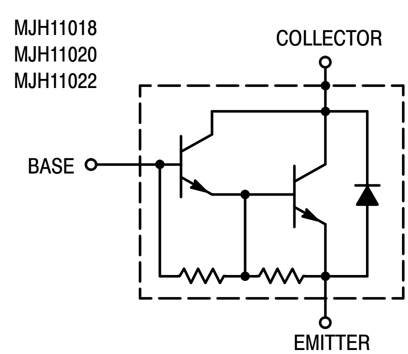
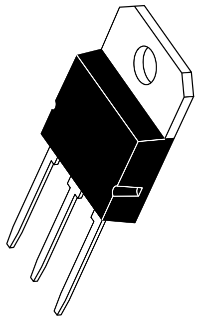


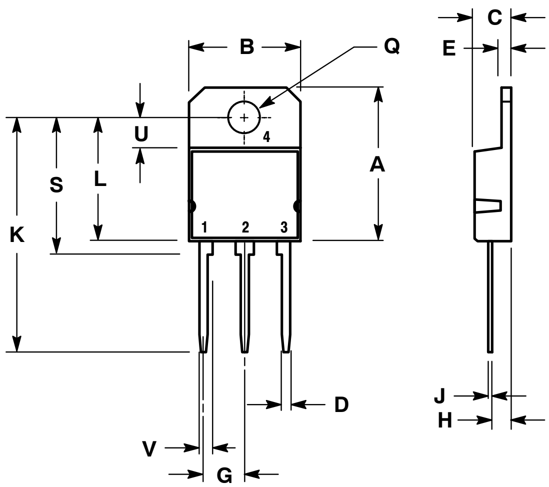
Figure 9. Darlington Schematic



SOT−93 (TO−218)
CASE 340D−02
ISSUE E

DATE 01/03/2002

SCALE 1:1



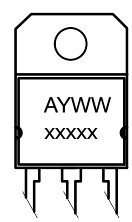
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	---	20.35	---	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	---	16.20	---	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
xxxxx = Device Code

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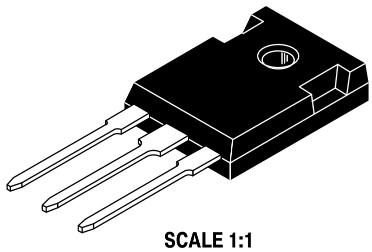
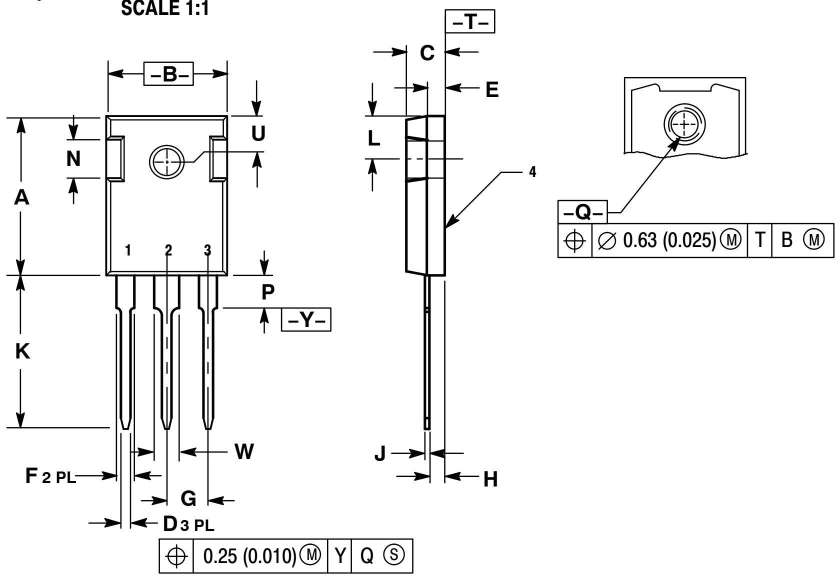
DESCRIPTION:	SOT−93	PAGE 1 OF 1



SCALE 1:1

TO−247
CASE 340L−02
ISSUE F

DATE 26 OCT 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	8.30
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	---	4.50	---	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)

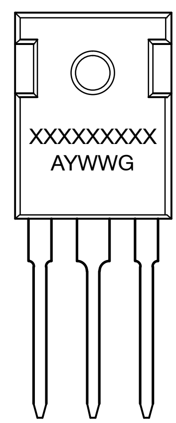
STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 6:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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STATUS:	**ON SEMICONDUCTOR STANDARD**	
NEW STANDARD:		
DESCRIPTION:	**TO−247**	**PAGE 1 OF 2**

ISSUE	REVISION	DATE
D	CHANGE OF OWNERSHIP FROM MOTOROLA TO ON SEMICONDUCTOR. DIM A WAS 20.80−21.46/0.819−0.845. DIM K WAS 19.81−20.32/0.780−0.800. UPDATED STYLE 1, ADDED STYLES 2, 3, & 4. REQ. BY L. HAYES.	25 AUG 2000
E	DIM E MINIMUM WAS 2.20/0.087. DIM K MINIMUM WAS 20.06/0.790. ADDED GENERIC MARKING DIAGRAM. REQ. BY S. ALLEN.	26 FEB 2010
F	ADDED STYLES 5 AND 6. REQ. BY J. PEREZ.	26 OCT 2011

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