MC14543B

BCD-to-Seven Segment Latch/Decoder/Driver for Liquid Crystals

The MC14543B BCD−to−seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4−bit storage latch and an 8421 BCD−to−seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light−emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

Features

- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving 2 Low−power TTL Loads, 1 Low−power Schottky TTL Load or 2 HTL Loads Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4056A (with Pin 7 Tied to V_{SS}).
- Chip Complexity: 207 FETs or 52 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.
- This Device is Pb−Free and is RoHS Compliant

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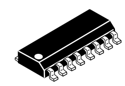
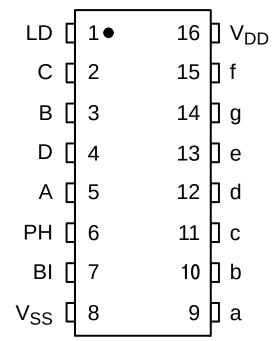


SOIC−16
D SUFFIX
CASE 751B

PIN ASSIGNMENT



MARKING DIAGRAM

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input Voltage Range, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	V
DC Input Current per Pin	I_{in}	±10	mA
Power Dissipation per Package (Note 1)	P_D	500	mW
Operating Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Maximum Continuous Output Drive Current (Source or Sink)	I_{OHmax} I_{OLmax}	10 (per Output)	mA
Maximum Continuous Output Power (Source or Sink) (Note 2)	P_{OHmax} P_{OLmax}	70 (per Output)	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Package: –7.0 mW/°C From 65°C To 125°C
2. $P_{OHmax} = I_{OH} (V_{OH} - V_{DD})$ and $P_{OLmax} = I_{OL} (V_{OL} - V_{SS})$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

TRUTH TABLE

Inputs							Outputs							
LD	**BI**	**Ph***	**D**	**C**	**B**	**A**	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**Display**
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	†	†				Inverse of Output Combinations Above							Display as above

X = Don’t care

† = Above Combinations

* = For liquid crystal readouts, apply a square wave to Ph
For common cathode LED readouts, select Ph = 0
For common anode LED readouts, select Ph = 1

** = Depends upon the BCD code previously applied when LD = 1

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 3)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	−	0.05	−	0	0.05	−	0.05	Vdc
		10	−	0.05	−	0	0.05	−	0.05	
		15	−	0.05	−	0	0.05	−	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	−	4.95	5.0	−	4.95	−	Vdc
		10	9.95	−	9.95	10	−	9.95	−	
		15	14.95	−	14.95	15	−	14.95	−	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	−	1.5	−	2.25	1.5	−	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	−	3.0	−	4.50	3.0	−	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	−	4.0	−	6.75	4.0	−	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	−	3.5	2.75	−	3.5	−	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	−	7.0	5.50	−	7.0	−	
(V_O = 1.5 or 13.5 Vdc)		15	11	−	11	8.25	−	11	−	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–3.0	−	–2.4	–4.2	−	–1.7	−	
(V_{OH} = 4.6 Vdc)		5.0	–0.64	−	–0.51	–0.88	−	–0.36	−	
(V_{OH} = 0.5 Vdc)		10	−	−	−	–10.1	−	−	−	
(V_{OH} = 9.5 Vdc)		10	–1.6	−	–1.3	–2.25	−	–0.9	−	
(V_{OH} = 13.5 Vdc)		15	–4.2	−	–3.4	–8.8	−	–2.4		
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	−	0.51	0.88	−	0.36	−	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	−	1.3	2.25	−	0.9	−	
(V_{OL} = 9.5 Vdc)		10	−	−	−	10.1	−	−	−	
(V_{OL} = 1.5 Vdc)		15	4.2	−	3.4	8.8	−	2.4		
Input Current	I_{in}	15	−	±0.1	−	±0.00001	±0.1	−	±1.0	μAdc
Input Capacitance	C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (Per Package) V_{in} = 0 or V_{DD}, I_{out} = 0 μA	I_{DD}	5.0	−	5.0	−	0.005	5.0	−	150	μAdc
		10	−	10	−	0.010	10	−	300	
		15	−	20	−	0.015	20	−	600	
Total Supply Current (Note 4, 5) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.6 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.1 μA/kHz) f + I_{DD}							
		15	I_T = (4.7 μA/kHz) f + I_{DD}							

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Noise immunity specified for worst−case input combination.

   Noise Margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
   2.0 V min @ V_{DD} = 10 V
   2.5 V min @ V_{DD} = 15 V

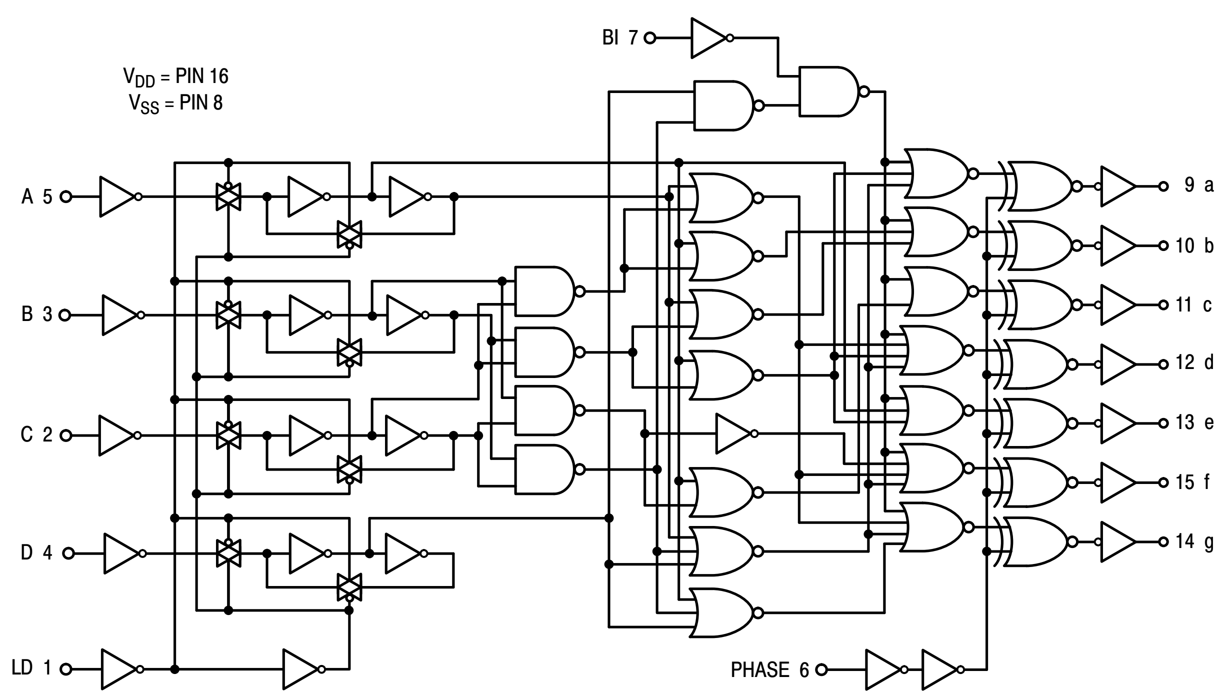
4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD}f$ where: I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.
5. The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (Note 6) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Turn−Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 520 ns		5.0	–	605	1210	
t_{PLH} = (0.66 ns/pF) C_L + 217 ns		10	–	250	500	
t_{PLH} = (0.5 ns/pF) C_L + 160 ns		15	–	185	370	
Turn−On Delay Time	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 420 ns		5.0	–	505	1650	
t_{PHL} = (0.66 ns/pF) C_L + 172 ns		10	–	205	660	
t_{PHL} = (0.5 ns/pF) C_L + 130 ns		15	–	155	495	
Setup Time	t_{su}	5.0	350		–	ns
		10	450		–	
		15	500		–	
Hold Time	t_h	5.0	40		–	ns
		10	30		–	
		15	20		–	
Latch Disable Pulse Width (Strobing Data)	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	

6. The formulas given are for the typical characteristics only.

LOGIC DIAGRAM



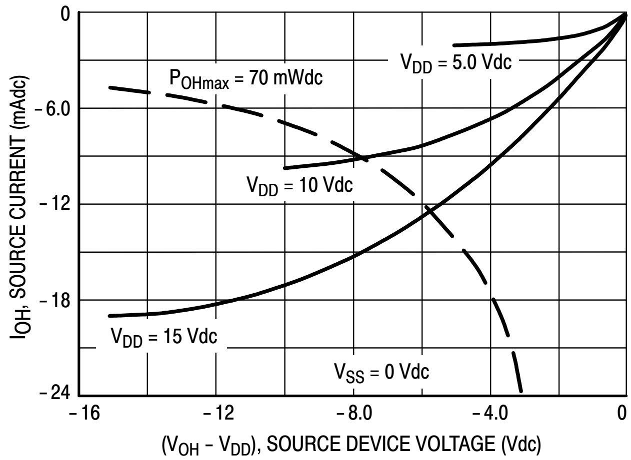


Figure 1. Typical Output Source Characteristics

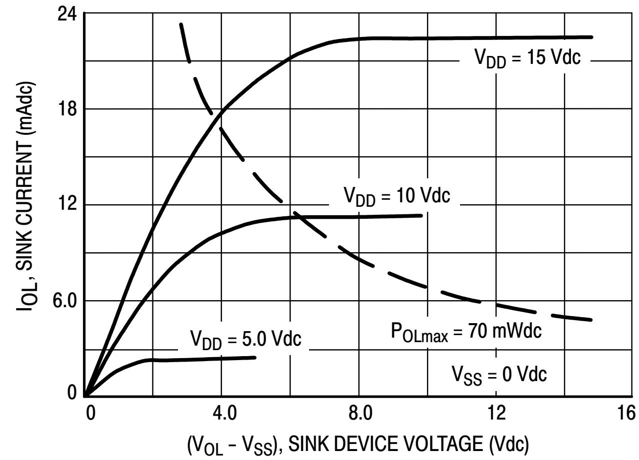


Figure 2. Typical Output Sink Characteristics

Inputs BI and Ph low, and Inputs D and LD high.
f in respect to a system clock.

All outputs connected to respective C_L loads.

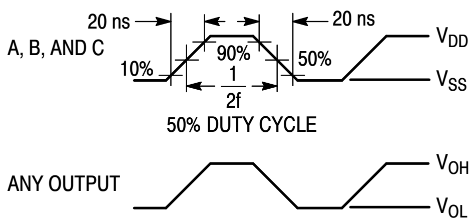
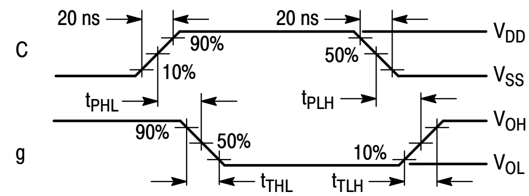
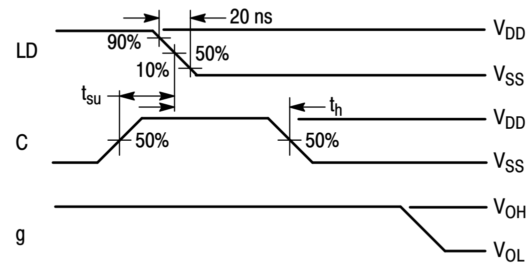


Figure 3. Dynamic Power Dissipation Signal Waveforms

(a) Inputs D, Ph, and BI low, and Inputs A, B, and LD high.



(b) Inputs D, Ph, and BI low, and Inputs A and B high.



(c) Data DCBA strobed into latches

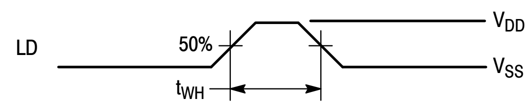
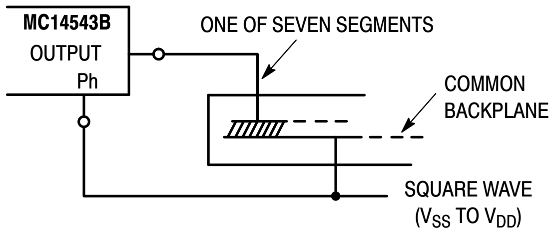


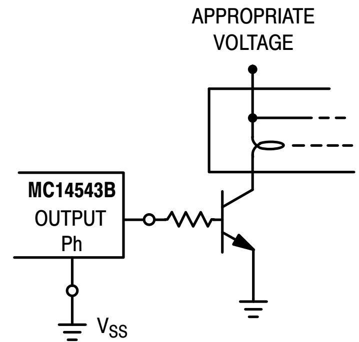
Figure 4. Dynamic Signal Waveforms

CONNECTIONS TO VARIOUS DISPLAY READOUTS

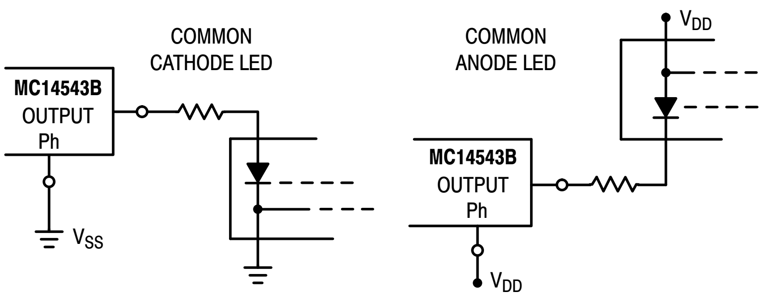
LIQUID CRYSTAL (LC) READOUT



INCANDESCENT READOUT

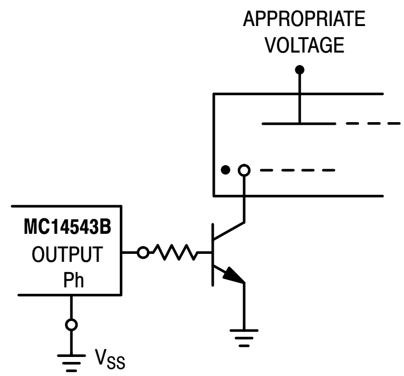


LIGHT EMITTING DIODE (LED) READOUT

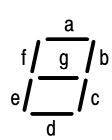


NOTE: Bipolar transistors may be added for gain (for $V_{DD} \leq 10$ V or $I_{out} \geq 10$ mA).

GAS DISCHARGE READOUT

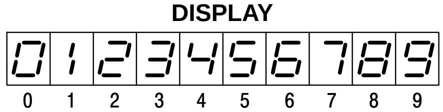


CONNECTIONS TO SEGMENTS



V_{DD} = PIN 16
V_{SS} = PIN 8

DISPLAY

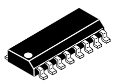


ORDERING INFORMATION

Device	Package	Shipping†
MC14543BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14543BDR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
NLV14543BDR2G*	SOIC−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

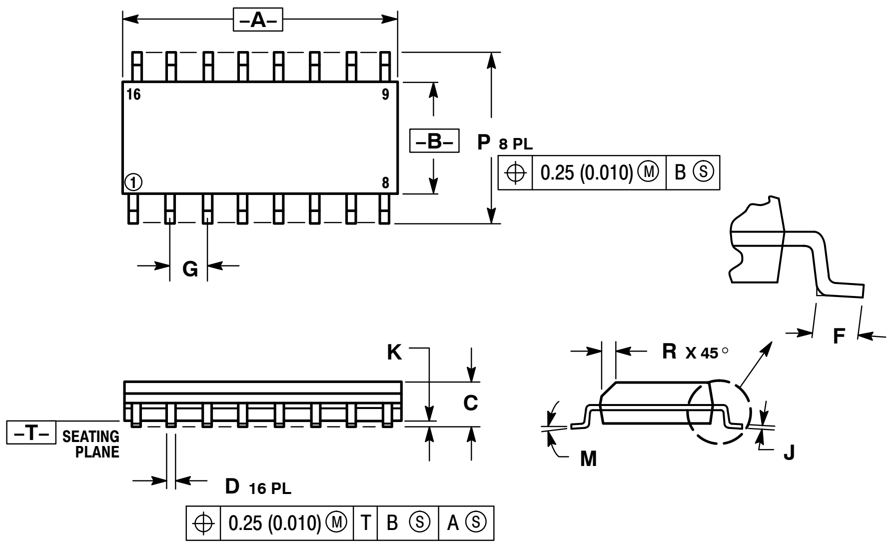


SCALE 1:1

SOIC−16

CASE 751B−05
ISSUE K

DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

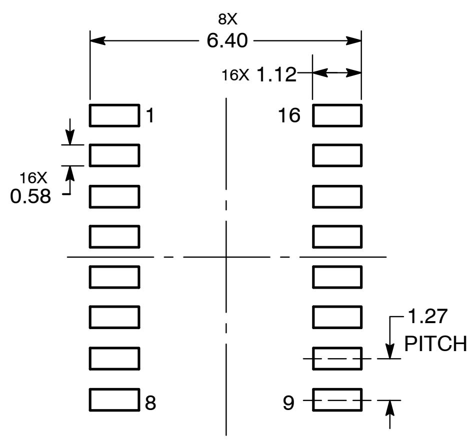
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	**SOIC−16**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
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