MC100EPT22

3.3 V Dual LVTTL/LVCMOS to Differential LVPECL Translator

ON Semiconductor®

Description

The MC100EPT22 is a dual LVTTL/LVCMOS to differential LVPECL translator. Because LVPECL (Positive ECL) levels are used only +3.3 V and ground are required. The small outline 8–lead package and the single gate of the EPT22 makes it ideal for those applications where space, performance, and low power are at a premium. Because the mature MOSAIC 5 process is used, low cost and high speed can be added to the list of features.

Features

- 420 ps Typical Propagation Delay
- Maximum Frequency = > 1.1 GHz Typical
- Operating Range: V_{CC} = 3.0 V to 3.6 V with GND = 0 V
- PNP LVTTL Inputs for Minimal Loading
- Q Output Will Default HIGH with Inputs Open
- The 100 Series Contains Temperature Compensation.
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

SOIC–8 NB
D SUFFIX
CASE 751–07

TSSOP–8
DT SUFFIX
CASE 948R–02

DFN8
MN SUFFIX
CASE 506AA

MARKING DIAGRAMS*

KPT22
ALYW
SOIC–8 NB

KA22
ALYW■
TSSOP–8
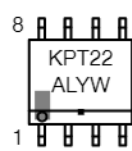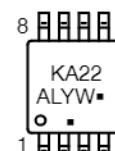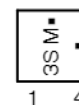
3S M
DFN8

A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
M	= Date Code
■	= Pb-Free Package

(Note: Microdot may be in either location)
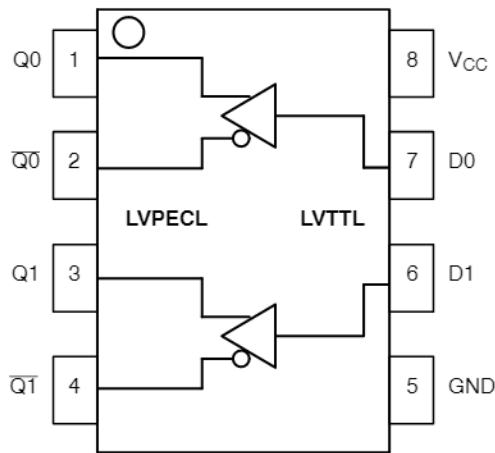
*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
MC100EPT22DG	SOIC–8 NB (Pb-Free)	98 Units/Tube
MC100EPT22DR2G	SOIC–8 NB (Pb-Free)	2500 Tape & Reel
MC100EPT22DTG	TSSOP–8 (Pb-Free)	100 Tape & Reel
MC100RPT22DTR2G	TSSOP–8 (Pb-Free)	2500 Tape & Reel
MC100EPT22MNR4G	DFN8 (Pb-Free)	1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC100EPT22

Figure 1. 8−Lead Pinout (Top View) **and Logic Diagram**

Table 1. PIN DESCRIPTION

PIN	FUNCTION
Q0, Q1, $\overline{Q0}$, $\overline{Q1}$	LVPECL Differential Outputs
D0, D1	LVTTL Inputs
V_{CC}	Positive Supply
GND	Ground
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

Table 2. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		N/A
Internal Input Pullup Resistor		N/A

ESD Protection
  Human Body Model
  Machine Model
  Charged Device Model
		> 4 kV
		> 200 V
		> 2 kV

Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb-Free Pkg
SOIC−8 NB TSSOP−8 DFN8		Level 1 Level 3 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		164 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Power Supply	GND = 0 V		6	V
V_I	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC−8 NB SOIC−8 NB	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC−8 NB	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP−8 TSSOP−8	185 140	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP−8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W
T_{sol}	Wave Solder (Pb-Free)			265	°C
θ_{JC}	Thermal Resistance (Junction-to-Case)	(Note 1)	DFN8	35 to 40	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

Table 4. TTL INPUT DC CHARACTERISTICS (V_{CC} = 3.3 V, GND = 0 V, T_A= −40°C to 85°C)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V			20	µA
I_{IHH}	Input HIGH Current MAX	V_{IN} = V_{CC}			100	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V			−0.6	mA
V_{IK}	Input Clamp Voltage	I_{IN} = −18 mA			−1.0	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 5. PECL OUTPUT DC CHARACTERISTICS (V_{CC} = 3.3 V, GND = 0.0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Power Supply Current	32	43	55	35	45	60	37	46	62	mA
V_{OH}	Output HIGH Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 2)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Output parameters vary 1:1 with V_{CC}.
2. All loading with 50 Ω to V_{CC} − 2.0 V.

Table 6. AC CHARACTERISTICS (V_{CC} = 3.0 V to 3.6 V, GND = 0.0 V (Note 1))

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (Figure 2)	0.8	1.1		0.8	1.1		0.8	1.1		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	250	400	650	250	420	675	300	500	700	ps
t_{skew}	Within–Device Skew (Note 2) Device-to-Device Skew (Note 3)		50 200	100 400		50 200	100 425		50 200	100 400	ps
t_{JITTER}	Random Clock Jitter (Figure 2)		0.2	< 1		0.2	< 1		0.2	< 1	ps
$t_{JIT(\Phi)}$	Additive Phase RMS Jitter Integration Range 12 kHz to 20 MHz 25 MHz 156.25 MHz					0.05 0.16					ps
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20%–80%)	50	110	200	60	120	220	70	140	250	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Measured using a 2.4 V source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} – 2.0 V.
2. Skew is measured between outputs under identical transitions and conditions on any one device.
3. Device-to-Device Skew for identical transitions at identical V_{CC} levels.
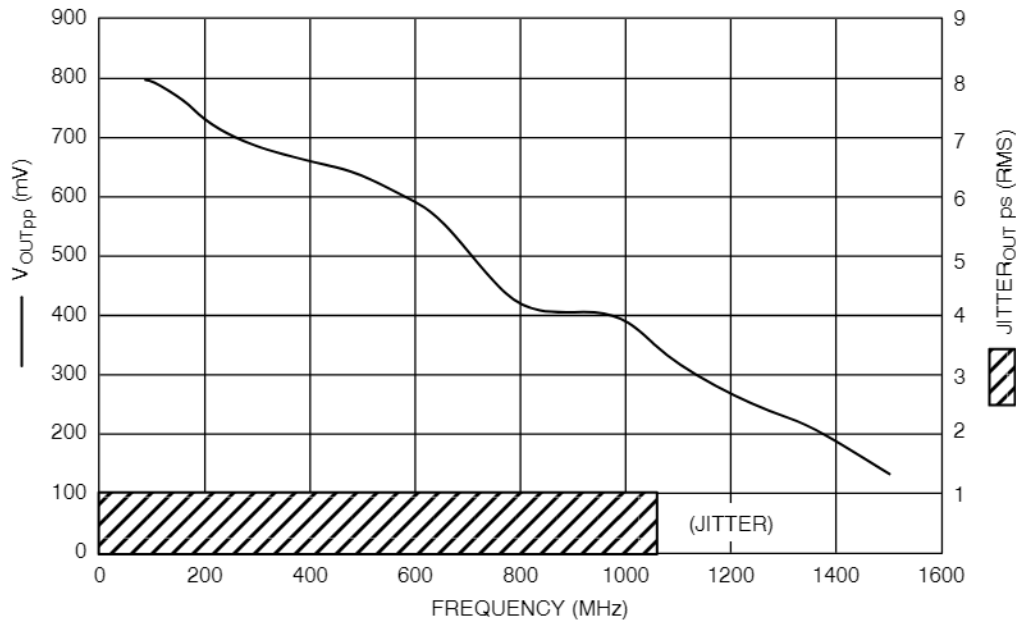
Figure 2. F_{max}/Jitter
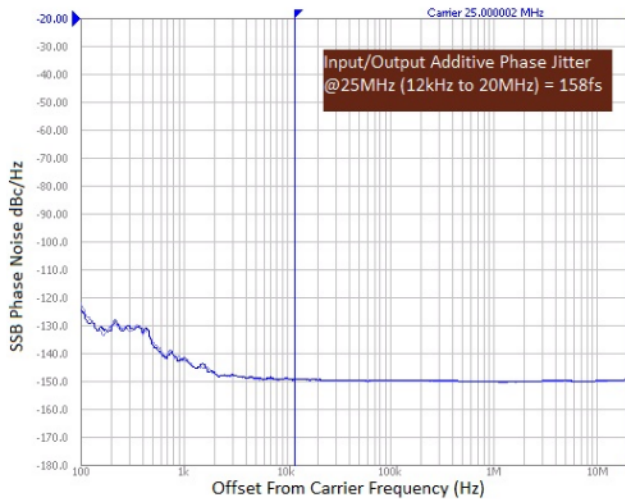
Figure 3. Typical Phase Noise Plot at
$f_{carrier}$ = 25 MHz
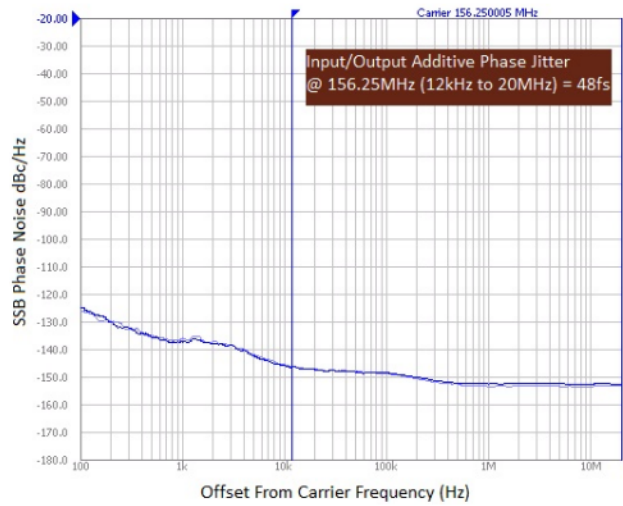
Figure 4. Typical Phase Noise Plot at
$f_{carrier}$ = 156.25 MHz

The above phase noise plots captured using Agilent E5052A show additive phase noise of the MC100EPT22 device at frequencies 25 MHz and 156.25 MHz respectively at an operating voltage of 3.3 V in room temperature. The RMS Phase Jitter contributed by the device (integrated between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 158 fs and 48 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.
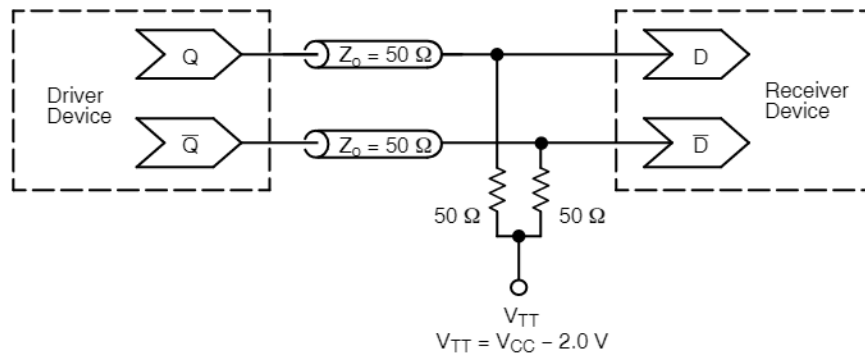
Figure 5. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices)

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

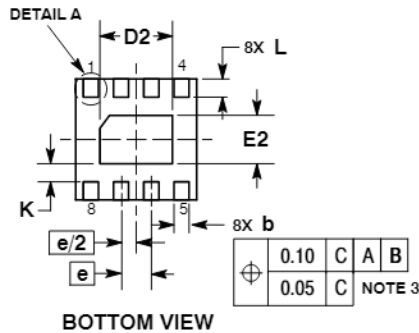**AND8090/D** – AC Characteristics of ECL Devices
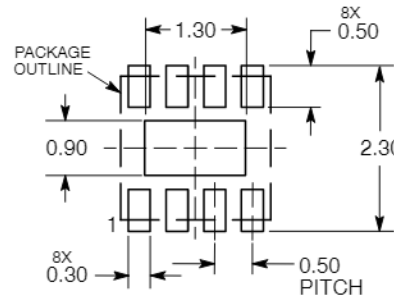
PACKAGE DIMENSIONS

SOIC−8 NB
D SUFFIX
CASE 751−07
ISSUE AK
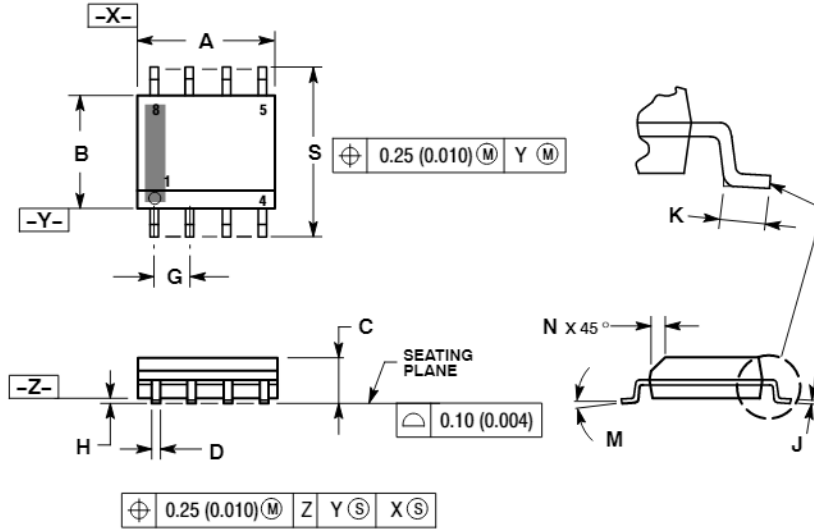
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*
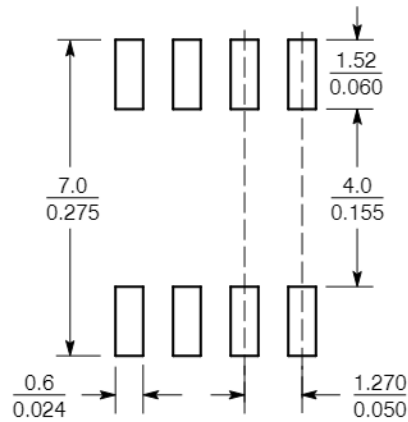
SCALE 6:1 $\left(\dfrac{mm}{inches}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP–8
DT SUFFIX
CASE 948R–02
ISSUE A
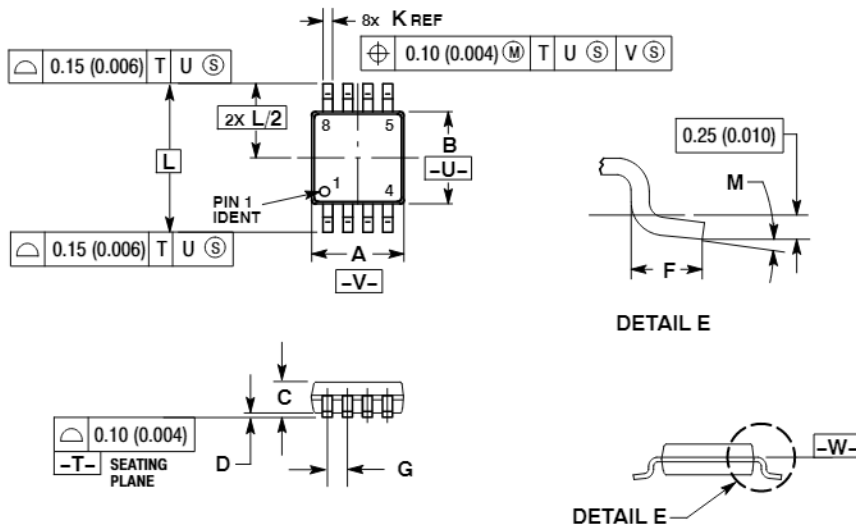
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

PACKAGE DIMENSIONS

DFN8 2x2, 0.5 P
MN SUFFIX
CASE 506AA
ISSUE F
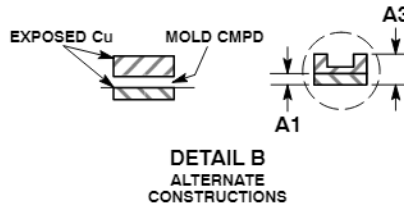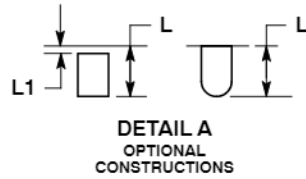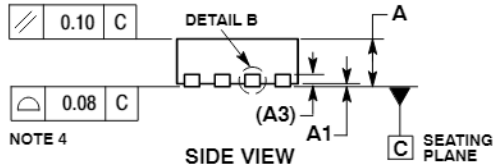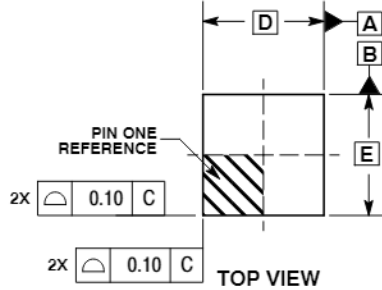
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.30 REF	
L	0.25	0.35
L1	---	0.10

DETAIL A
OPTIONAL CONSTRUCTIONS

EXPOSED Cu   MOLD CMPD

DETAIL B
ALTERNATE CONSTRUCTIONS

PIN ONE REFERENCE

2X | 0.10 | C

2X | 0.10 | C

TOP VIEW

0.10 | C

DETAIL B

0.08 | C

NOTE 4

SIDE VIEW

SEATING PLANE

DETAIL A

8X L

E2

8X b

e/2

e

0.10 | C A B
0.05 | C   NOTE 3

BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*

PACKAGE OUTLINE

1.30

8X 0.50

0.90

2.30

8X 0.30

0.50 PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION