# **5 V ECL 4-Bit D Flip-Flop**

### Description

The MC10E/100E131 is a quad master-slave D-type flip-flop with differential outputs. Each flip-flop may be clocked separately by holding Common Clock (C<sub>C</sub>) LOW and using the Clock Enable ( $\overline{CE}$ ) inputs for clocking. Common clocking is achieved by holding the  $\overline{CE}$  inputs LOW and using C<sub>C</sub> to clock all four flip-flops. In this case, the  $\overline{CE}$  inputs perform the function of controlling the common clock, to each flip-flop.

Individual asynchronous resets are provided (R). Asynchronous set controls (S) are ganged together in pairs, with the pairing chosen to reflect physical chip symmetry.

Data enters the master when both  $C_C$  and  $\overline{CE}$  are LOW, and transfers to the slave when either  $C_C$  or  $\overline{CE}$  (or both) go HIGH.

The 100 Series contains temperature compensation.

#### Features

- 1100 MHz Min. Toggle Frequency
- Differential Outputs
- Individual and Common Clocks
- Individual Resets (asynchronous)
- Paired Sets (asynchronous)
- PECL Mode Operating Range:
  - $V_{CC} = 4.2 \text{ V to } 5.7 \text{ V with } V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:
  - $V_{CC} = 0$  V with  $V_{EE} = -4.2$  V to -5.7 V
- Metastability Time Constant is 200 ps.
- Internal Input 50 k $\Omega$  Pulldown Resistors
- ESD Protection:
  - Human Body Model; > 2 kV
  - Machine Model; > 200 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level: 3 (Pb-Free)
  - For Additional Information, see Application Note <u>AND8003/D</u>
- Flammability Rating:UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 240 devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



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PLCC-28 FN SUFFIX CASE 776-02

### **MARKING DIAGRAM\***



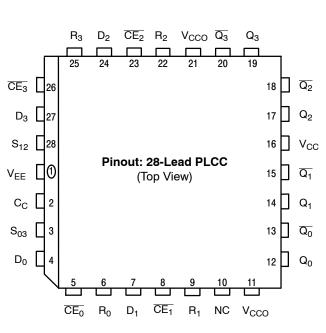
XXX	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

\*For additional marking information, refer to Application Note <u>AND8002/D</u>.

### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC10E131FNG	PLCC-28 (Pb-Free)	37 Units/Tube
MC10E131FNR2G	PLCC-28 (Pb-Free)	500/Tape & Reel
MC100E131FNG	PLCC-28 (Pb-Free)	37 Units/Tube
MC100E131FNR2G	PLCC-28 (Pb-Free)	500/Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, <u>BRD8011/D</u>.



\* All  $V_{CC}$  and  $V_{CCO}$  pins are tied together on the die.

Warning: All  $V_{CC}$ ,  $V_{CCO}$ , and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

#### Figure 1. Pinout Diagram

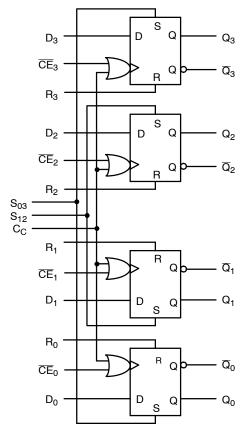


Figure 2. Logic Diagram

PIN	FUNCTION						
D <sub>0</sub> – D <sub>3</sub>	ECL Data Inputs						
$\overline{CE}_0 - \overline{CE}_3$	ECL Clock Enables (Individual)						
R <sub>0</sub> – R <sub>3</sub>	ECL Resets						
C <sub>C</sub>	ECL Common Clock						
S <sub>03</sub> , S <sub>12</sub>	ECL Sets (paired)						
$Q_0 - Q_3, \overline{Q}_0 - \overline{Q}_3$	ECL Differential Outputs						
V <sub>CC</sub> , V <sub>CCO</sub>	Positive Supply						
V <sub>EE</sub>	Negative Supply						
NC	No Connect						

#### Table 1. PIN DESCRIPTION

#### **Table 2. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		8	V
$V_{EE}$	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-8	V
VI	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	$\begin{array}{l} V_I \leq V_{CC} \\ V_I \geq V_{EE} \end{array}$	6 -6	V
l <sub>out</sub>	Output Current	Continuous Surge		50 100	mA
T <sub>A</sub>	Operating Temperature Range			0 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	PLCC-28	63.5 43.5	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	PLCC-28	22 to 26	°C/W
T <sub>sol</sub>	Wave Solder (Pb-Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

		-40°C				0°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I <sub>EE</sub>	Power Supply Current		58	70		58	70		58	70		58	70	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)				3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)				3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V <sub>IH</sub>	Input HIGH Voltage				3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V <sub>IL</sub>	Input LOW Voltage				3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
Ι <sub>ΙΗ</sub>	Input HIGH Current C <sub>C</sub> S R, CE D			350 450 300 150			350 450 300 150			350 450 300 150			350 450 300 150	μΑ
IIL	Input LOW Current				0.5	0.3		0.5	0.25		0.3	0.2		μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary –0.46 V / +0.06 V. 2. Outputs are terminated through a 50  $\Omega$  resistor to V<sub>CC</sub> – 2.0 V.

## Table 4. 10E SERIES NECL DC CHARACTERISTICS (V<sub>CCx</sub> = 0.0 V; V<sub>EE</sub> = -5.0 V (Note 1))

			<b>−40°C</b>			0°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I <sub>EE</sub>	Power Supply Current		58	70		58	70		58	70		58	70	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)				-1020	-930	-840	-980	-895	-810	-910	-815	-720	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)				-1950	-1790	-1630	-1950	-1790	-1630	-1950	-1773	-1595	mV
V <sub>IH</sub>	Input HIGH Voltage				-1170	-1005	-840	-1130	-970	-810	-1060	-890	-720	mV
VIL	Input LOW Voltage				-1950	-1715	-1480	-1950	-1715	-1480	-1950	-1698	-1445	mV
Ι <sub>ΙΗ</sub>	Input HIGH Current C <sub>C</sub> S R, CE D			350 450 300 150			350 450 300 150			350 450 300 150			350 450 300 150	μA
IIL	Input LOW Current				0.5	0.3		0.5	0.065		0.3	0.2		μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary –0.46 V / +0.06 V.

2. Outputs are terminated through a 50  $\Omega$  resistor to V<sub>CC</sub> – 2.0 V.

### Table 5. 100E SERIES PECL DC CHARACTERISTICS (V<sub>CCx</sub> = 5.0 V; V<sub>EE</sub> = 0.0 V (Note 1))

			–40°C 0°C 25°C						85°C					
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I <sub>EE</sub>	Power Supply Current		58	70		58	70		58	70		67	81	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)				3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)				3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V <sub>IH</sub>	Input HIGH Voltage		3975		3835	3975	4120	3835	3975	4120	3835	3975	4120	mV
V <sub>IL</sub>	Input LOW Voltage		3355		3190	3355	3525	3190	3355	3525	3190	3355	3525	mV
Iн	Input HIGH Current C <sub>C</sub> S R, CE D			350 450 300 150			350 450 300 150			350 450 300 150			350 450 300 150	μΑ
IIL	Input LOW Current				0.5	0.3		0.5	0.25		0.5	0.2		μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary –0.46 V / +0.8 V. 2. Outputs are terminated through a 50  $\Omega$  resistor to V<sub>CC</sub> – 2.0 V.

## Table 6. 100E SERIES NECL DC CHARACTERISTICS ( $V_{CCx}$ = 0.0 V; $V_{EE}$ = -5.0 V (Note 1))

			–40°C			0°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I <sub>EE</sub>	Power Supply Current		58	70		58	70		58	70		67	81	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)				-1025	-950	-880	-1025	-950	-880	-1025	-950	-880	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)				-1810	-1705	-1620	-1810	-1745	-1620	-1810	-1740	-1620	mV
VIH	Input HIGH Voltage		-1025		-1165	-1025	-880	-1165	-1025	-880	-1165	-1025	-880	mV
VIL	Input LOW Voltage		-1645		-1810	-1645	-1475	-1810	-1645	-1475	-1810	-1645	-1475	mV
lιΗ	Input HIGH Current C <sub>C</sub> S R, CE D			350 450 300 150			350 450 300 150			350 450 300 150			350 450 300 150	μΑ
١ <sub>IL</sub>	Input LOW Current				0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{FF}$  can vary -0.46 V / +0.8 V.

2. Outputs are terminated through a 50  $\Omega$  resistor to V<sub>CC</sub> – 2.0 V.

#### Table 7. AC CHARACTERISTICS ( $V_{CCx} = 5.0 \text{ V}$ ; $V_{EE} = 0.0 \text{ V}$ or $V_{CCx} = 0.0 \text{ V}$ ; $V_{EE} = -5.0 \text{ V}$ (Note 1))

			<b>−40°C</b>			25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit	
f <sub>MAX</sub>	Maximum Toggle Frequency	1100	1400		1100	1400		1100	1400		MHz	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay to Output CE C <sub>C</sub> R S	310 275 400 300	600 600 635 550	750 725 875 775	360 325 450 350	500 500 640 550	700 675 825 725	360 325 450 350	500 500 640 550	700 675 825 725	ps	
t <sub>S</sub>	Setup Time (Note 2) D	200	20		150	20		150	20		ps	
t <sub>H</sub>	Hold Time (Note 2) D	225	-20		175	-20		175	-20		ps	
t <sub>RR</sub>	Reset Recovery Time	450	150		400	150		400	150		ps	
t <sub>PW</sub>	Minimum Pulse Width CLK R, S	400 400			400 400			400 400			ps	
t <sub>SKEW</sub>	Within-Device Skew (Note 3)		60			60			60		ps	
t <sub>JITTER</sub>	Random Clock Jitter		< 1			< 1			< 1		ps	
t <sub>r</sub> /t <sub>f</sub>	Rise/Fall Time (20-80%)	275	460	725	300	480		300	480	675	ps	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. 10 Series: V<sub>EE</sub> can vary -0.46 V / +0.06 V.

100 Series: VEE can vary -0.46 V / +0.8 V.

2. Setup/hold times guaranteed for both  $C_C$  and  $\overline{CE}$ .

3. Within-device skew is defined as identical transitions on similar paths through a device.

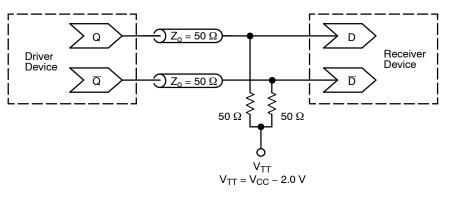


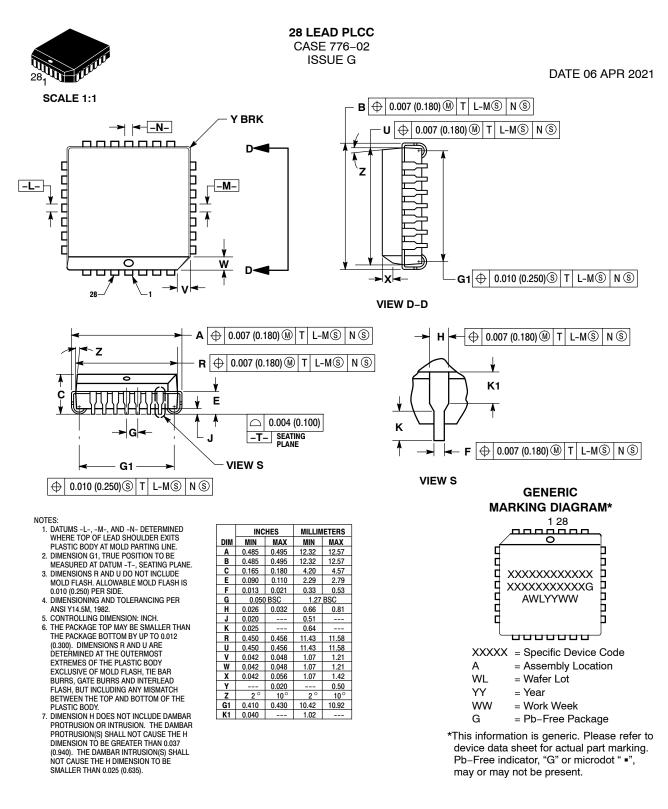
Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note<u>AND8020/D</u> – Termination of ECL Logic Devices.)

#### **Resource Reference of Application Notes**

AN1405/D	-	ECL Clock Distribution Techniques
AN1406/D	-	Designing with PECL (ECL at +5.0 V)
AN1503/D	-	ECLinPS <sup>™</sup> I/O SPiCE Modeling Kit
AN1504/D	-	Metastability and the ECLinPS Family
AN1568/D	-	Interfacing Between LVDS and ECL
AN1672/D	-	The ECL Translator Guide
AND8001/D	-	Odd Number Counters Design
AND8002/D	-	Marking and Date Codes
AND8020/D	-	Termination of ECL Logic Devices
AND8066/D	-	Interfacing with ECLinPS
AND8090/D	-	AC Characteristics of ECL Devices

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