

BDV65B (NPN), BDV64B (PNP)

Complementary Silicon Plastic Power Darlington

... for use as output devices in complementary general purpose amplifier applications.

Features

- High DC Current Gain – HFE = 1000 (min) @ 5 A_{dc}
- Monolithic Construction with Built-in Base Emitter Shunt Resistors
- These are Pb-Free Devices*

MAXIMUM RATINGS

| Rating | Symbol | Max | Unit |
|---|-----------------------------------|----------------|-----------------|
| Collector-Emitter Voltage | V _{CEO} | 100 | Vdc |
| Collector-Base Voltage | V _{CB} | 100 | Vdc |
| Emitter-Base Voltage | V _{EB} | 5.0 | Vdc |
| Collector Current – Continuous – Peak | I _C | 10 20 | A _{dc} |
| Base Current | I _B | 0.5 | A _{dc} |
| Total Device Dissipation @ T _C = 25°C Derate above 25°C | P _D | 125 1.0 | W W/°C |
| Operating and Storage Junction Temperature Range | T _J , T _{stg} | -65 to +150 | °C |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|--------------------------------------|------------------|-----|------|
| Thermal Resistance, Junction-to-Case | R _{θJC} | 1.0 | °C/W |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

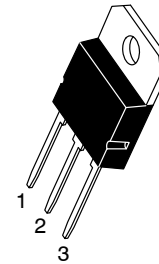
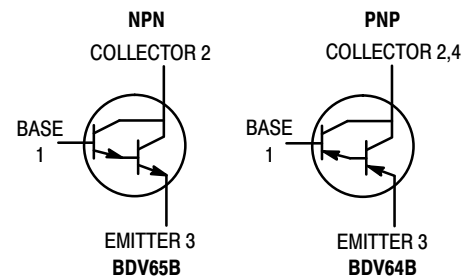
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



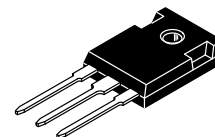
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10 AMPERE DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS 60-80-100-120 VOLTS, 125 WATTS



SOT-93
(TO-218)
CASE 340D



TO-247
CASE 340L
STYLE 3

NOTE: Effective June 2012 this device will be available only in the TO-247 package. Reference FPCN# 16827.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

BDV65B (NPN), BDV64B (PNP)

MARKING DIAGRAMS



BDV6xB = Device Code
 x = 4 or 5
 A = Assembly Location
 Y = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

| Device Order Number | Package Type | Shipping |
|---------------------|---------------------|-----------------|
| BDV65BG | TO-218 (Pb-Free) | 30 Units / Rail |
| BDV64BG | TO-218 (Pb-Free) | 30 Units / Rail |
| BDV65BG | TO-247 (Pb-Free) | 30 Units / Rail |
| BDV64BG | TO-247 (Pb-Free) | 30 Units / Rail |



Figure 1. Power Derating

BDV65B (NPN), BDV64B (PNP)

ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Min | Max | Unit |
|---|----------------|------|-----|------|
| OFF CHARACTERISTICS | | | | |
| Collector–Emitter Sustaining Voltage (1) ($I_C = 30 \text{ mAdc}$, $I_B = 0$) | $V_{CEO(sus)}$ | 100 | – | Vdc |
| Collector Cutoff Current ($V_{CE} = 50 \text{ Vdc}$, $I_B = 0$) | I_{CEO} | – | 1.0 | mAdc |
| Collector Cutoff Current ($V_{CB} = 100 \text{ Vdc}$, $I_E = 0$) | I_{CBO} | – | 0.4 | mAdc |
| Collector Cutoff Current ($V_{CB} = 50 \text{ Vdc}$, $I_E = 0$, $T_C = 150^\circ\text{C}$) | I_{CBO} | – | 2.0 | mAdc |
| Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$) | I_{EBO} | – | 5.0 | mAdc |
| ON CHARACTERISTICS | | | | |
| DC Current Gain ($I_C = 5.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) | h_{FE} | 1000 | – | – |
| Collector–Emitter Saturation Voltage ($I_C = 5.0 \text{ Adc}$, $I_B = 0.02 \text{ Adc}$) | $V_{CE(sat)}$ | – | 2.0 | Vdc |
| Base–Emitter Saturation Voltage ($I_C = 5.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) | $V_{BE(on)}$ | – | 2.5 | Vdc |

BDV65B (NPN), BDV64B (PNP)

NPN

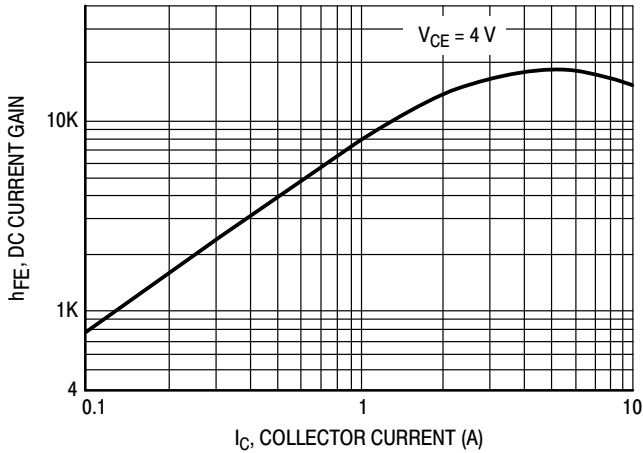


Figure 2. DC Current Gain

PNP



Figure 3. DC Current Gain

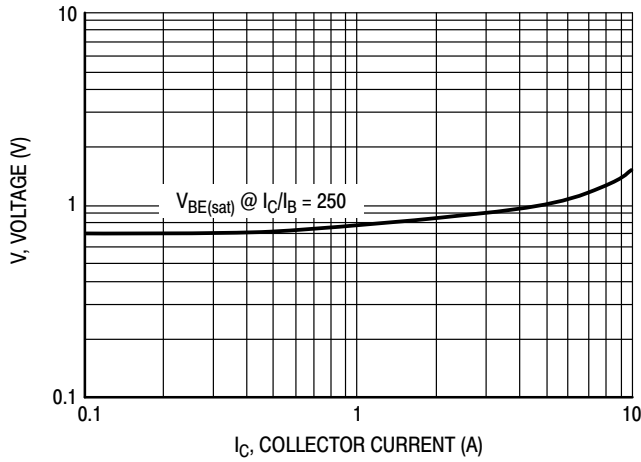


Figure 4. "On" Voltages

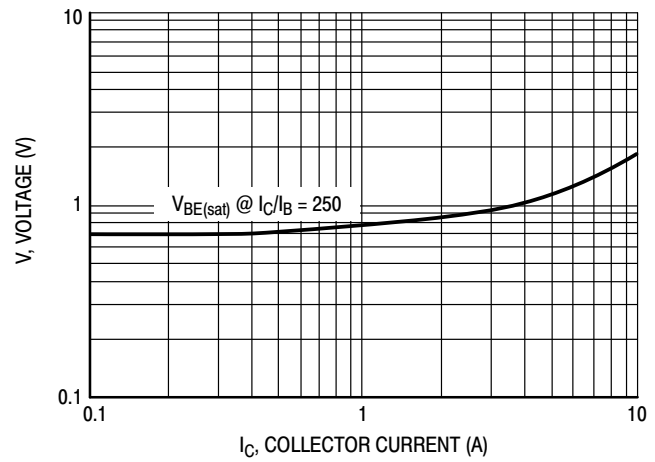


Figure 5. "On" Voltages

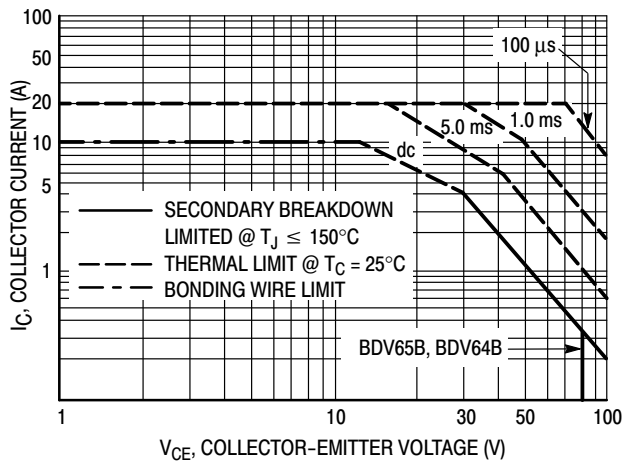


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150^\circ\text{C}$, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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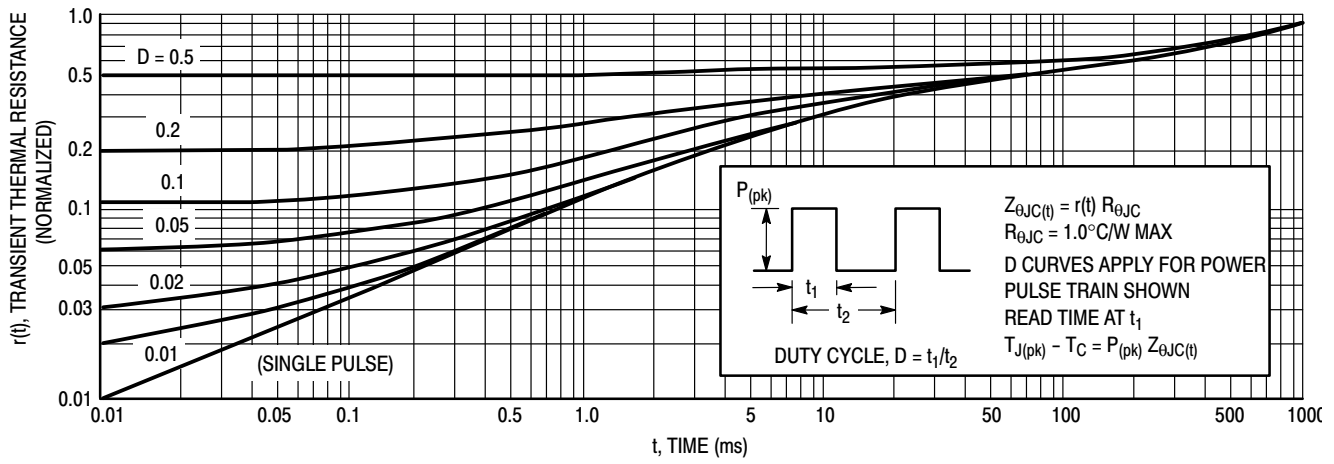


Figure 7. Thermal Response

MECHANICAL CASE OUTLINE

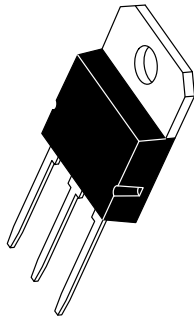
PACKAGE DIMENSIONS

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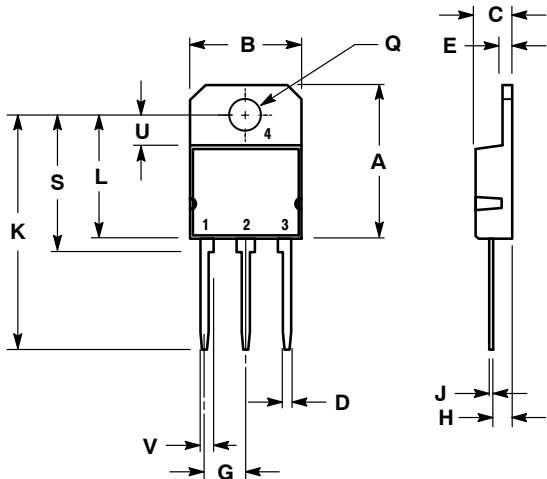


SOT-93 (TO-218) CASE 340D-02 ISSUE E

DATE 01/03/2002



SCALE 1:1



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 20.35 | --- | 0.801 |
| B | 14.70 | 15.20 | 0.579 | 0.598 |
| C | 4.70 | 4.90 | 0.185 | 0.193 |
| D | 1.10 | 1.30 | 0.043 | 0.051 |
| E | 1.17 | 1.37 | 0.046 | 0.054 |
| G | 5.40 | 5.55 | 0.213 | 0.219 |
| H | 2.00 | 3.00 | 0.079 | 0.118 |
| J | 0.50 | 0.78 | 0.020 | 0.031 |
| K | 31.00 REF | | 1.220 REF | |
| L | --- | 16.20 | --- | 0.638 |
| Q | 4.00 | 4.10 | 0.158 | 0.161 |
| S | 17.80 | 18.20 | 0.701 | 0.717 |
| U | 4.00 REF | | 0.157 REF | |
| V | 1.75 REF | | 0.069 | |

MARKING DIAGRAM



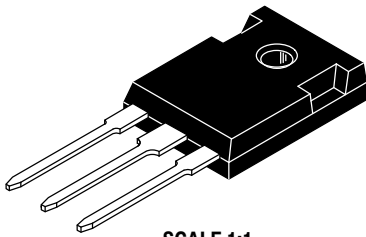
A = Assembly Location
Y = Year
WW = Work Week
xxxxx = Device Code

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

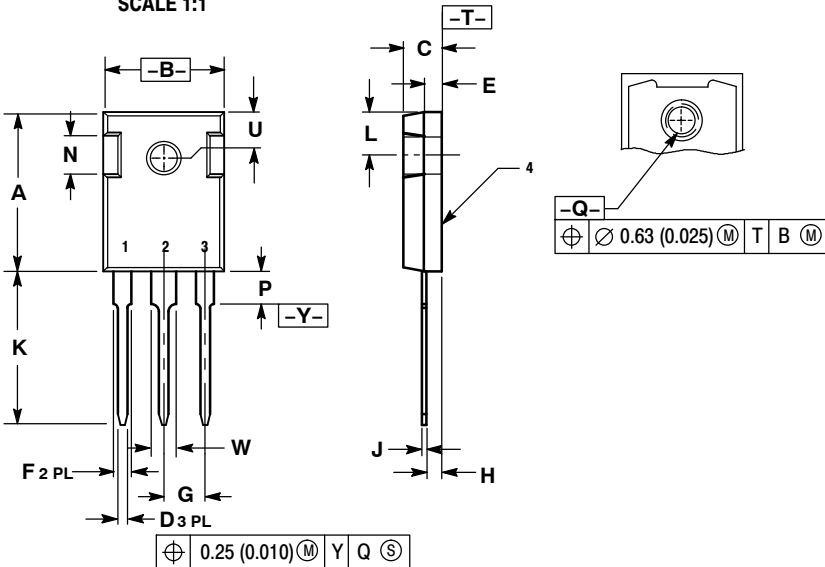
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TO-247
CASE 340L-02
ISSUE F

DATE 26 OCT 2011

SCALE 1:1

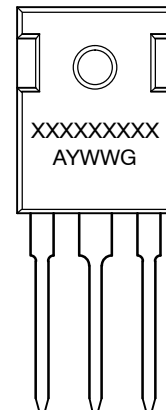


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 20.32 | 21.08 | 0.800 | 0.830 |
| B | 15.75 | 16.26 | 0.620 | 0.640 |
| C | 4.70 | 5.30 | 0.185 | 0.209 |
| D | 1.00 | 1.40 | 0.040 | 0.055 |
| E | 1.90 | 2.60 | 0.075 | 0.102 |
| F | 1.65 | 2.13 | 0.065 | 0.084 |
| G | 5.45 BSC | | 0.215 BSC | |
| H | 1.50 | 2.49 | 0.059 | 0.098 |
| J | 0.40 | 0.80 | 0.016 | 0.031 |
| K | 19.81 | 20.83 | 0.780 | 0.820 |
| L | 5.40 | 6.20 | 0.212 | 0.244 |
| N | 4.32 | 5.49 | 0.170 | 0.216 |
| P | --- | 4.50 | --- | 0.177 |
| Q | 3.55 | 3.65 | 0.140 | 0.144 |
| U | 6.15 BSC | | 0.242 BSC | |
| W | 2.87 | 3.12 | 0.113 | 0.123 |

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package


- STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN
- STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)
- STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE
- STYLE 6:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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| NEW STANDARD: | | |
| DESCRIPTION: | TO-247 | PAGE 1 OF 2 |



| ISSUE | REVISION | DATE |
|-------|---|-------------|
| D | CHANGE OF OWNERSHIP FROM MOTOROLA TO ON SEMICONDUCTOR. DIM A WAS 20.80-21.46/0.819-0.845. DIM K WAS 19.81-20.32/0.780-0.800. UPDATED STYLE 1, ADDED STYLES 2, 3, & 4. REQ. BY L. HAYES. | 25 AUG 2000 |
| E | DIM E MINIMUM WAS 2.20/0.087. DIM K MINIMUM WAS 20.06/0.790. ADDED GENERIC MARKING DIAGRAM. REQ. BY S. ALLEN. | 26 FEB 2010 |
| F | ADDED STYLES 5 AND 6. REQ. BY J. PEREZ. | 26 OCT 2011 |
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