BLDC Motor Pre-driver with Speed Control, Single-phase, 12 V, 24 V and 48 V

LV8310H

ON Semiconductor®

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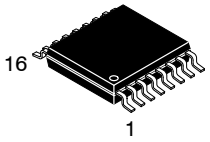


TSSOP−16
CASE 948F

Overview

The LV8310HGR2G is a pre-driver for a 12 V, 24 V and 48 V single phase BLDC motor, which controls motor rotational speed with the built-in closed loop speed controller. Its target speed can be set by input PWM duty cycle. The speed curve setting can be stored to the internal nonvolatile memory (NVM). In addition, Lead-angle can also be adjusted by the configuration saved in the internal NVM. Thus, it can drive various kinds of motors at high efficiency and low noise.

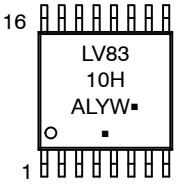
Features

- Driver Output for External Power FETs (P-MOS High Side, N-MOS Low Side)
- Selectable High Side Gate Driver Polarity: One for 12 V Motor Voltage and the other for 24 V/48 V Motor Voltage with External Level Shifter FET
- PI Closed Loop Speed Control Function
- Single-phase Full Wave Driver
- PWM Duty Cycle Input (25 Hz to 100 kHz)
- Soft Start-up Function
- PWM Soft Switching Phase Transitions
- Soft PWM Duty Cycle Transitions (Changing the Target Speed Gradually)
- Built-in Current Limit Function and Over Current Protection Function
- Built-in Thermal Protection Function
- Built-in Locked Rotor Protection and Automatic Recovery Function
- FG or RD Signal Output Selectable
- Dynamic Lead Angle Adjustment with Respect to Input Duty Cycle
- Parameter Setting by Serial Communication
- Embedded EEPROM as NVM
- Parameter Setting to the NVM
- Pb-Free and Halogen Free

Typical Applications

- Telecom Server and Base Station Cooling Fan
- Desktop PC Cooling Fan
- Server Cooling Fan
- Refrigerator Circulation Fan
- Appliance Cooling Fan
- Power Supply Unit Cooling Fan

MARKING DIAGRAM



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 34 of this data sheet.

Application Diagram

Figure 1 shows 12 V application diagram of the chip and Figure 2 shows the higher voltage (24 V/48 V) application diagram of the chip. For 12 V application, the REG and VDD pins must be hard wired to each other in the shortest path and the TYPE pin must be grounded. For the higher voltage application, the REG, VDD and TYPE pins must be hard wired to each other in the shortest path.

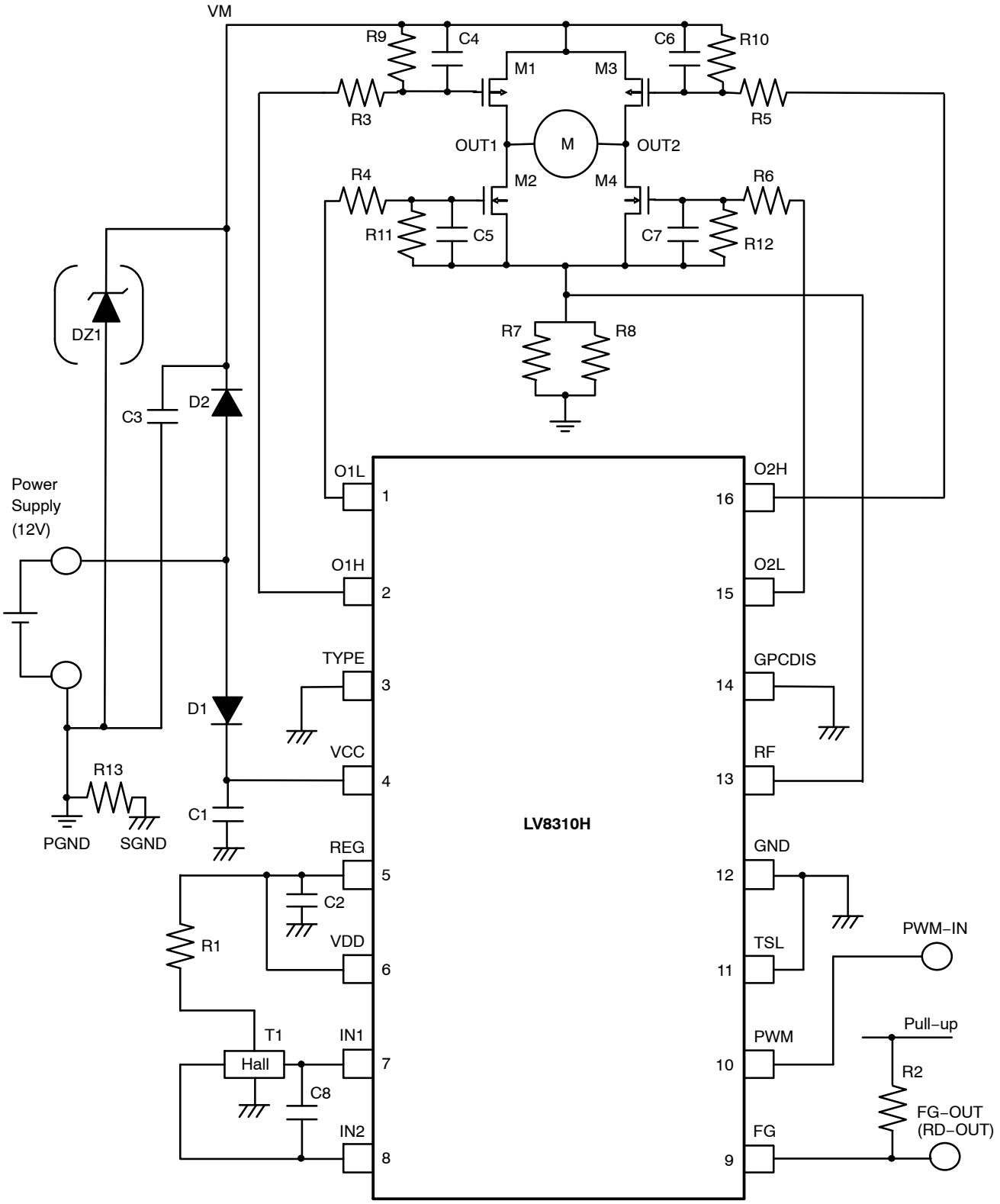


Figure 1. Example of Application Diagram for 12 V

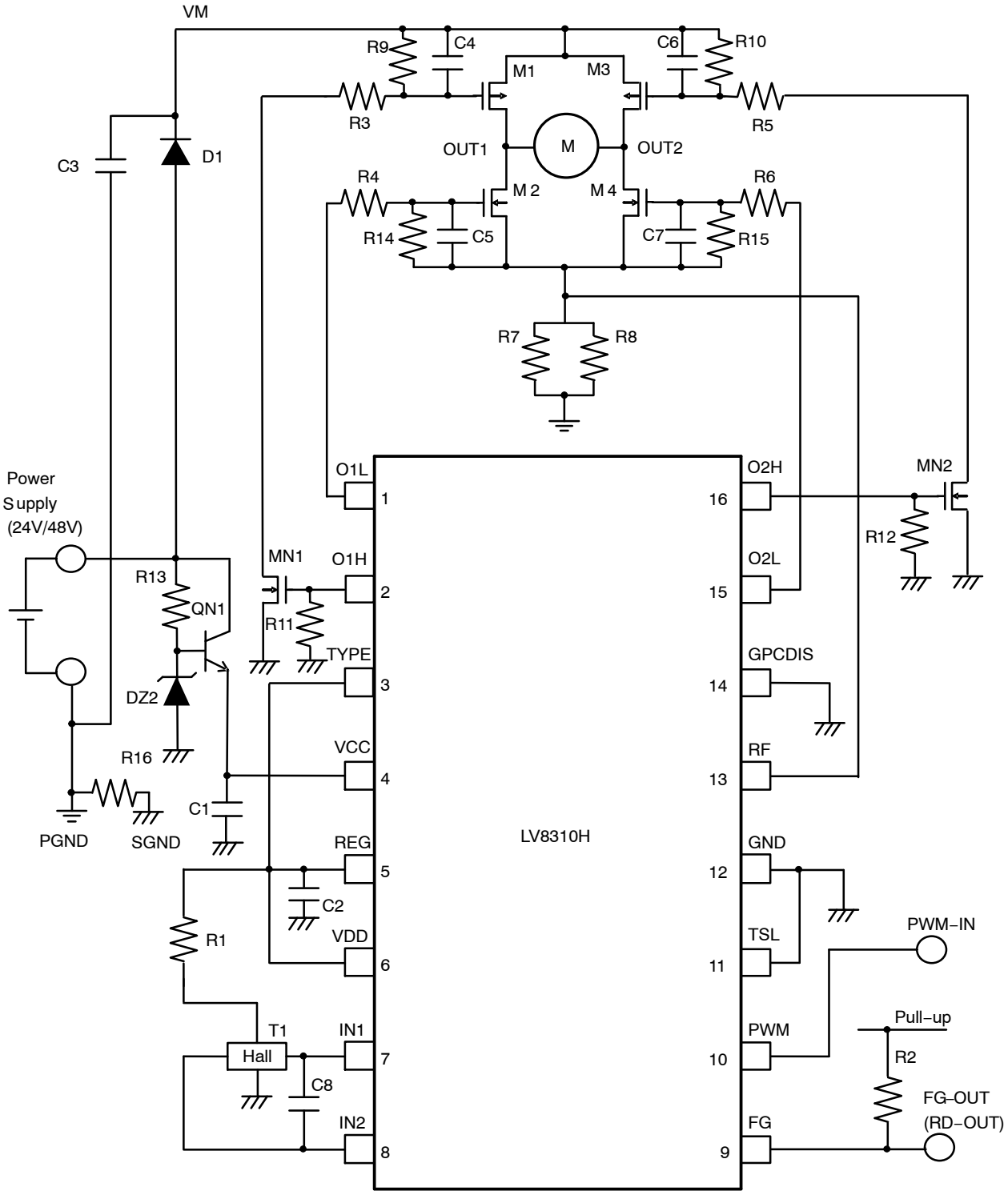


Figure 2. Example of Application Diagram for 24 V/48 V

External Components

Table 1 shows the external component list for 12 V application and Table 2 shows the external component list for higher voltage application.

Please refer to Table 9 “Pin Description” as well.

Table 1. EXAMPLE OF EXTERNAL COMPONENT VALUE FOR 12 V APPLICATION (Figure 1)

Device	Qty	Description	Value	Tol	Footprint	Manufacture	Manufacture Part Number
M1, M3	1	Power MOS FET (Pch)	–	–	SOIC8	ON Semiconductor	FW4604
M2, M4	1	Power MOS FET (Nch)	–	–	SOIC8	ON Semiconductor	FW4604
D1	1	Anti-reverse connection diode	–	–			
D2	1	Anti-reverse connection diode	–	–			
DZ1	1	12 V Zener diode	12 V	–			
C1	1	VCC bypass capacitor	10 μF 50 V	10%			
C2	1	REG bypass capacitor	1 μF 25 V	10%			
C3	1	FET power bypass capacitor	10 μF 50 V	10%			
C4−C7	4	LPF resistor for FET gate	*	–			
C8	1	Filter of system noise	0.1 μF 50 V	10%			
R1	1	Current limiter resistor for Hall	2 kΩ 1/4 W	5%			
R2	1	FG pull-up resistor	10 kΩ 1/4 W	5%			
R3−R6	4	LPF capacitor for FET gate	100 Ω 1/8 W	5%			
R7, R8	2	Current sense resistor	100 mΩ 1 W	5%			
R9, R10	2	O1H/O2H pull-up resistor is required when Gate Polarity Check is enabled (GPCDIS pin = low) and TYPE pin = low	100 kΩ 1/8 W	5%			
R11, R12	2	Adjust the delay of FET drive	*				
R13	1	Short SGND to PGND	0 Ω 1/8 W	5%			
T1	1	Hall element					

*Depend on the user environment. If FW4604 is selected as a M1, M2, M3 and M4, these components are not needed.

Table 2. EXAMPLE OF EXTERNAL COMPONENT VALUE FOR HIGHER VOLTAGE APPLICATION (Figure 2)

Device	Qty	Description	Value	Tol	Footprint	Manufacture	Manufacture Part Number
M1, M3	1	Power MOS FET (Pch)	–	–	SOIC8	ON Semiconductor	FW389
M2, M4	1	Power MOS FET (Nch)	–	–	SOIC8	ON Semiconductor	FW389
QN1	1	VCC voltage supply circuit NPN−Tr	–	–			
MN1, MN2	2	Nch-FET for high side drive	–	–			
D1	1	Anti-reverse connection diode	–	–			
DZ2	1	12 V Zener diode	12 V	–			
C1	1	VCC bypass capacitor	1 μF 50 V	10%			
C2	1	REG bypass capacitor	1 μF 25 V	10%			
C3	1	FET power bypass capacitor	10 μF 50 V	10%			

Table 2. EXAMPLE OF EXTERNAL COMPONENT VALUE FOR HIGHER VOLTAGE APPLICATION (Figure 2) (continued)

Device	Qty	Description	Value	Tol	Footprint	Manufacture	Manufacture Part Number
C4−C7	4	LPF resistor for FET gate	1000 pF 50 V	10%			
C8	1	Filter of system noise	0.1 μF 50 V	10%			
R1	1	Current limiter resistor for Hall	2 kΩ 1/4 W	5%			
R2	1	FG pull-up resistor	10 kΩ 1/4 W	5%			
R3−R6	4	LPF capacitor for FET gate	100 Ω 1/8 W	5%			
R7, R8	2	Current sense resistor	100 mΩ 1 W	5%			
R9, R10	2	Pch gate pull-up resistor is required when Gate Polarity Check is enabled (GPCDIS pin = low) and TYPE pin = high	1 kΩ 1/4 W	5%			
R11, R12	2	O1H/O2H pull-down resistor	10 kΩ 1/8 W	5%			
R13	1	VCC voltage supply circuit resistor	1 kΩ 1/2 W	5%			
R14, R15	2	Adjust the delay of FET drive					
R16	1	Short SGND to PGND	0 Ω 1/8 W	5%			
T1	1	Hall element	−	−			

VCC and GND (VCC, GND)

The power supplies of the IC need to be decoupled properly. The following three capacitors must be connected.

- between VCC (pin 4) and GND (pin 12) as C1 in the application diagrams
- between REG (VDD) and SGND as C2
- between VM and PGND as C3

The Zener diode (DZ1) in Figure 1 is mandatory to prevent the IC break down in case the supply voltage exceeds the absolute maximum ratings due to the flyback voltage.

Hall-Sensor Input Pins (IN1, IN2)

Differential output signals of the hall sensor are connected at IN1 and IN2. It is recommended that the capacitor (C8) is connected between both pins to filter system noise. The value of C8 should be selected properly depending on the system noise. When a Hall IC is used, the output of the Hall IC must be connected to the IN1 pin and the IN2 pin must be kept in the middle level of the Hall IC power supply voltage which should be corresponded to recommended operating range.

Command Input Pin (PWM)

This pin reads the duty cycle of the PWM pulse which controls rotational speed. The PWM input signal level is supported from 2.8 V to 5.5 V. Linear voltage control is not supported. The minimum pulse width is 100 ns.

Current Limiter Resistor for Hall (R1)

Hall output amplitude can be adjusted by R1.

The amplitude is proportional to Hall bias level VH for particular magnetic flux density. VH is determined by the following equation.

$$VH = VREG \times \left(\frac{Rh}{Rh + R1}\right) \quad \text{(eq. 1)}$$

Where

VREG: REG pin voltage (5 V)
Rh: Hall resistance

However, it should be considered with Hall sensor specification and Hall bias current. The bias current should be set under 20 mA which is REG pin max current.

Table 3. TRUTH TABLE (LV8310H, 12 V)

IN1	IN2	*Inner PWM State	O1L	O1H	O2L	O2H	FG	Operation State
L	H	On	H	H	L	L	Hi−Z	Drive mode
		Off	H	H	H	H		Regeneration mode
H	L	On	L	L	H	H	L	Drive mode
		Off	H	H	H	H		Regeneration mode

*Inner PWM state means the OUTPUT active period decided by inner control logic. Don't match with PWM−pin input signal.
*Condition: Register "DRVMODE [1:0]" = 01, TYPE = Low

Table 4. TRUTH TABLE (LV8310H, 24 V/48 V)

IN1	IN2	*Inner PWM State	O1L	O1H	O2L	O2H	FG	Operation State
L	H	On	H	L	L	H	Hi−Z	Drive mode
		Off	L	L	L	H		Regeneration mode
H	L	On	L	H	H	L	L	Drive mode
		Off	L	H	L	L		Regeneration mode

*Inner PWM state means the OUTPUT active period decided by inner control logic. Don't match with PWM−pin input signal.
*Condition: Register "DRVMODE [1:0]" = 10, TYPE = High

SPECIFICATIONS

Table 5. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	VCC_{MAX}	VCC pin	−0.3 to 20	V
Maximum output voltage	V_{OUTMAX}	O1H/O1L/O2H/O2L pin	20	V
Maximum output current	I_{OUTMAX}	O1H/O1L/O2H/O2L pin	50	mA
Maximum output peak current (Note 1)	I_{OUT}peak	O1H/O1L/O2H/O2L pin	150	mA
REG pin maximum output current	I_{REGMAX}	REG pin	20	mA
IN1/IN2 pin input voltage	V_{INMAX}	IN1/IN2 pin	−0.3 to 5.5	V
PWM pin input voltage	V_{PWMMAX}	PWM pin	−0.3 to 5.5	V
FG pin withstanding voltage	V_{FGMAX}	FG pin	−0.3 to 20	V
FG pin Maximum current	I_{FGMAX}	FG pin	7.5	mA
TYPE pin input voltage	$V_{TYPEMAX}$		−0.3 to 5.5	V
GPCDIS pin input voltage	V_{GPCMAX}		−0.3 to 5.5	V
Allowable power dissipation (Note 2)	P_{DMAX}	LV8310H	0.735	W
Operating temperature	T_{OP}		−40 to +105	°C
Storage temperature	T_{STG}		−55 to +150	°C
Maximum junction temperature	T_{Jmax}		150	°C
Moisture Sensitivity Level (MSL) (Note 3)	MSL		1	−
Lead Temperature Soldering Pb-Free Versions (30 s or less) (Note 4)	T_{SLD}		255	°C
ESD Human body Model: HBM (Note 5)	ESD_{HBM}		±4000	V
ESD Charged Device Model : CDM (Note 6)	ESD_{CDM}		±1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. I_{OUT}peak is the peak current with duty-cycle < 5%
2. Specified circuit board: Toroidal shaped. The actual area is 320 mm^2 and thickness is 0.8 mm, glass epoxy 2−layer board which has 1/2 oz copper traces on top and bottom of the board.
3. Moisture Sensitivity Level (MSL): IPC/JEDEC standard: J−STD−020A
4. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D
   http://www.onsemi.com/pub_link/Collateral/SOLDERRM−D.PDF
5. ESD Human Body Model is based on JEDEC standard: JESD22−A114
6. ESD Charged Device Model is based on JEDEC standard: JESD22−C101

Table 6. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	170	°C/W
Thermal Resistance, Junction-to-Case (Top) (Note 2)	$R_{\Psi JT}$	6.5	°C/W

Table 7. RECOMMENDED OPERATING RANGES

Parameter	Symbol	Conditions	Ratings	Unit
VCC supply voltage	VCC_{TYP}	VCC pin	12	V
VCC operating supply voltage range1	VCC_{OP1}	VCC pin	6.0 to 16	V
VCC operating supply voltage range2 (Note 7)	VCC_{OP2}	VCC pin	3.9 to 6.0	V
VCC operating supply voltage range for NVM program / erase operation	VCC_{NVM}	VCC pin	10.8 to 16	V
PWM input frequency range	F_{PWM}	PWM pin	25 to 100k	Hz
PWM minimum input low/high pulse width	T_{WPWM}	PWM pin	100	ns
IN1 input voltage range	V_{IN1}	IN1 pin	0 to VREG	V
IN2 input voltage range	V_{IN2}	IN2 pin	0.3 to 0.55 × VREG	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. When the VCC voltage is below 6.0 V, there are possibility to change the electric characteristics due to low VCC. However a motor keeps rotation until to 3.9 V, normally.

Table 8. ELECTRICAL CHARACTERISTICS (T_A = 25°C, VCC_{OP} = 12 V unless otherwise noted)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Circuit current	ICC		3.9	14	25	mA
O1H/O1L/O2H/O2L High−side on−resistance	R_{OH-ON}	I_O = 10 mA		30	80	Ω
O1H/O1L/O2H/O2L Low−side on−resistance	R_{OL-ON}	I_O = 10 mA		30	80	Ω
O1H/O1L/O2H/O2L PWM output frequency	f_{PWMO}			48		kHz
PWM pin low level input voltage	V_{PWML}		0		1.0	V
PWM pin high level input voltage	V_{PWMH}		2.3		5.5	V
PWM input resolution	Δ_{PWM}			8		Bit
PWM input bias current	Ipwmin	VDD = 5.5 V, PWM = 0 V	14	28	43	μA
TYPE pin input resistance	Rtype	To GND	100	200	300	KΩ
GPCDIS pin input resistance	Rgpcdis	To GND	100	200	300	KΩ
FG pin low level output voltage	V_{FGL}	I_{FG} = 5 mA			0.3	V
FG pin leak current	I_{FGLK}	VCC = 16 V, V_{FG} = 16 V			1	μA
REG pin output voltage	V_{REG}		4.7	5.0	5.3	V
REG pin output voltage load regulation	ΔVregld	IREG = −10 mA		20	50	mV
Lock−detection time1 (Note 8)	T_{LD1}	Under rotation	0.27	0.3	0.33	S
Lock−detection time2 (Note 9)	T_{LD2}	Start−up	0.63	0.7	0.77	S
Lock−Stop release time1 from 1st to 4th off time	T_{LRoff1}		3.1	3.5	3.9	S
Lock−Restart on time	T_{LRon}		0.63	0.7	0.77	S
Lock−Restart time ratio1	R_{LR1}	T_{LRoff1} / T_{LRon}		5		–
Lock−Stop release time2 (Note 10) as from 5th off time	T_{LRoff2}		12.5	14	15.5	S
Lock−Restart time ratio2 (Note 10) as from 5th off time	R_{LR2}	T_{LRoff2} / T_{LRon}		20		–
Thermal shutdown protection detection temperature	T_{TSD}	(Design Target)	150	180		°C
Thermal shutdown protection detection hysteresis	ΔT_{TSD}	(Design Target)		40		°C
Over current detection voltage	V_{OVC}		135	150	165	mV
Current limiter detection voltage	V_{CL}		90	100	110	mV
Hall input bias current	Ihin	IN1, IN2 = 0 V		0	1	μA

Table 8. ELECTRICAL CHARACTERISTICS (T_A = 25°C, VCC_{OP} = 12 V unless otherwise noted) (continued)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Hall input sensitivity	ΔVhin		40			mV
UVLO detection voltage	Vuvdet	VCC voltage	3.1	3.4	3.6	V
UVLO release voltage	Vuvrls	VCC voltage	3.3	3.6	3.9	V
UVLO hysteresis voltage	ΔVuv		0.1	0.2	0.4	V
NVM program/erase cycling	CYC_{NVM}	w.r.t. VCC_{NVM}			10	cycle
NVM data retention	RET_{NVM}		10			year

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. When a motor rotates with below 50 rpm (phase change period over 0.3 s), lock protection will works.
9. When a motor can't rotate for 0.7 s after start−up, lock protection will work.
10. When the locked rotor state continues for long time, lock stop period changes as from 5th off time.

Block Diagram

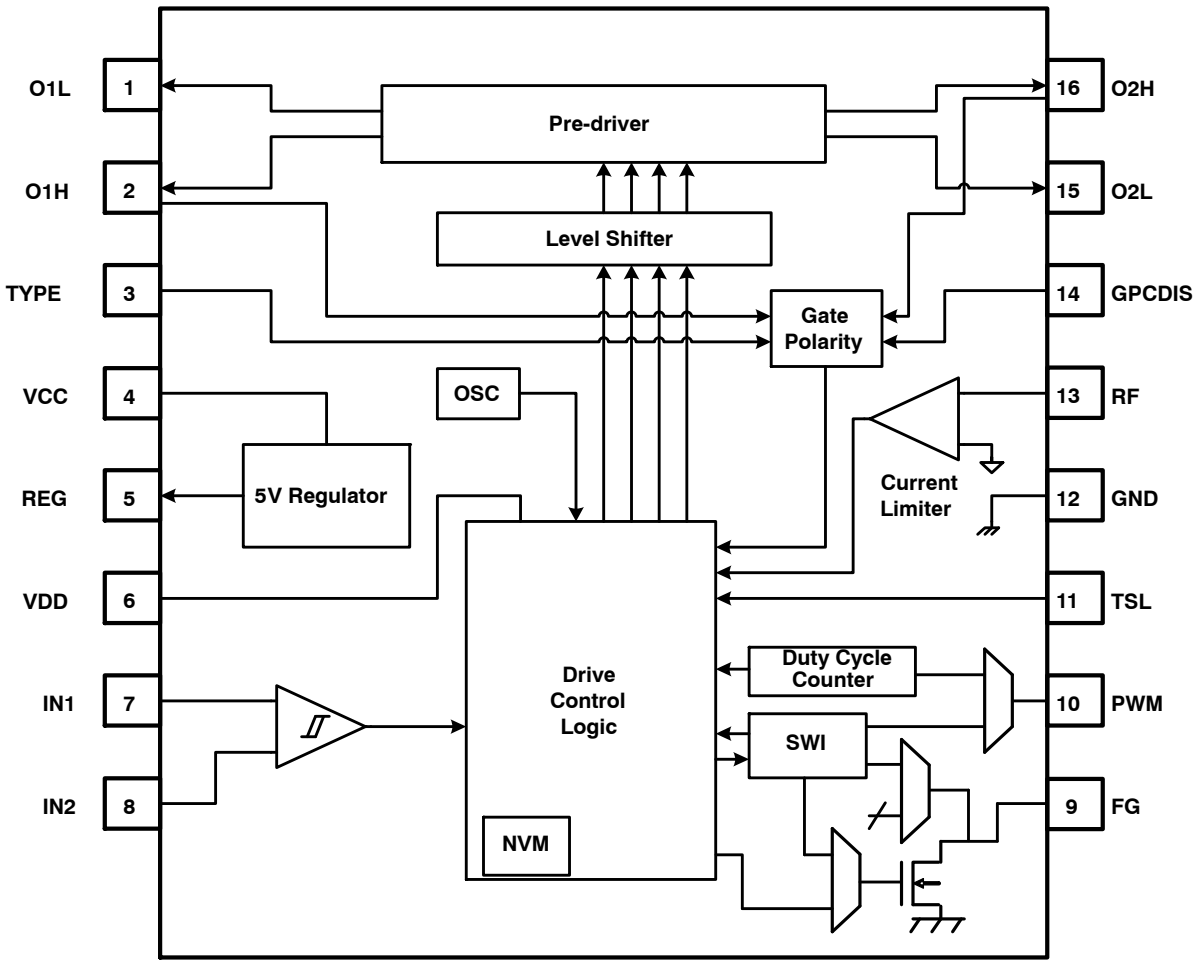


Figure 3. Block Diagram

Pin Assignment

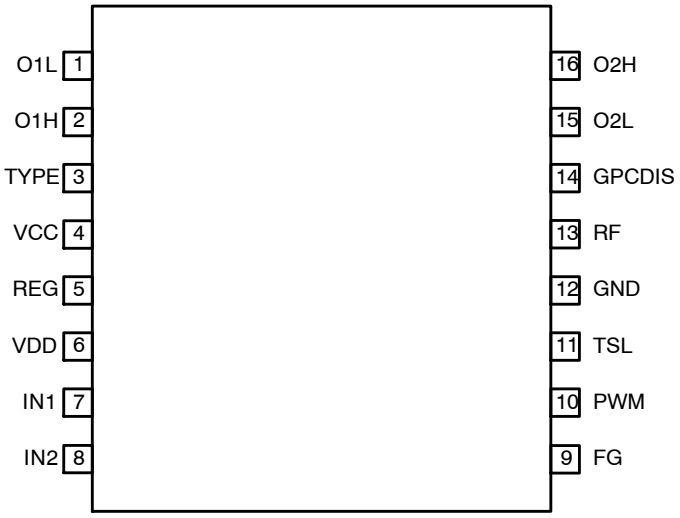


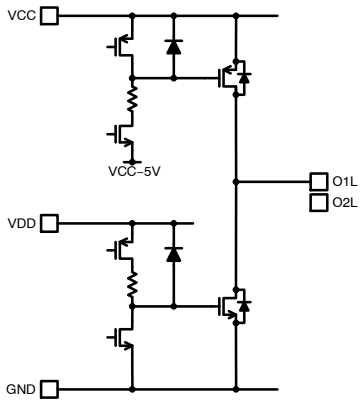
Figure 4. Pin Assignment Block Diagram

Table 9. PIN LIST AND FUNCTION

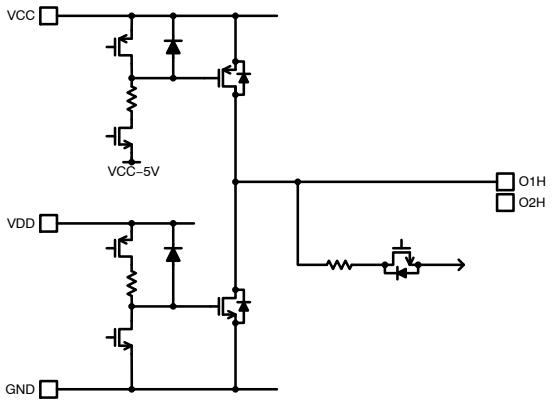
Pin No.	Pin Name	Description
1	O1L	Low-side external power FET's gate drive output
2	O1H	High-side external power FET's gate drive output
3	TYPE	Application type selection (L: 12 V application as shown in Figure 1, H: 24 V/48 V application as shown in Figure 2)
4	VCC	Power supply pin
5	REG	5 V regulator output. This voltage acts as a power source for oscillator, protection circuits, and so on. The maximum load current of REG is 20 mA. Be sure not to exceed this maximum current
6	VDD	Power supply pin for both digital and analog circuits. This pin must be connected to REG pin
7	IN1	Hall sensor input pin. The differential outputs of the hall sensor need to be connected to IN1 and IN2
8	IN2	
9	FG	The FG (frequency generator) output controls the motor electrical rotational speed (FG output synchronizes with the Hall sensor signal). This pin can function as RD (rotation detection) by bit setting of Reg. 0x010C "TACHSEL". The FG pin is an open drain output. Recommended pull up resistor is 1 kΩ to 100 kΩ. Leave the pin open when not in use. Parameter setting through the communication is performed by the pin use
10	PWM	Rotational control signal input pin. The rotational speed is controlled by duty-cycle of the pulse and is proportional to the duty-cycle ratio. Parameter setting through the communication is performed by this pin
11	TSL	Communication input selection and internal test mode pin. When short to GND, FG pin is serial in/out. When short to REG, PWM pin is serial in and FG pin is for serial out
12	GND	Internal circuit ground pin
13	RF	Sense resistor voltage input for current limit / over current protection
14	GPCDIS	O1H, O2H pull-up/down gate polarity check function disable (Low: enable, High: disable)
15	O2L	Low-side external power FET's gate drive output
16	O2H	High-side external power FET's gate drive output

Simplified Equivalent Circuit

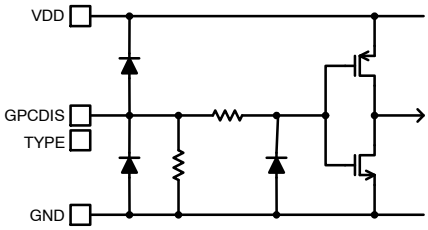
O1L, O2L



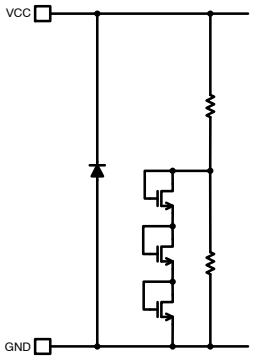
O1H, O2H



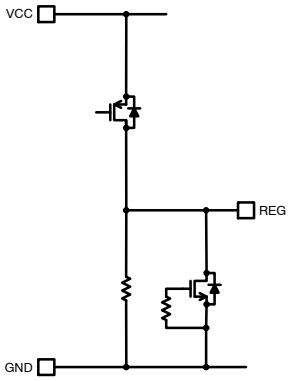
TYPE, GPCDIS



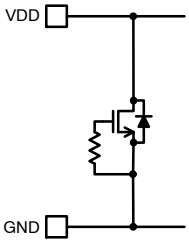
VCC/GND



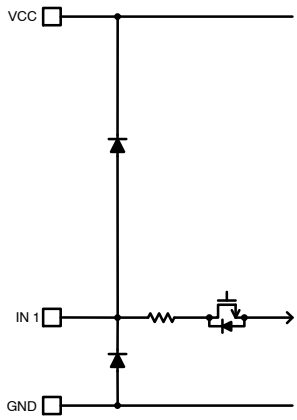
REG



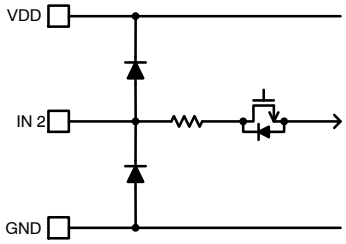
VDD



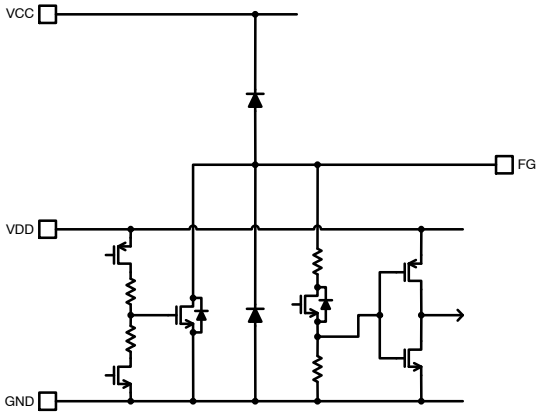
IN1



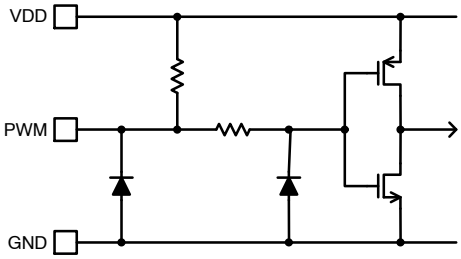
IN2



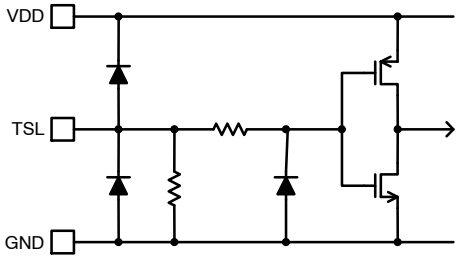
FG



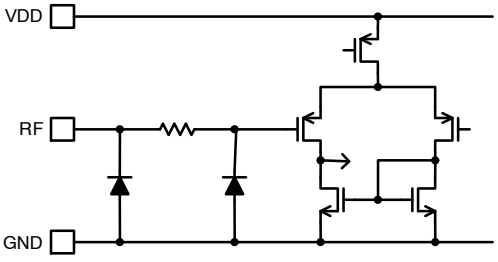
PWM



TSL



RF



OPERATION DESCRIPTION

The LV8310H has various functions and parameters which are defined by built-in registers. Refer to the Register map and description page for the detail.

Spin-up Sequence

To spin-up a motor, power is applied to VCC pin and the appropriate input PWM signal (see “DUTY_L” and “DUTY_S” setting description in section “Steady rotation”) is applied to PWM pin. The LV8310H starts driving the motor whose current direction is determined by the Hall sensor signal. To avoid the unnecessary rush current, the “soft start” mode is provided, which gradually increases output duty-cycle. After the soft start mode, LV8310H goes to steady rotation mode. The detail of the soft start mode and steady rotation mode are described in the sections below.

If a motor already rotates at the power on in faster speed than 304 rpm, the soft start mode is skipped and goes to steady rotation mode immediately.

Soft Start

For soft start mode, the duty-cycle ramp up profile is defined by the initial duty-cycle, slope, and exit condition. The initial duty-cycle is fixed and it starts from 4%. The slope is programmable. It is determined by registers “ENDPWM” and “INCTIM”. The duty-cycle is increased up to the end duty-cycle “ENDPWM” for duration time “INCTIM”. The end duty-cycle is selectable at 24% or 80% (see Table 10). The duration time can be selected from 0.0002 s to 15.2 s (see Table 11). The exit condition means it’s in the state of either the duty cycle reaching ”ENDPWM” or that the rotational speed is reaching the exit target speed specified by the register “RELLEV” (see Table 12). Soft start operation requires at least 8 electrical cycles (4 mechanical cycles in case of 4 poles single phase) independent on the exit condition.

Table 10. SOFT START END DUTY-CYCLE

ENDPWM	End Duty-cycle
0	24% output duty-cycle
1	80% output duty-cycle

Table 11. SOFT START DURATION TIME

INCTIM			Duration Time (s)	
[2]	[1]	[0]	ENDPWM = 1 (End Duty-cycle = 80%)	ENDPWM = 0 (End Duty-cycle = 24%)
0	0	0	0.15	0.0002
0	0	1	0.76	0.48
0	1	0	1.51	0.96
0	1	1	2.28	1.50
1	0	0	3.04	2.00
1	0	1	4.56	3.00
1	1	0	7.60	5.00
1	1	1	15.2	10.0

Table 12. SOFT START EXIT TARGET SPEED

RELLEV	Exit Target Speed
0	97% of target speed determined by input PWM duty-cycle
1	500 rpm

To avoid overshoot at the transition from soft start to the steady rotation mode, the release condition is set to 97% of the target speed in case of RELLEV=0.

Figure 5 and 6 show the image of soft start mode.

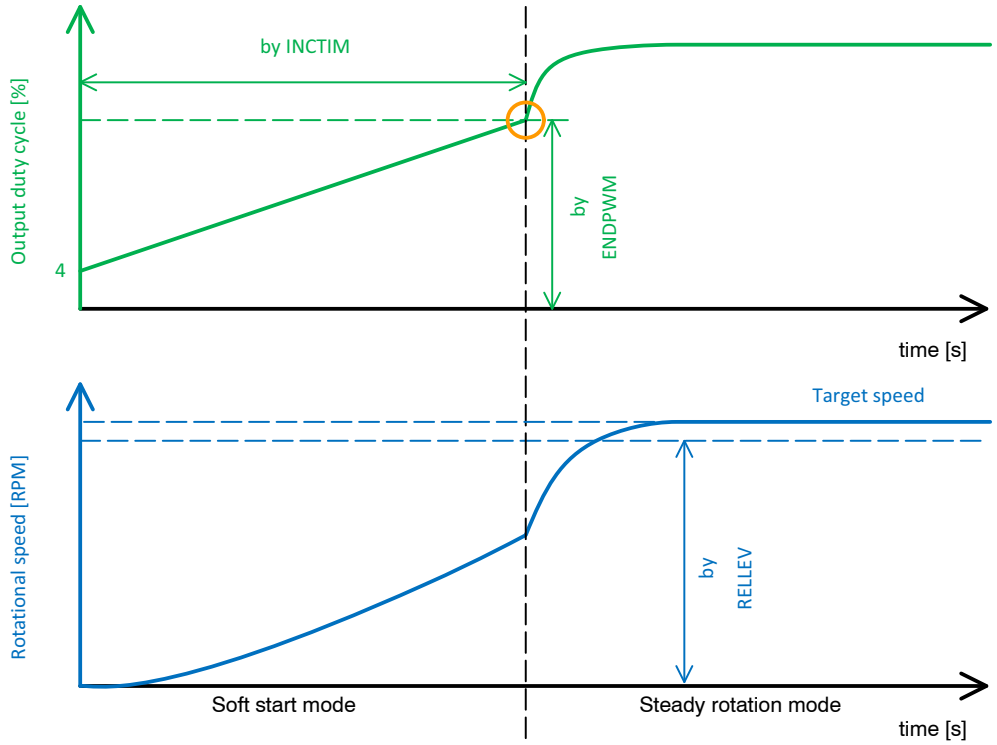


Figure 5. The Image of Soft Start Exit by End Duty-cycle

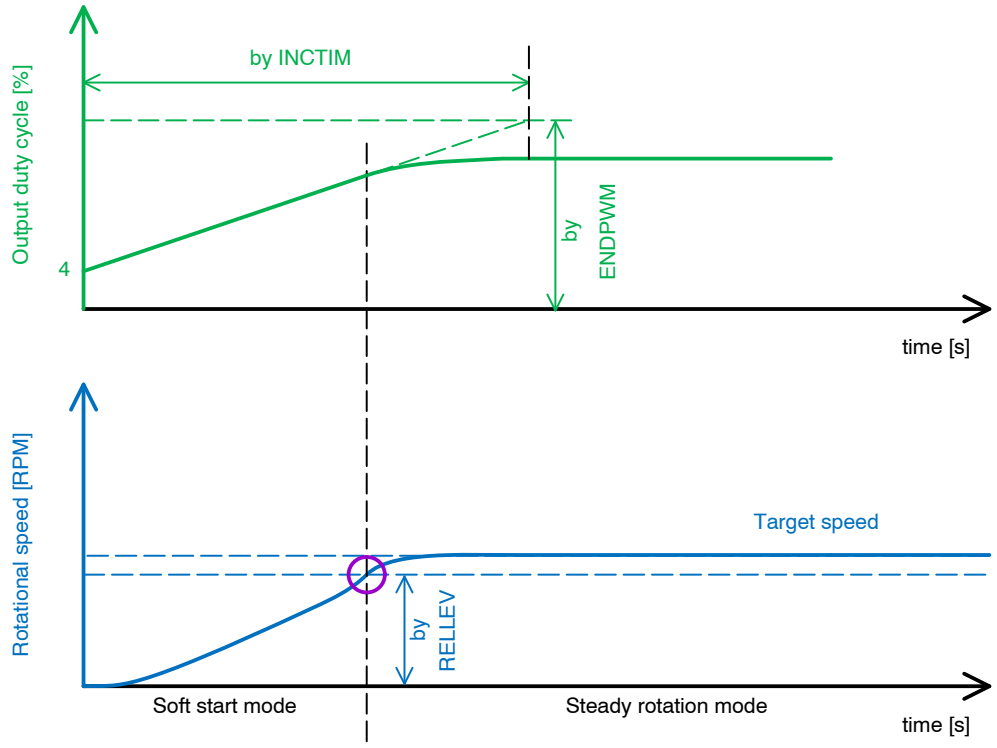


Figure 6. The Image of Soft Start Exit by Target Speed

As the green curve shown in Figure 5, the output duty-cycle in the soft start mode starts from 4% of the output duty. Then the output duty-cycle is increased to the end duty-cycle linearly, which is shown by yellow circle. After that, LV8310H goes to the steady rotation mode. Figure 6 shows the case which the rotational speed reaches the exit target speed before the output duty-cycle reaches to the exit condition.

Figure 7 is the example of the duration time in case of "ENDPWM = 0".

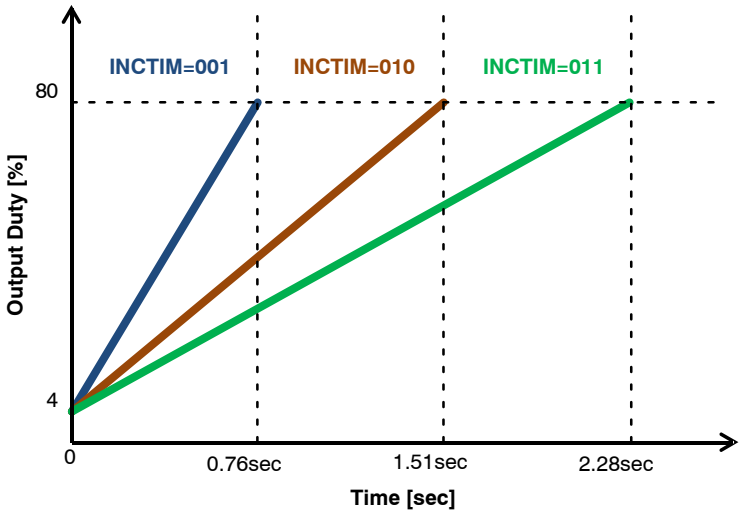


Figure 7. Example: The Image of Soft Start Duration Time

Steady Rotation

The rotational speed is controlled by built-in PI closed loop speed control function. The target rotational speed is defined by input PWM pin.

The input PWM frequency range is 25 Hz−100 kHz. The output frequency is fixed to 48 kHz and it is not related to input PWM frequency. Figure 8 shows the speed control profile which is relationship between input PWM duty-cycle and the target rotational speed. Registers to determine this relationship are;

- TAG_L (Address 0x0100 D [7:0]): Minimum target rotational speed
- TAG_H (Address 0x0101 D [7:0]): Maximum target rotational speed
- DUTY_L (Address 0x0102 D [7:0]): Minimum input duty-cycle
- DUTY_H (Address 0x0103 D [7:0]): Maximum input duty-cycle
- FULL (Address 0x0109 D [2]): Speed selection at input duty-cycle over DUTY_H
- DUTY_S (Address 0x0109 D [3:0]): Speed selection at input duty-cycle under DUTY_L

The detail of each register will be explained later.

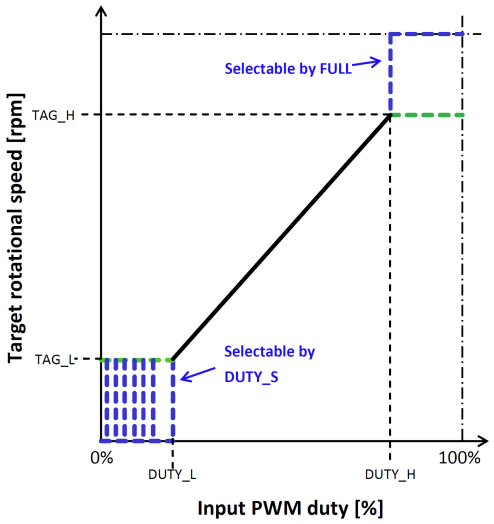


Figure 8. Speed Control Profile

TAG_L/TAG_H: Minimum/Maximum Target Rotational Speed Setting

The minimum speed is set by “TAG_L” and the maximum speed is set by “TAG_H” within the range of DUTY_L and DUTY_H. (See Figure 9.)

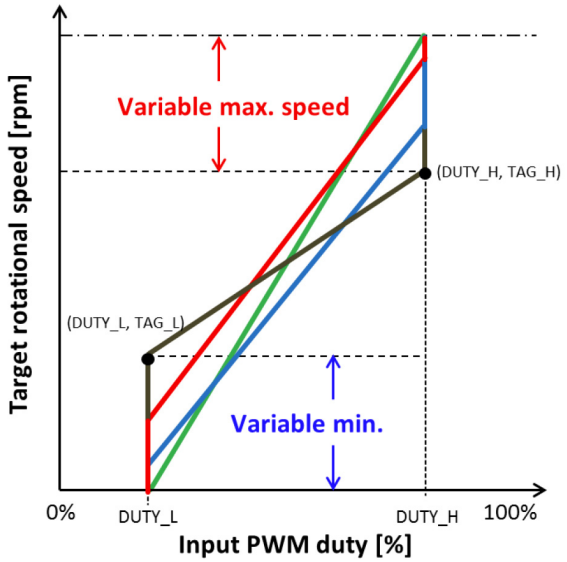


Figure 9. Max/Min Speed Setting

Table 13 and Table 14 show the list of RPM that can be used for speed setting.

Do not set the maximum speed setting (TAG_H) less than the minimum speed setting (TAG_L).

Table 13. MINIMUM ROTATIONAL SPEED SETTING TABLE FOR TAG_L

Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM
0x00	0	0x20	610	0x40	930	0x60	1380	0x80	2020	0xA0	3050	0xC0	4650	0xE0	7300
0x01	300	0x21	620	0x41	940	0x61	1400	0x81	2040	0xA1	3100	0xC1	4700	0xE1	7400
0x02	310	0x22	630	0x42	950	0x62	1420	0x82	2060	0xA2	3150	0xC2	4750	0xE2	7500
0x03	320	0x23	640	0x43	960	0x63	1440	0x83	2080	0xA3	3200	0xC3	4800	0xE3	7600
0x04	330	0x24	650	0x44	970	0x64	1460	0x84	2100	0xA4	3250	0xC4	4850	0xE4	7700
0x05	340	0x25	660	0x45	980	0x65	1480	0x85	2120	0xA5	3300	0xC5	4900	0xE5	7800
0x06	350	0x26	670	0x46	990	0x66	1500	0x86	2140	0xA6	3350	0xC6	4950	0xE6	7900
0x07	360	0x27	680	0x47	1000	0x67	1520	0x87	2160	0xA7	3400	0xC7	5000	0xE7	8000
0x08	370	0x28	690	0x48	1010	0x68	1540	0x88	2180	0xA8	3450	0xC8	5050	0xE8	8100
0x09	380	0x29	700	0x49	1020	0x69	1560	0x89	2200	0xA9	3500	0xC9	5100	0xE9	8200
0x0A	390	0x2A	710	0x4A	1030	0x6A	1580	0x8A	2220	0xAA	3550	0xCA	5150	0xEA	8300
0x0B	400	0x2B	720	0x4B	1040	0x6B	1600	0x8B	2240	0xAB	3600	0xCB	5200	0xEB	8400
0x0C	410	0x2C	730	0x4C	1050	0x6C	1620	0x8C	2260	0xAC	3650	0xCC	5300	0xEC	8500
0x0D	420	0x2D	740	0x4D	1060	0x6D	1640	0x8D	2280	0xAD	3700	0xCD	5400	0xED	8600
0x0E	430	0x2E	750	0x4E	1070	0x6E	1660	0x8E	2300	0xAE	3750	0xCE	5500	0xEE	8700
0x0F	440	0x2F	760	0x4F	1080	0x6F	1680	0x8F	2320	0xAF	3800	0xCF	5600	0xEF	8800
0x10	450	0x30	770	0x50	1090	0x70	1700	0x90	2340	0xB0	3850	0xD0	5700	0xF0	8900
0x11	460	0x31	780	0x51	1100	0x71	1720	0x91	2360	0xB1	3900	0xD1	5800	0xF1	9000
0x12	470	0x32	790	0x52	1110	0x72	1740	0x92	2380	0xB2	3950	0xD2	5900	0xF2	9100
0x13	480	0x33	800	0x53	1120	0x73	1760	0x93	2400	0xB3	4000	0xD3	6000	0xF3	9200
0x14	490	0x34	810	0x54	1140	0x74	1780	0x94	2450	0xB4	4050	0xD4	6100	0xF4	9300
0x15	500	0x35	820	0x55	1160	0x75	1800	0x95	2500	0xB5	4100	0xD5	6200	0xF5	9400
0x16	510	0x36	830	0x56	1180	0x76	1820	0x96	2550	0xB6	4150	0xD6	6300	0xF6	9500
0x17	520	0x37	840	0x57	1200	0x77	1840	0x97	2600	0xB7	4200	0xD7	6400	0xF7	9600
0x18	530	0x38	850	0x58	1220	0x78	1860	0x98	2650	0xB8	4250	0xD8	6500	0xF8	9700
0x19	540	0x39	860	0x59	1240	0x79	1880	0x99	2700	0xB9	4300	0xD9	6600	0xF9	9800
0x1A	550	0x3A	870	0x5A	1260	0x7A	1900	0x9A	2750	0xBA	4350	0xDA	6700	0xFA	9900
0x1B	560	0x3B	880	0x5B	1280	0x7B	1920	0x9B	2800	0xBB	4400	0xDB	6800	0xFB	10000
0x1C	570	0x3C	890	0x5C	1300	0x7C	1940	0x9C	2850	0xBC	4450	0xDC	6900	0xFC	10100
0x1D	580	0x3D	900	0x5D	1320	0x7D	1960	0x9D	2900	0xBD	4500	0xDD	7000	0xFD	10200
0x1E	590	0x3E	910	0x5E	1340	0x7E	1980	0x9E	2950	0xBE	4550	0xDE	7100	0xFE	10300
0x1F	600	0x3F	920	0x5F	1360	0x7F	2000	0x9F	3000	0xBF	4600	0xDF	7200	0xFF	10400

Table 14. MAXIMUM ROTATIONAL SPEED SETTING TABLE FOR TAG_H

Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM
0x00	300	0x20	940	0x40	2040	0x60	4700	0x80	10600	0xA0	17000	0xC0	23400	0xE0	29800
0x01	320	0x21	960	0x41	2080	0x61	4800	0x81	10800	0xA1	17200	0xC1	23600	0xE1	30000
0x02	340	0x22	980	0x42	2120	0x62	4900	0x82	11000	0xA2	17400	0xC2	23800	0xE2	30200
0x03	360	0x23	1000	0x43	2160	0x63	5000	0x83	11200	0xA3	17600	0xC3	24000	0xE3	30400
0x04	380	0x24	1020	0x44	2200	0x64	5100	0x84	11400	0xA4	17800	0xC4	24200	0xE4	30600
0x05	400	0x25	1040	0x45	2240	0x65	5200	0x85	11600	0xA5	18000	0xC5	24400	0xE5	30800
0x06	420	0x26	1060	0x46	2280	0x66	5400	0x86	11800	0xA6	18200	0xC6	24600	0xE6	31000
0x07	440	0x27	1080	0x47	2320	0x67	5600	0x87	12000	0xA7	18400	0xC7	24800	0xE7	31200
0x08	460	0x28	1100	0x48	2360	0x68	5800	0x88	12200	0xA8	18600	0xC8	25000	0xE8	31400
0x09	480	0x29	1120	0x49	2400	0x69	6000	0x89	12400	0xA9	18800	0xC9	25200	0xE9	31600
0x0A	500	0x2A	1160	0x4A	2500	0x6A	6200	0x8A	12600	0xAA	19000	0xCA	25400	0xEA	31800
0x0B	520	0x2B	1200	0x4B	2600	0x6B	6400	0x8B	12800	0xAB	19200	0xCB	25600	0xEB	32000
0x0C	540	0x2C	1240	0x4C	2700	0x6C	6600	0x8C	13000	0xAC	19400	0xCC	25800	0xEC	32200
0x0D	560	0x2D	1280	0x4D	2800	0x6D	6800	0x8D	13200	0xAD	19600	0xCD	26000	0xED	32400
0x0E	580	0x2E	1320	0x4E	2900	0x6E	7000	0x8E	13400	0xAE	19800	0xCE	26200	0xEE	32600
0x0F	600	0x2F	1360	0x4F	3000	0x6F	7200	0x8F	13600	0xAF	20000	0xCF	26400	0xEF	32800
0x10	620	0x30	1400	0x50	3100	0x70	7400	0x90	13800	0xB0	20200	0xD0	26600	0xF0	33000
0x11	640	0x31	1440	0x51	3200	0x71	7600	0x91	14000	0xB1	20400	0xD1	26800	0xF1	33200
0x12	660	0x32	1480	0x52	3300	0x72	7800	0x92	14200	0xB2	20600	0xD2	27000	0xF2	33400
0x13	680	0x33	1520	0x53	3400	0x73	8000	0x93	14400	0xB3	20800	0xD3	27200	0xF3	33600
0x14	700	0x34	1560	0x54	3500	0x74	8200	0x94	14600	0xB4	21000	0xD4	27400	0xF4	33800
0x15	720	0x35	1600	0x55	3600	0x75	8400	0x95	14800	0xB5	21200	0xD5	27600	0xF5	34000
0x16	740	0x36	1640	0x56	3700	0x76	8600	0x96	15000	0xB6	21400	0xD6	27800	0xF6	34200
0x17	760	0x37	1680	0x57	3800	0x77	8800	0x97	15200	0xB7	21600	0xD7	28000	0xF7	34400
0x18	780	0x38	1720	0x58	3900	0x78	9000	0x98	15400	0xB8	21800	0xD8	28200	0xF8	34600
0x19	800	0x39	1760	0x59	4000	0x79	9200	0x99	15600	0xB9	22000	0xD9	28400	0xF9	34800
0x1A	820	0x3A	1800	0x5A	4100	0x7A	9400	0x9A	15800	0xBA	22200	0xDA	28600	0xFA	35000
0x1B	840	0x3B	1840	0x5B	4200	0x7B	9600	0x9B	16000	0xBB	22400	0xDB	28800	0xFB	35200
0x1C	860	0x3C	1880	0x5C	4300	0x7C	9800	0x9C	16200	0xBC	22600	0xDC	29000	0xFC	35400
0x1D	880	0x3D	1920	0x5D	4400	0x7D	10000	0x9D	16400	0xBD	22800	0xDD	29200	0xFD	35600
0x1E	900	0x3E	1960	0x5E	4500	0x7E	10200	0x9E	16600	0xBE	23000	0xDE	29400	0xFE	35800
0x1F	920	0x3F	2000	0x5F	4600	0x7F	10400	0x9F	16800	0xBF	23200	0xDF	29600	0xFF	36000

DUTY_L/DUTY_H: Minimum/Maximum Input Duty-cycle Setting

The range of PWM input duty-cycle can be set by the registers “DUTY_L” and “DUTY_H” whose range is 0 to 100%. The equation of resolution is

$$D_{min} = \frac{DUTY\_L}{255} \times 100\ [\%] \qquad \text{(eq. 2)}$$

$$D_{max} = \frac{DUTY\_H}{255} \times 100\ [\%] \qquad \text{(eq. 3)}$$

Where:

D_{min} is minimum input duty-cycle

D_{max} is maximum input duty-cycle

Do not set “DUTY_H” less than “DUTY_L”.

Figure 10 shows the relationship between input duty-cycle and target rotational speed. TAG_L/TAG_H define the start and end points of the speed curve and the value between (DUTY_L, TAG_L) and (DUTY_H, TAG_H) are interpolated linearly.

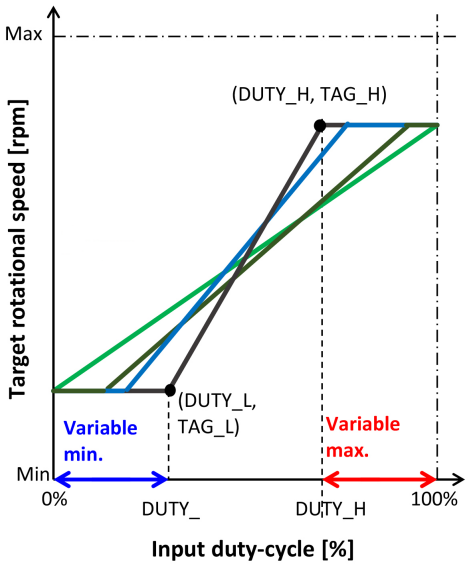


Figure 10. Input Duty-cycle Setting

FULL: Speed Selection at Input Duty-cycle over DUTY_H

For the behavior at input duty-cycle which is over DUTY_H, the register “FULL” provides two options. FULL = 0 is to keep the speed specified by “TAG_H” and FULL = 1 is to go to 100% output duty-cycle as shown in Figure 11.

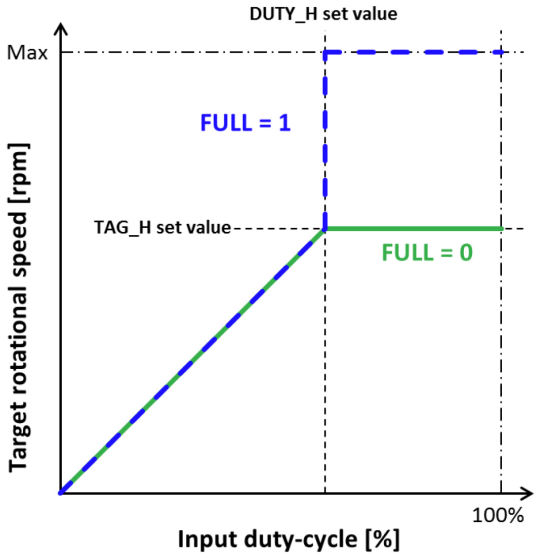


Figure 11. Max Speed Function Setting

DUTY_S: Speed Selection at Input Duty-cycle under DUTY_L

For the behavior at input duty-cycle less than DUTY_L, the register “DUTY_S” provides several options. The “DUTY_S” sets the input duty cycle of the motor speed to 0 rpm. It is calculated by Equation 4, except for the case of “DUTY_S” = 15.

$$D_0 = \frac{5 \times \text{DUTY\_S}}{255} \times 100\ [\%] \qquad \text{(eq. 4)}$$

Where D_0 is input duty-cycle of the motor speed 0 rpm

Table 15 shows the option of “DUTY_S”.

- When DUTY_S = 15, the threshold duty-cycle is same as the “DUTY_L” setting.
- When DUTY_S = 1 to 14, the motor speed keeps “TAG_L” setting from “DUTY_L” to “DUTY_S” and goes to 0 rpm at defined by Equation 4.
- When DUTY_S = 0, the motor speed keeps “TAG_L” setting whenever input duty-cycle is less than “DUTY_L”.
- If “DUTY_L” setting is smaller than “DUTY_S” setting, the threshold is same as “DUTY_L” setting.

To restart the motor rotation, the input duty-cycle must be set higher than “DUTY_S” + 1.6% (i.e. the hysteresis is 1.6%).

Figure 12 shows the speed curves for various “DUTY_S”.

Table 15. THE SETTING OF DUTY_S

DUTY_S	Motor Stop Duty Setting (%)
0	0
1	1.9
2	3.9
3	5.8
4	7.8
5	9.8
6	11.7
7	13.7
8	15.6
9	17.6
10	19.6
11	21.5
12	23.5
13	25.4
14	27.4
15	The value of DUTY_L

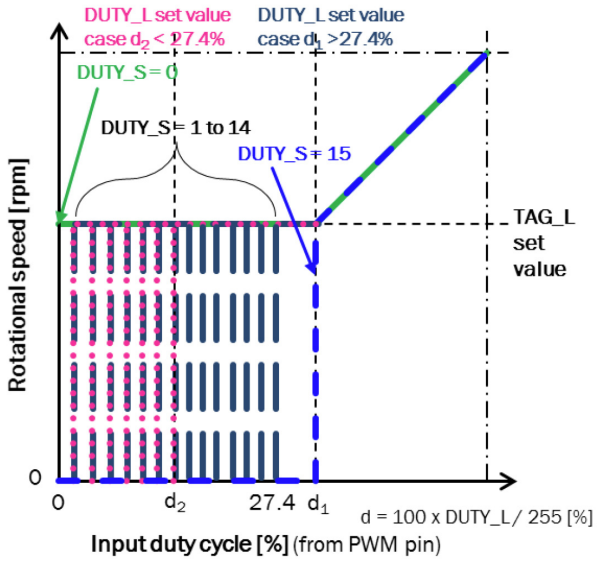


Figure 12. Min Speed Function Setting Image

Output Waveform

The output pulse signal is about 0 V – VCC and its duty is controlled by built-in PI closed loop speed control function. The duty before commutation change decreases gradually to 0% and the duty after commutation change increases gradually to the duty level controlled by speed control function by built-in function called Soft Switch. The state is shown in Figure 13 as a schematic view.

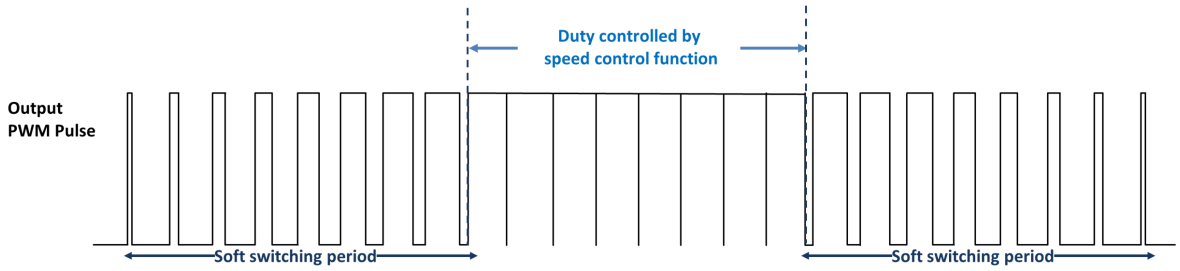


Figure 13. Output Waveform Image

Soft Switch Setting

The LV8310H can adjust Soft switch period as the ratio of L and S shown in Figure 14. It is defined by Equation 5 and Register “SSWHIGH” and “SSWLOW” can adjust it.

$$\text{Soft switch width [\%]} = \frac{S}{L} \times 100 \quad \text{(eq. 5)}$$

Where:

S is Soft Switch period

L is one commutation period

Figure 14 shows the Soft Switch image.

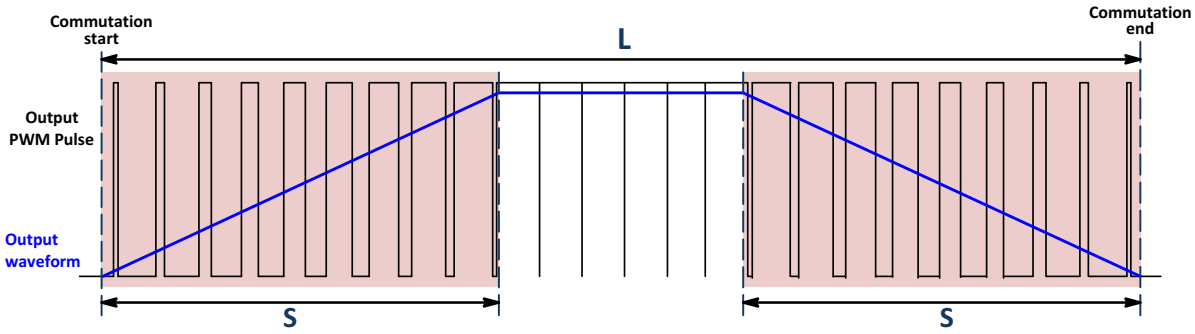


Figure 14. Soft Switch Image

SSWHIGH is for the maximum target rotational speed defined by TAG_H and SSWLOW is for the minimum target rotational speed defined by TAG_L. Each register has 4bits and Table 16 shows the adjustable value.

Table 16. SOFT SWITCH WIDTH ADJUSTMENT

Register	S/L ratio	Register	S/L ratio
0000	2.9%	1000	26.4%
0001	5.9%	1001	29.3%
0010	8.8%	1010	32.2%
0011	11.7%	1011	35.2%
0100	14.6%	1100	38.1%
0101	17.6%	1101	41.0%
0110	20.5%	1110	43.9%
0111	23.4%	1111	46.9%

Once “SSWHIGH” and “SSWLOW” are set, the ratio of Soft Start in other speed is interpolated as shown in Figure 15.

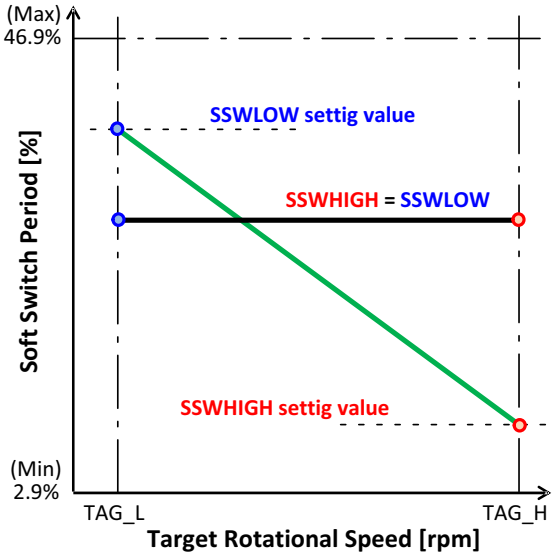


Figure 15. The Relationship Between Soft Switch and Target Rotational Speed

FG Output

FG signal output is decided by the Hall signal cross point. The relationship between motor speed and FG frequency represents the following equation.

$$f_{FG}\,[Hz] = \frac{N}{60} \times \frac{p}{2} \qquad \text{(eq. 6)}$$

Where:

N: Motor speed [rpm]

p: Number of Pole.

Figure 16 shows the timing chart of the hall sensor output and the FG output.

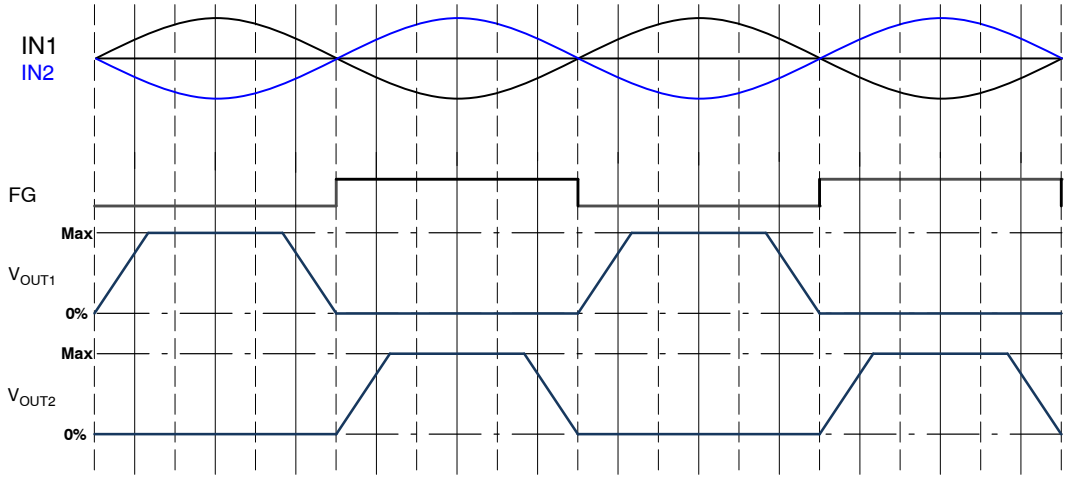


Figure 16. Timing Chart of Output

Lead-angle Setting

In the output, the output current delays from the output voltage because of the inductance of motor coil. The output current which flows in a motor coil generates torque for the motor and the torque is maximized by the synchronization of output current with the BEMF phase. Therefore, this delay decreases an efficiency of motor rotation. It is generally increased in proportion to the rotational speed.

The LV8310H can cancel the delay by earlier commutation than the Hall sensor signal as shown in Figure 17. This phase adjustment is called “Lead-angle”.

In Figure 17, the output voltage VOUT1 and the output current IOUT1 in black are changed to the waveform in red after the Lead-angle adjustment and it is the most optimum commutation timing.

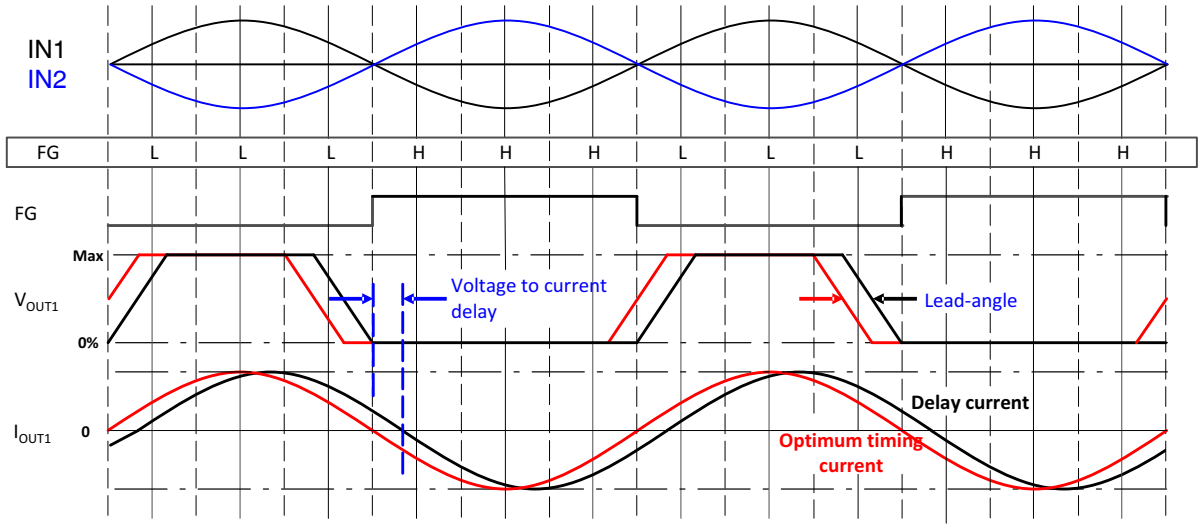


Figure 17. The Relationship Between the Lead-Angle and the Delay of Output Current

The relationship between rotational speed and Lead-angle is shown in Figure 18. The optimum Lead−angle will vary by the motor characteristics so it is necessary to adjust the Lead−angle based on the motor in use

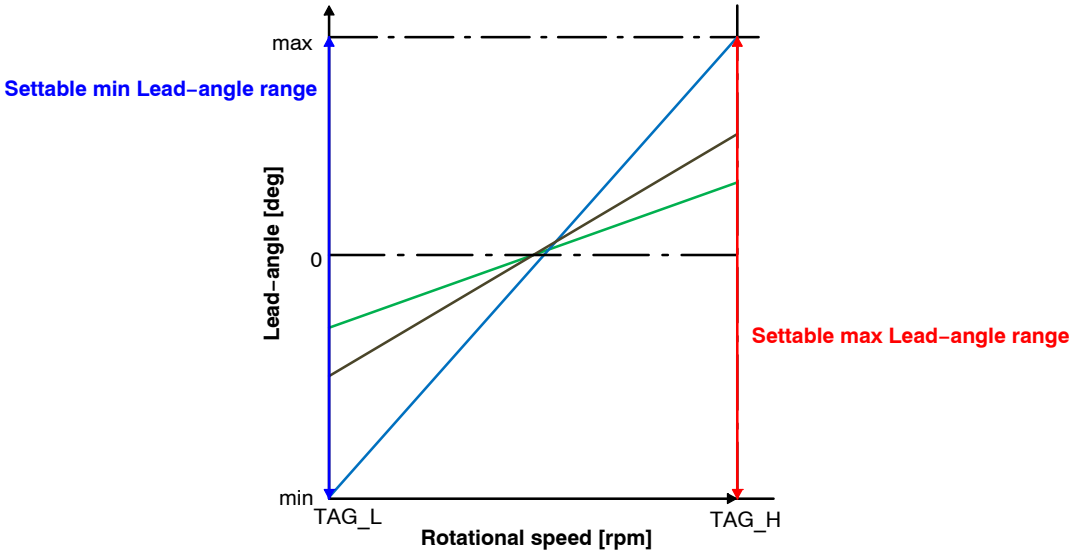


Figure 18. Lead-Angle Curve Image

The LV8310H can set the Lead-angle at maximum target rotational speed (TAG_H) and at minimum target rotational speed (TAG_L) by “DLDEG_H” and “DLDEG_L” individually.

These register have 8 bits D[7:0] in each and both MSBs define the direction of phase delay. When MSB sets to “0”, the Lead-angle is set to minus value which means phase delay, that is, the output voltage commutation is delay than the Hall sensor signal. When MSB sets to 1, the Lead-angle is set to plus value which means phase advance, that is, the output voltage commutation is earlier than the Hall sensor signal. The resolution is approximately 0.175°. Hence, the adjustable range is from −22.225° to 22.225° expressed in the following equation.

$$L_{max} = \frac{22.225}{127} \times \text{DLDEG\_H [deg]} \quad \text{(eq. 7)}$$

$$L_{min} = \frac{22.225}{127} \times \text{DLDEG\_L [deg]} \quad \text{(eq. 8)}$$

Where:

Lmax: Lead-angle at maximum target rotational speed (TAG_H)

Lmin: Lead-angle at minimum target rotational speed (TAG_L)

Once DLDEG_H and DLDEG_L are set, the Lead-angle in other speed is set to interpolated and extrapolated value according to the rotational speed, even though the rotational speed is defined by FULL = 1.

Protections

The LV8310H has the following protection functions

- TSD (Thermal Shut Down)
- UVLO (Under Voltage Lock Out)
- Lock protection
- CLM (Current Limiter)
- OCP (Over Current Protection)
- GPC (Gate Polarity Check)

When the TSD or Lock protection works, all of the FETs are turned off. When UVLO or CLM works, the output PWM is off and the motor goes to re-circulation mode.

Thermal Shutdown Protection (TSD)

When LV8310H junction temperature rises to 180°C, TSD will activate and turn off high-side and low-side Power FET. Therefore, OUT1 and OUT2 will become high impedance and the coil current will shut off. When it falls under 140°C, TSD will deactivate and motor will start to rotate.

The TRUTH TABLE of TSD is as shown in Table 17.

Table 17. TSD TRUTH TABLE

Operating Voltage	State of TYPE Pin	O1H	O1L	O2H	O2L
12 V	Low (GND)	H	L	H	L
24 V, 48 V	High (5 V)	L	L	L	L

Under Voltage Lock Out (UVLO)

When VCC voltage goes to low level (3.4 V), UVLO will activate and stop the motor. It is cleared when VCC voltage is recovered to above 3.6 V. The TRUTH TABLE of UVLO is as shown in Table 18.

Table 18. UVLO TRUTH TABLE

Input			Register	Output			
TYPE	IN1	IN2	DRVMODE	O1H	O1L	O2H	O2L
L	L	H	00 / 01	H	H	H	L
L	H	L	00 / 01	H	L	H	H
H	L	H	00 / 01	L	H	L	L
H	H	L	00 / 01	L	L	L	H
L	L	H	10 / 11	H	L	L	L
L	H	L	10 / 11	L	L	H	L
H	L	H	10 / 11	L	L	H	L
H	H	L	10 / 11	H	L	L	L

Lock Detection and Lock Protection

When the motor is locked, the heat is continuously generated because the IC keeps trying to rotate the motor.

The lock protection works to prevent such a heat generation by turning off the motor current. The TRUTH TABLE of Lock Protection is as shown in Table 19. When a motor is locked in the steady rotation mode and IC doesn't detect the FG edge for more than 0.3 s which is equivalent to 50 rpm, the lock protection works (Figure 19).

The lock protection signal can be output from FG pin by setting the register "TACHSEL". Please see Table 26. In this mode, the RD signal goes to "High", though it is "Low" at motor starts.

When the motor restarts and IC detects 4 phase changes at least (depends on rotation speed), the RD signal goes to "Low".

Table 19. LOCK PROTECTION TRUTH TABLE

Operating Voltage	State of TYPE Pin	O1H	O1L	O2H	O2L
12 V	Low (GND)	H	L	H	L
24 V, 48 V	High (5 V)	L	L	L	L

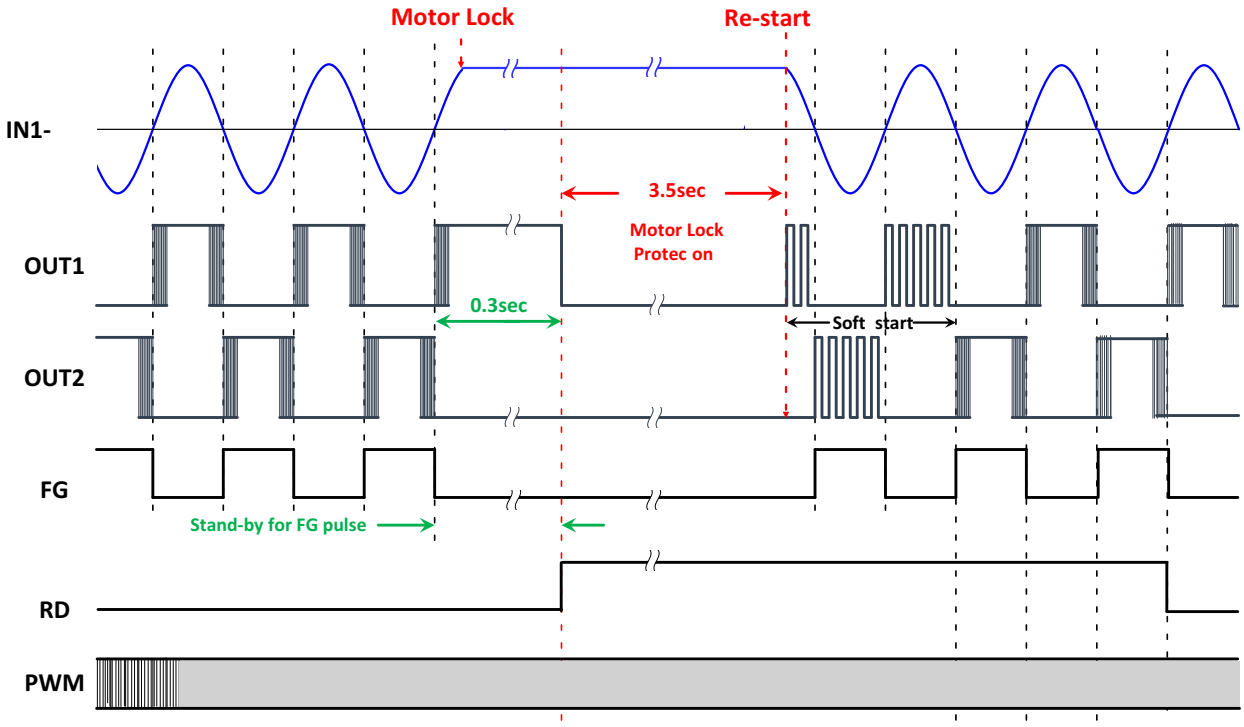


Figure 19. Timing Chart of the Lock Protection

Figure 20 shows the relationship between protection period and the number of protection times. 1st to 4th protection period take 3.5 s and 5th protection period takes 14 s. To reset the lock protection mode, Stop duty cycle must be applied to the PWM input signal. To retry the motor rotation, Proper duty cycle must be applied to the PWM input signal.

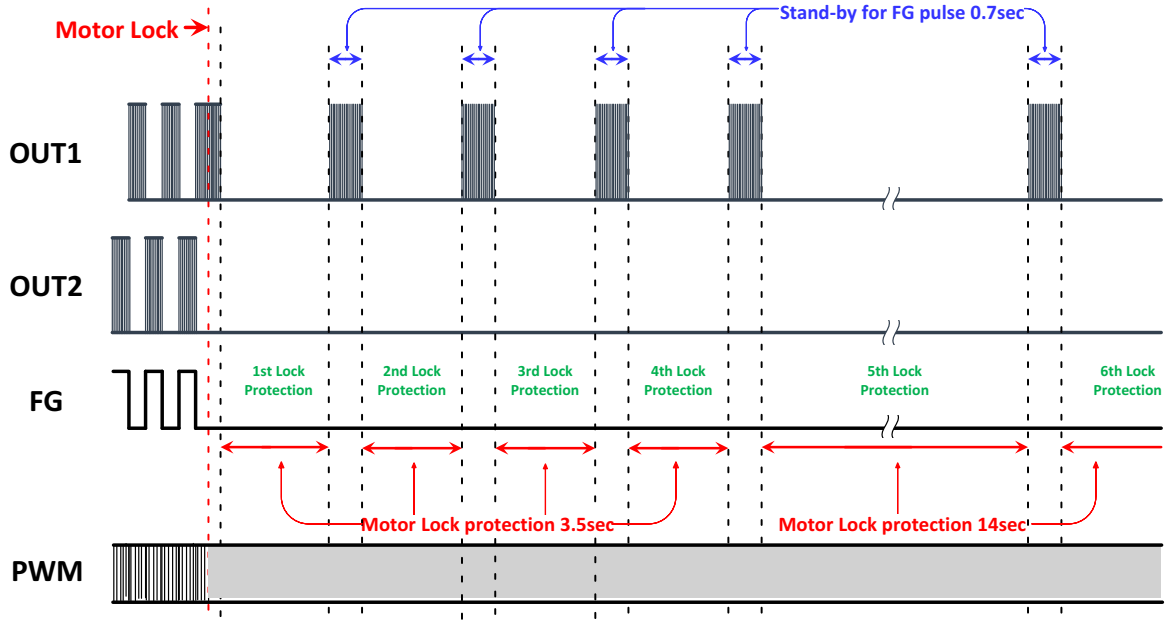


Figure 20. The Relationship Between Protection Time and the Number of Protection Time

These protection periods and the number of protection times are applied in accordance with the internal counter. It will reset the counter if the duty−cycle which sets the motor speed to 0 rpm determined by “DUTY_L” and “DUTY_S” is entered during lock protection period (in either 3.5 sec or 14 sec). In this case, the lock protection counter will activate from the initial state starting from PWM Pos−Edge and protection period will start from 1st time as shown in Figure 21 and Figure 22.

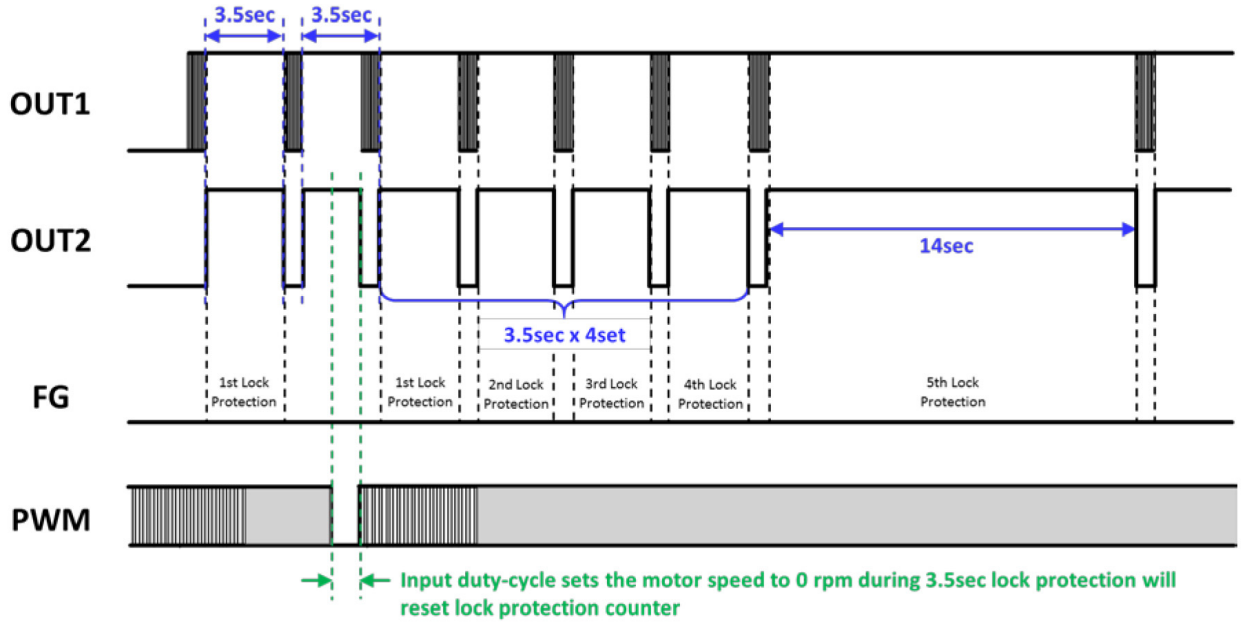


Figure 21. Lock protection counter reset during 3.5 sec lock protection period

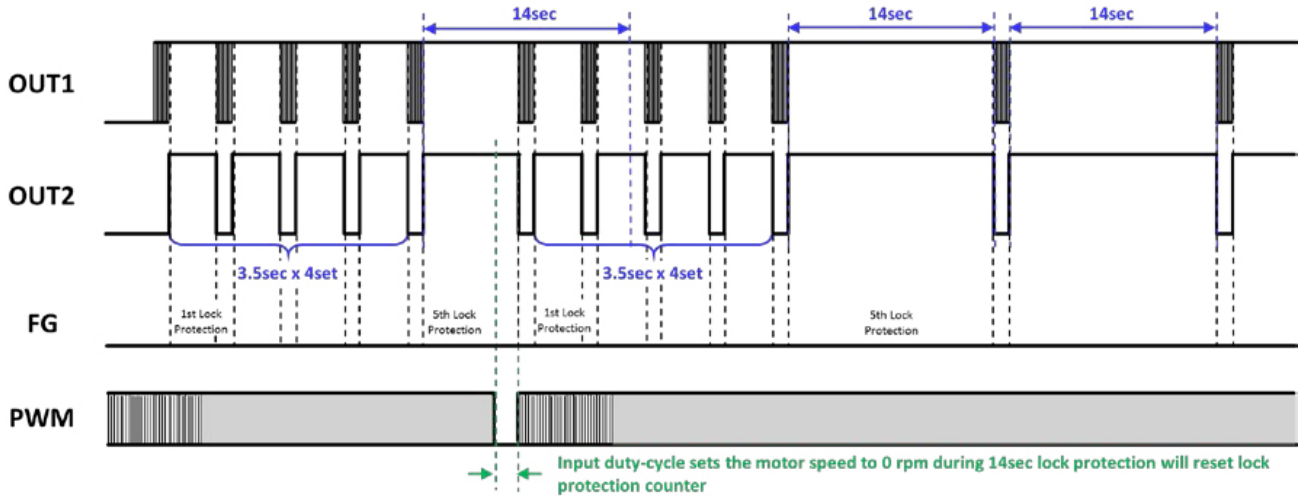


Figure 22. Lock protection counter reset during 14 sec lock protection period

The lock protection period is changed by the condition of output signal. If the duty−cycle which sets motor speed to 0 rpm is input and the output signals are disappeared during the restart period in lock protection period as shown in light blue in Figure 23, the counter is not reset and the remaining restart period is applied immediately when PWM Pos−Edge will be input as shown in pink in Figure 23. In this case, the protection period is not related to the internal lock protection timer and protection period is not fixed to 3.5 sec or 14 sec.

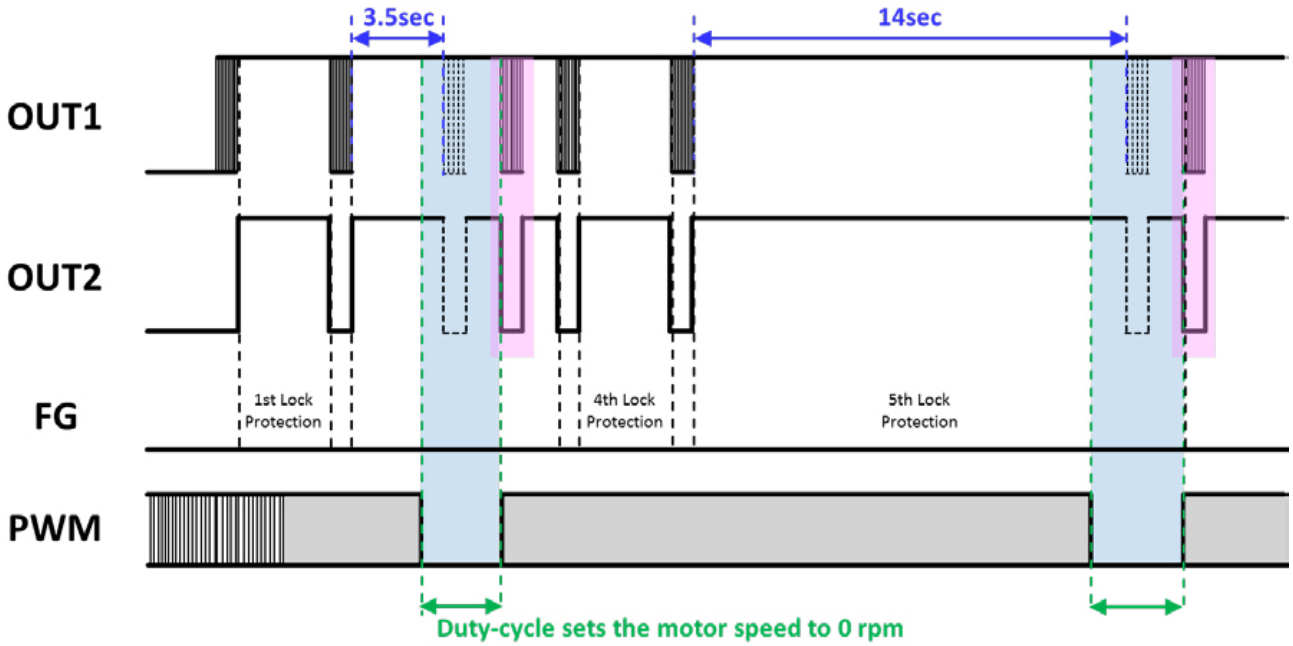


Figure 23. In case of having changes in protection period

Current Limiter (CLM)

When the coil current becomes large, CLM will activate and then output will be in the re-circulation state. The current is monitored by RF pin and the threshold is 100 mV.

There are three registers related to the current limiter function. The first one is CL_SKIP which can set the period of protection operation when CL is detected. The second one is CL_ASYNC. When “1” is set to this register while CL is active, synchronous rectification of the output becomes disabled. The third one is OCP_MASK which sets the masking time to ignore upper and lower FET’s reverse recovery. See Table 26 for more details.

Overcurrent Protection (OCP)

OCP monitors the coil current by RF pin and if it becomes larger than 150 mV even if CLM is activated, OCP will activate and motor driver will stop. The TRUTH TABLE of OCP is as shown in Table 20.

Register called OCP_LAT_CLR allows to select behavior when OCP is activated. One is to keep the motor stopped until the next power on sequence, and the other one is to activate Lock protection mode. See Table 26 for more details.

Table 20. OCP TRUTH TABLE

Operating Voltage	State of TYPE Pin	O1H	O1L	O2H	O2L
12 V	Low (GND)	H	L	H	L
24 V, 48 V	High (5 V)	L	L	L	L

Gate Polarity Check

The LV8310H can handle both 12 V and higher voltage (24 V/48 V) application by TYPE pin setting. The TYPE pin sets to GND for 12 V application and it sets to VDD for higher voltage application. In case of 12 V application, O1H and O2H pin must be pulled up to VCC via a resister and in the other case, they must be pulled down to GND via a resister. For the detail, please see the application circuit on Figure 1 and Figure 2. If these polarities setting is incorrect, shoot-through current is occurred and has possibility to break down the output FETs.

Gate Polarity Check (GPC) checks the polarity and the voltage of the O1H and O2H at the device power on. If the check result is incorrect, GPC turns both O1L and O2L into Low to prevent FET from breaking down by shoot through current. The TRUTH TABLE when GPC error is posted is shown as Table 21. Because GPC checks it in power up sequence, it is no affects if noise is generated to TYPE and GPCDIS pin after the motor starting. The IC only keeps this error status until power off.

Table 21. GPC TRUTH TABLE

Operating Voltage	State of TYPE Pin	O1H	O1L	O2H	O2L
12 V	Low (GND)	H	L	H	L
24 V, 48 V	High (5 V)	L	L	L	L

GPC is ignored when GPCDIS pin is pulled up to 5 V.

Nonvolatile Memory

The LV8310H has internal nonvolatile memory which can store register values which define various parameters and settings. The stored register values will be reloaded at POR shown as Figure 24. LV8310H has also the communication mode. It allows user to modify register values, and to store them to the nonvolatile memory (Figure 24). It doesn't need the resistors as like the conventional models to set the various review. In addition, PCB design becomes simpler.

Here is a list of the main configurable items.

- Max/Min rotational speed.
- Max/Min input duty-cycle.
- Lead-angle
- Soft start
- Speed control slope

Program/Erase to the memory is performed through a built-in register. Please note that Program/Erase is allowed for 10 times only. For more detail, please see the application note "NVM Programming Procedure".

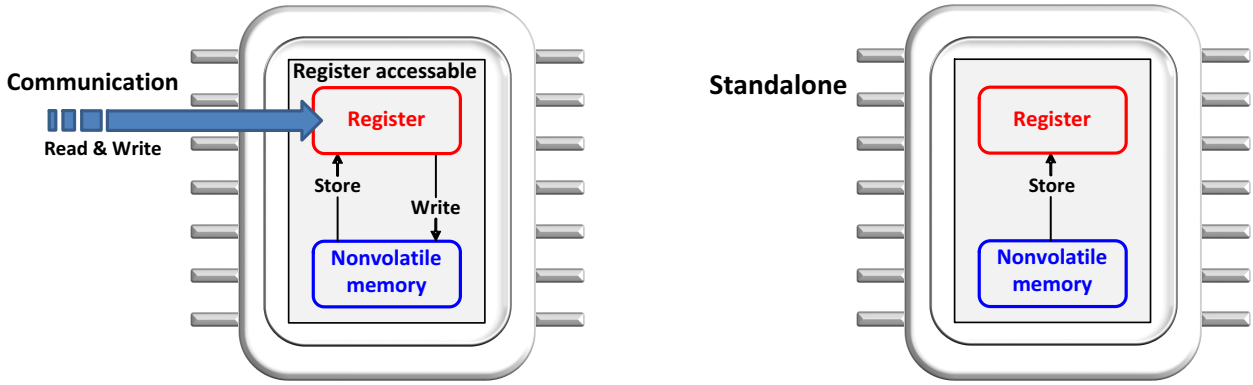


Figure 24. Image of the Internal Register and Nonvolatile Memory

Serial Interface

The LV8310H allows communication via UART (Universal Asynchronous Receiver Transmitter). Various parameter registers can be accessed through UART communication.

UART is one to one communication and the LV8310H doesn't support parallel access to the multiple devices, so be sure to turn on only the target devices.

The LV8310H provides two UART modes, a one-wire mode and a two-wire mode. In one-wire mode, the FG pin is used for both input and output. In two-wire mode, the FG pin is used as output and the PWM pin is used as input. The state of the TSL pin defines the UART mode as shown in Table 22.

Table 22. I/O PIN CONDITION IN UART MODE

	One−wire Mode	Two−wire Mode
TSL Pin	Pull down (GND)	Pull-up (VDD)
Communication Pin	FG pin (For Read and Write)	PWM pin (For Write) FG pin (For Read)

Figure 25 shows the connection image of one-wire mode. The communication line FG should be open-drain type because it supports duplex mode. Therefore the communication pin of the MPU or CPU must be an open-drain output. Figure 26 shows the connection image of two−wire mode. Please refer to the Application note AND9761/D for more detail.

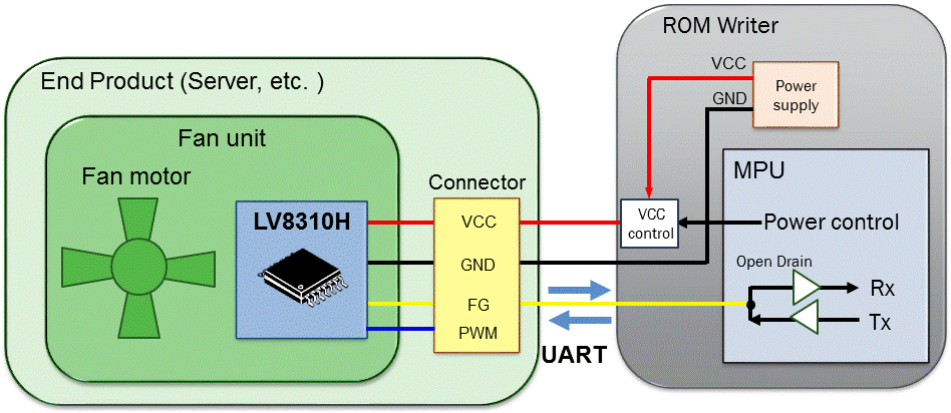


Figure 25. Connection Image of One-wire Mode

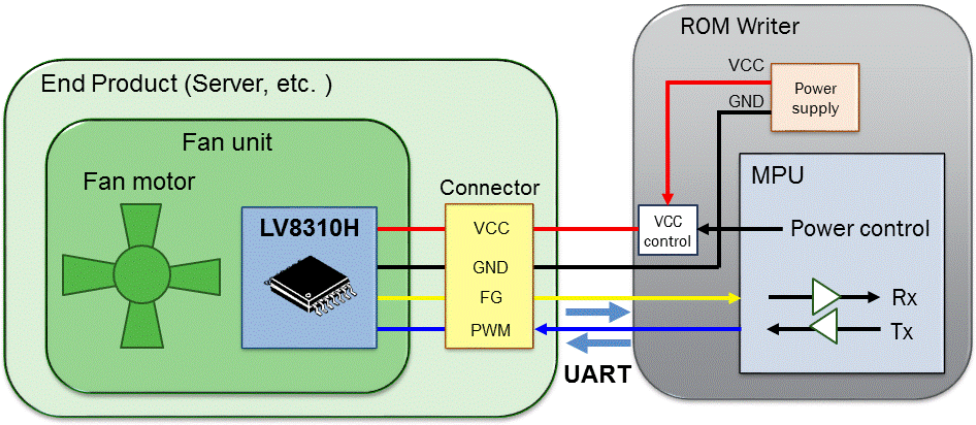


Figure 26. Connection Image of Two-wire Mode

About the detail of communication protocol, please see the Application note, AND9761/D.

REGISTER MAP

Internal register map can be classified into four types as shown in Table 23.

- Read only
- Read/Write, User defined registers to be written to nonvolatile memory.
- Read/Write
- Write only (Auto clear)

Table 23. REG. MAP 1 (Address 0x0000 – 0x0114)

Address	Initial	Register							
		D7	D6	D5	D4	D3	D2	D1	D0
0x0000	0xAA	1	0	1	0	1	0	1	0
0x0001	0x55	0	1	0	1	0	1	0	1
0x0002	0x00					0	0	RECALC_EN	RELOAD_EN
0x0003	0x00								RELOAD
0x0004	0x00								RECALC
0x0005	0xB8	Identification number							
0x0100	0x15	TAG_L[7:0]							
0x0101	0x63	TAG_H[7:0]							
0x0102	0x19	DUTY_L[7]	DUTY_L[6:0]						
0x0103	0x65	DUTY_H[7]	DUTY_H[6:0]						
0x0104	0x00	DLDEG_L[7:0]							
0x0105	0x8B	DLDEG_H[7:0]							
0x0106	0x6F	SSWHIGH[3:0]				SSWLOW[3:0]			
0x0107	0x01					0	PWMIN_INV	DRVMODE[1:0]	
0x0108	0x0A	DWNSET	FULL	SS_SW_SEL	RELLEV	ENDPWM	INCTIM[2:0]		
0x0109	0x0F					DUTY_S[3:0]			
0x010A	0x01							DTIME[1:0]	
0x010B	0x0E				0	CL_SKIP	CL_ASYNC	OCP_LAT_CLR	STEPSEL
0x010C	0x00							TACHSEL[1:0]	
0x010D	0x02							PWMAV[1:0]	
0x010E	0x00					0	0	OCP_MASK[1:0]	
0x010F	0x00			0	0	0	0	ON_INTERNAL	0
0x0110	0x00					LOCK_FAULT	0	0	0
0x0111	0x20	MSKDEG_TP[3:0]				0	0	0	0
0x0112	NA	RESERVED							
0x0113	0xB0	IX[3:0]				0	IG[2:0]		
0x0114	0x20	0	PX[2:0]			0	PG[2:0]		

Table 24. REG. MAP 2 (Address 0x0219)

Address	Initial	Register							
		D7	D6	D5	D4	D3	D2	D1	D0
0x0219	0x00		SWI_ERR[6:0]						

Registers in the black cells do not exist. Therefore, these registers cannot be written and the read values are always zero. The bits with numeric values (0 or 1) must remain as−is.

There are some register addresses which contain both the bits stored in NVM and the bits not stored in NVM. Confirm the bit types to save the data to NVM.

Table 25. REGISTER ADDRESS 0X0000−0X0005 REGISTER DESCRIPTION 1

Function	Address	Bits	Register Name	Description
Fixed register 1	0x0000	[7:0]	−	Data of 0xAA are stored. (Read only)
Fixed register 2	0x0001	[7:0]	−	Data of 0x55 are stored. (Read only)
Enable re-calculation	0x0002	[1]	RECALC_EN	This register enables re-calculation of Speed/Lead Angle/Soft SW setting. 0: Disable 1: Enable
Register re-loading (memory to register)	0x0002	[0]	RELOAD_EN	This register enables data reloading from NVM. 0: Disable 1: Enable
Register re-loading (memory to register)	0x0003	[0]	RELOAD	When this bit is set to 1, data reloading from NVM is executed while RELOAD_EN is set to 1. This register is auto clear type.
Trigger of re-calculation	0x0004	[0]	RECALC	When this bit is set to 1, re-calculation of Speed/Lead Angle/Soft SW setting is executed while RECALC_EN is set to 1. This register is auto clear type.
Device ID	0x0005	[7:0]	ID_NUMBER	Data of device ID are stored. (Read only)

Table 26. REGISTER ADDRESS 0X0100−0X0114 REGISTER DESCRIPTION 2

Function	Address	Bits	Register Name	Description
Minimum speed setting	0x0100	[7:0]	TAG_L	These registers set minimum/maximum rotational speed. 0000 0000: 0/300rpm (Min / Max) 1111 1111: 10400/36000rpm (Min / Max) * Refer to the section “Steady Rotation” for details.
Maximum speed setting	0x0101	[7:0]	TAG_H	
Minimum input duty cycle setting	0x0102	[7:0]	DUTY_L	This register sets minimum input duty-cycle. 0000 0000: Duty 0% 0111 1111: Duty 49.8%
Maximum input duty cycle setting	0x0103	[7:0]	DUTY_H	This register sets maximum input duty-cycle. 1000 0000: Duty 50.2% 1111 1111: Duty 100%
Lead-angle setting at minimum speed	0x0104	[7:0]	DLDEG_L	This register adjusts Lead-angle at rotational speed set by TAG_L. 000 0000: 0 degree, 111 1111: −22.225 deg (DLDEG_L[7] = 0) 000 0000: 0 degree, 111 1111: +22.225 deg (DLDEG_L[7] = 1)
Lead-angle setting at maximum speed	0x0105	[7:0]	DLDEG_H	This register adjusts Lead-angle at rotational speed set by TAG_H. 000 0000: 0 degree, 111 1111: −22.225deg (DLDEG_H[7] = 0) 000 0000: 0 degree, 111 1111: +22.225deg (DLDEG_H[7] = 1)
Soft switch width setting at maximum speed	0x0106	[7:4]	SSWHIGH	Soft switch width is set at rotational speed set by TAG_H. 0000: equivalent to 2.9% of a commutation period 1111: equivalent to 46.9% of a commutation period

Table 26. REGISTER ADDRESS 0X0100−0X0114 REGISTER DESCRIPTION 2 (continued)

Function	Address	Bits	Register Name	Description
Soft switch width setting at minimum speed	0x0106	[3:0]	SSWLOW	Soft switch width is set by the rotational speed set by TAG_L setting. 0000: equivalent to 2.9% of a commutation period 1111: equivalent to 46.9% of a commutation period
Speed control slope invert	0x0107	[2]	PWMIN_INV	Control slope polarity for input duty-cycle is changed. 0: Normal mode (Low duty-cycle is low speed rotation) 1: Invert mode (Low duty-cycle is high speed rotation)
Sync/Async drive select	0x0107	[1:0]	DRVMODE	This register selects synchronous / asynchronous drive. 00: High-side switching is PWM. Low-side switching is asynchronous 01: High-side switching is PWM. Low-side switching is synchronous 10: High-side switching is asynchronous. Low-side switching is PWM 11: High-side switching is synchronous. Low-side switching is PWM
Sync-drive stop mode (deceleration)	0x0108	[7]	DWNSET	This register selects drive mode when the target speed is less than 80% of the actual motor speed. *When receives control less than 80% of existing speed. 0: Normal (Synchronization drives are always maintained) 1: It is changed to asynchronous drive in speed decrease
Maximum speed setting 2	0x0108	[6]	FULL	This register defines the output behavior when input PWM is greater than the duty cycle set by DUTY_H. 0: Fixed speed set by TAG_H 1: Fixed duty cycle of 100% with soft switch
Soft switch mask time select	0x0108	[5]	SS_SW_SEL	This register sets soft switch period in soft start mode. 0: Rise 2.5 ms, Fall 5 ms 1: Rise 1.25 ms, Fall 2.5 ms
Soft start release condition	0x0108	[4]	RELLEV	This register selects rotational speed of soft start exit condition. 0: When rotational speed arrives at 97% of the target speed. 1: When rotational speed arrives at 500 rpm.
Soft start release condition	0x0108	[3]	ENDPWM	This register selects max output duty-cycle of soft start release condition. 0: Max output duty-cycle is 24% 1: Max output duty-cycle is 80%
Soft start release time	0x0108	[2:0]	INCTIM	This register sets the soft start duration time.
Minimum speed setting 2	0x0109	[3:0]	DUTY_S	This register sets the various speed when input duty-cycle is less than DUTY_L.
Dead Time setting	0x010A	[1:0]	DTIME	This register sets dead time in synchronous rectification drive. 00: 125 ns 01: 250 ns 10: 500 ns 11: 0 ns
Disable period of motor current in CLM	0x010B	[3]	CL_SKIP	This register sets disable period of motor current when CLM is active. 0: Only for corresponding PWM pulse 1: For corresponding and next PWM pulse
Disable motor synchronous rectification in CLM	0x010B	[2]	CL_ASYNC	This register disables motor synchronous rectification when CLM is active. 0: Synchronous rectification is not disable when CLM is active 1: Synchronous rectification is disable until detecting Hall signal or motor stop signal when CLM is active. After detecting Hall signal or motor stop, synchronous rectification is enabled
Condition to enter Lock Protection mode in OCP active	0x010B	[1]	OCP_LAT_CLR	This register selects the status when OCP is activated. 0: The motor stops until next power on sequence 1: The IC goes to “Lock Protection mode”
Speed control slope setting	0x010B	[0]	STEPSEL	To prevent drastic changes of a target speed in the closed loop control, this register selects slopes of the target speed change against the input duty cycle change. (The amount is prescribed in the time per 1FG pulse) 0: 1/4 of the existing speed, or ±2047 rpm (smaller one is chosen) 1: 1/8 of the existing speed, or ±1023 rpm (smaller one is chosen)

Table 26. REGISTER ADDRESS 0X0100−0X0114 REGISTER DESCRIPTION 2 (continued)

Function	Address	Bits	Register Name	Description
FG/RD select	0x010C	[1:0]	TACHSEL	This register selects FG pin function. 00: FG output 01: RD output (Rotation is Low, Locked motor is High) 10: FG output 11: RD output (Rotation is High, Locked motor is Low)
Input PWM average setting	0x010D	[1:0]	PWMAV	The number of times to perform averaging for input PWM duty cycle. 00: Not averaged 01: Averaged 4 times 10: Averaged 8 times 11: Averaged 16 times
Mask time for reverse recovery time setting	0x010E	[1:0]	OCP_MASK	This register sets the masking time to ignore the reverse recovery for both high-side and low-side Power FET. 00: 0.5 μs 01: 1.0 μs 10: 2.0 μs 11: 4.0 μs
Lock protection enable	0x0110	[3]	LOCK_FAULT	This register selects enable or disable of the lock protection function. 0: Lock protection enable 1: Lock protection disable
OFF time setting (TOP)	0x0111	[7:4]	MSKDEG_TP	This register sets off period at commutation initiation. It is selected as follows. [7] 0: In angle 1: In time [6:4] 000: 0deg or 0 s 001: 0.35deg or 2.0 μs 010: 0.70deg or 4.0 μs 011: 1.05deg or 10.0 μs 100: 2.10deg or 14.0 μs 101: 3.50deg or 20.0 μs 110: 4.90deg or 28.0 μs 111: 7.00deg or 40.0 μs
Feedback Gain Adjustment 1	0x0113	[7:4]	IX	Integral gain coarse 0000: 1x 0001: 2x 0010: 4x 0011: 8x 0100: 16x 0101: 32x 0110: 64x 0111: CUT 1000: 1x 1001: 1/2x 1010: 1/4x 1011: 1/8x 1100: 1/16x 1101: 1/32x 1110: 1/64x 1111: CUT
Feedback Gain Adjustment 2	0x0113	[2:0]	IG	Integral gain fine 000: 1x 001: 7/8x 010: 6/8x 011: 5/8x 100: 4/8x 101: 3/8x 110: 2/8x 111: 1/8x

Table 26. REGISTER ADDRESS 0X0100−0X0114 REGISTER DESCRIPTION 2 (continued)

Function	Address	Bits	Register Name	Description
Feedback Gain Adjustment 3	0x0114	[6:4]	PX	Proportional gain coarse 000: 1x 001: 2x 010: 4x 011: 8x 100: 16x 101: 32x 110: 64x 111: CUT
Feedback Gain Adjustment 4	0x0114	[2:0]	PG	Proportional gain fine 000: 1x 001: 7/8x 010: 6/8x 011: 5/8x 100: 4/8x 101: 3/8x 110: 2/8x 111: 1/8x

Table 27. REGISTER ADDRESS 0X0219 REGISTER DESCRIPTION

Function	Address	Bits	Register Name	Description
Communication error status	0x0219	[6:0]	SWI_ERR	Communication error status is stored to these registers. (Read only) Refer to a section “COMMUNICATION ERROR” for more information.

COMMUNICATION ERROR

The Communication error is reported in the Register (Address 0x0219). Table 28 shows the error report functions.

Table 28. ERROR REPORT DESCRIPTION

Address	Bit	DRVMODE	Error Description	State After Error		
				Mode	Communication	Transferred Data
0X0219	D[6]	R/W Field Data Error	Non-zero value is written in the D[5:1] in R/W Field	Wait for the data from the master	Enable	In write mode: Nullified In read mode: No action
	D[5]	Time out Error	The delay between the fields in “Communication mode” is longer than 3 fields	“Standby”	Terminated	
	D[4]	Checksum Error	Checksum value is wrong in write mode	“Error”	Terminated	Nullified
	D[3]	Data Length Field parity Error	The parity in “Data Length Field” is wrong	“Error”	Terminated	Nullified
	D[2]	R/W Field parity Error	The parity in “R/W Field” is wrong	“Error”	Terminated	Nullified
	D[1]	Header Error	Header input is not correct	“Error”	Terminated	Nullified
	D[0]	Framing Error	The signal pin is “Low” state in Stop bits	“Error”	Terminated	Nullified

When “Time out error” posts ”1” in D[5] of register 0x0219, the LV8310H goes into standby mode.

If the data length is long and the “Time out Error” is happened during the Register write, the data with the correct “Checksum” transferred before the “Time out Error” is stored in register, then the LV8310H goes to “Standby mode”.

When “Checksum error” posts “1” in D[4] of Register 0x0219 while in the Write mode, the LV8310H goes into Error mode and the communication is terminated. In this case, the transferred data is discarded but the data with correct “Checksum” transferred before the “Checksum error” is stored in the register.

Other errors, except for “R/W Field Data Error” also write “1” in the specified register and the LV8310H goes to “Error mode” as well. To recover from “Error mode”, the communication pin should be kept “High” for longer than the time corresponding to 4 “Fields”, then the LV8310H goes to “Standby mode” automatically despite of the status of error register.

Each error register keeps the error bit until the master reads the error register.

Reading Reg.0x0219 as 1byte will clear the error bits. Multiple read will not clear the error bits.

It is recommended to read the error register after every transaction to confirm that the communication is completed successfully.

Figure 27 shows the state diagram. Refer to the application note AND9761 as well for more information regarding the communication.

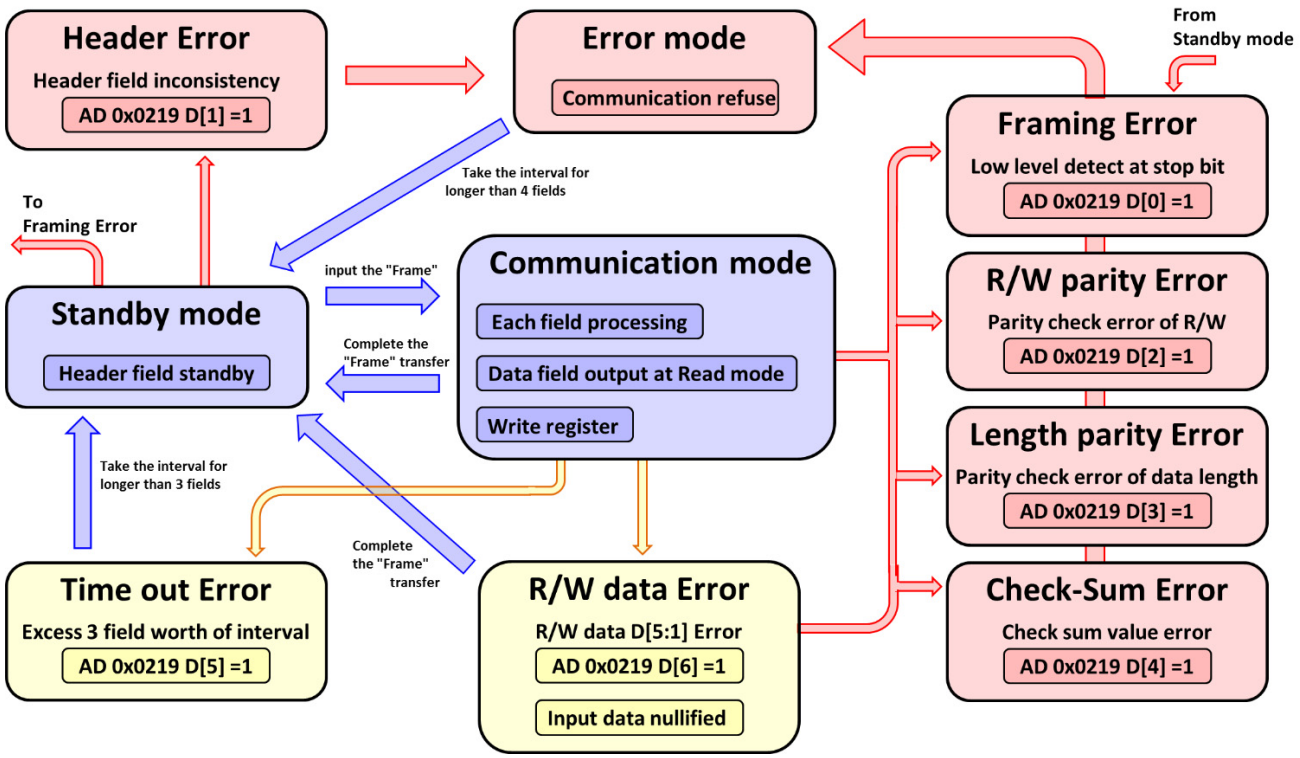


Figure 27. State Transition Diagram of Each Error

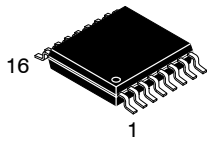
ORDERING INFORMATION TABLE

Device	Package	Shipping†
LV8310HGR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

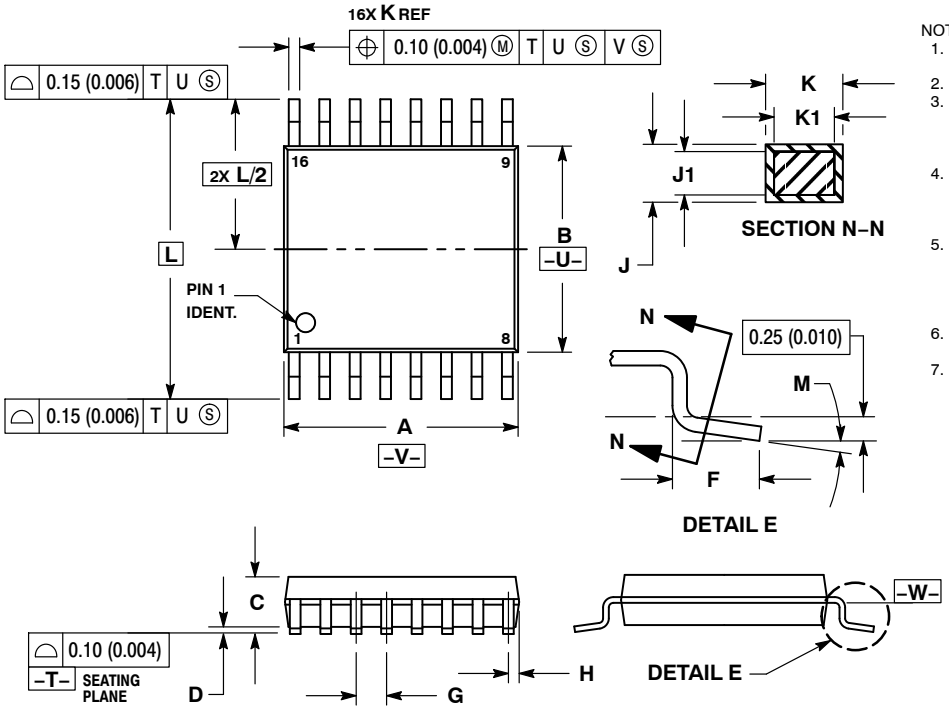
ON Semiconductor®



SCALE 2:1

TSSOP−16
CASE 948F−01
ISSUE B

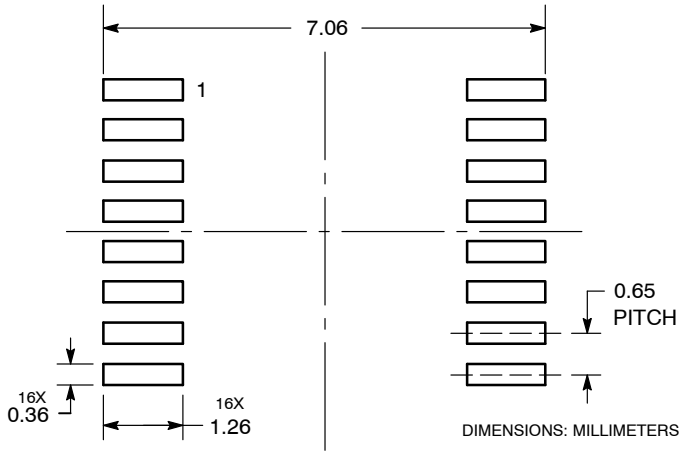
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

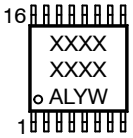
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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