LMV331, NCV331, LMV393, LMV339

Single, Dual, Quad General Purpose, Low Voltage Comparators

The LMV331 is a CMOS single channel, general purpose, low voltage comparator. The LMV393 and LMV339 are dual and quad channel versions, respectively. The LMV331/393/339 are specified for 2.7 V to 5 V performance, have excellent input common−mode range, low quiescent current, and are available in several space saving packages.

The LMV331 is available in 5−pin SC−70 and TSOP−5 packages. The LMV393 is available in a 8−pin Micro8™, SOIC−8, and a UDFN8 package, and the LMV339 is available in a SOIC−14 and a TSSOP−14 package.

The LMV331/393/339 are cost effective solutions for applications where space saving, low voltage operation, and low power are the primary specifications in circuit design for portable applications.

Features

- Guaranteed 2.7 V and 5 V Performance
- Input Common−mode Voltage Range Extends to Ground
- Open Drain Output for Wired−OR Applications
- Low Quiescent Current: 60 μA/channel TYP @ 5 V
- Low Saturation Voltage 200 mV TYP @ 5 V
- Propagation Delay 200 ns TYP @ 5 V
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery Monitors
- Notebooks and PDA's
- General Purpose Portable Devices
- General Purpose Low Voltage Applications

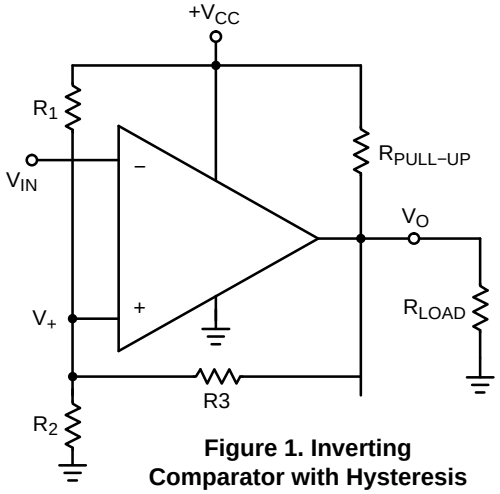

Figure 1. Inverting Comparator with Hysteresis

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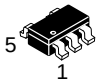
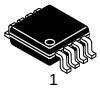
SC−70
CASE 419A



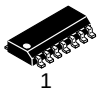
TSOP−5
CASE 483



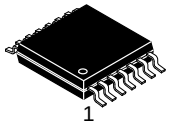
Micro8
CASE 846A

SOIC−8
CASE 751

UDFN8
CASE 517AJ



SOIC−14
CASE 751A



TSSOP−14
CASE 948G

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

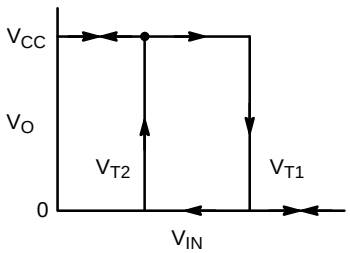
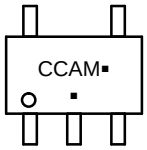


Figure 2. Hysteresis Curve

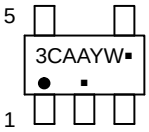
MARKING DIAGRAMS

SC−70
CASE 419A



CCA = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

TSOP−5
CASE 483

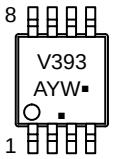


A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

UDFN8
CASE 517AJ

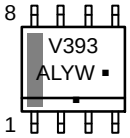
CA = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

Micro8
CASE 846A



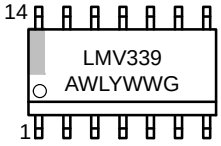
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

SOIC−8
CASE 751



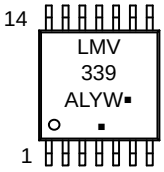
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

SOIC−14
CASE 751A



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

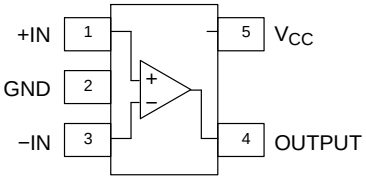
TSSOP−14
CASE 948G



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

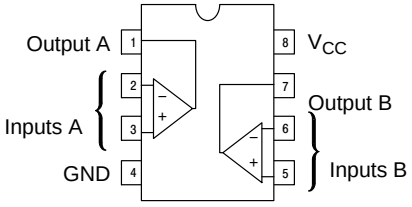
PACKAGE PINOUTS

SC−70/TSOP−5



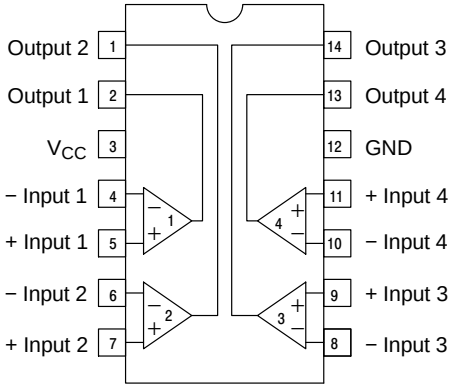
(Top Views)

Micro8 / SOIC−8 / UDFN8



(Top Views)

SOIC−14 / TSSOP−14



(Top Views)

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_S	Voltage on any Pin (referred to V^- pin)	5.5	V
V_{IDR}	Input Differential Voltage Range	±Supply Voltage	V
T_J	Maximum Junction Temperature	150	°C
T_A	Operating Ambient Temperature Range LMV331, LMV393, LMV339 NCV331 (Note 3)	 −40 to 85 −40 to 125	°C
T_{stg}	Storage Temperature Range	−65 to 150	°C
T_L	Mounting Temperature (Infrared or Convection (1/16″ From Case for 30 Seconds))	260	°C
V_{ESD}	ESD Tolerance (Note 1) Machine Model Human Body Model	 100 1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage Temperature Range (Note 2)	2.7 to 5.0	V
θ_{JA}	Thermal Resistance SC−70 TSOP−5 Micro8 SOIC−8 UDFN8 SOIC−14 TSSOP−14	 280 333 238 212 350 156 190	°C/W

1. Human Body Model, applicable std. MIL−STD−883, Method 3015.7. Machine Model, applicable std. JESD22−A115−A (ESD MM std. of JEDEC) Field−Induced Charge−Device Model, applicable std. JESD22−C101−C (ESD FICDM std. of JEDEC).
2. The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.
3. NCV prefix is qualified for automotive usage.

2.7 V DC ELECTRICAL CHARACTERISTICS (All limits are guaranteed for T_A = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1.35 V unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}			1.7	9	mV
Input Offset Voltage Average Drift	T_C V_{IO}			5		μV/°C
Input Bias Current (Note 4)	I_B			< 1		nA
Input Offset Current (Note 4)	I_{IO}			< 1		nA
Input Voltage Range	V_{CM}			0 to 2		V
Saturation Voltage	V_{SAT}	$I_{SINK} \le 1$ mA		120		mV
Output Sink Current	I_O	$V_O \le 1.5$ V	5	23		mA
Supply Current LMV331 NCV331 LMV393 LMV339	I_{CC}			40 40 70 140	100 100 140 200	μA

2.7 V AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 2.7 V, R_L = 5.1 kΩ, V^- = 0 V unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Propagation Delay − High to Low	t_{PHL}	Input Overdrive = 10 mV Input Overdrive = 100 mV		1000 500		ns
Propagation Delay − Low to High	t_{PLH}	Input Overdrive = 10 mV Input Overdrive = 100 mV		800 200		ns

4. Guaranteed by design and/or characterization.

5.0 V DC ELECTRICAL CHARACTERISTICS (All limits are guaranteed for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 2.5 V unless otherwise noted. Limits over temperature are guaranteed by design and/or characterization.)

Parameter	Symbol	Condition (Note 6)	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	$T_A = T_{LO}$ to T_{HIGH}		1.7	9	mV
Input Offset Voltage Average Drift		$T_A = T_{LO}$ to T_{HIGH}		5		μV/°C
Input Bias Current (Note 5)	I_B	$T_A = T_{LO}$ to T_{HIGH}		< 1		nA
Input Offset Current (Note 5)	I_{IO}	$T_A = T_{LO}$ to T_{HIGH}		< 1		nA
Input Voltage Range	V_{CM}			0 to 4.2		V
Voltage Gain (Note 5)	A_V		20	50		V/mV
Saturation Voltage	V_{SAT}	I_{SINK} = 10 mA $T_A = T_{LO}$ to T_{HIGH}		200	400 700	mV
Output Sink Current	I_O	$V_O \le 1.5$ V	10	84		mA
Supply Current LMV331	I_{CC}	$T_A = T_{LO}$ to T_{HIGH}		60	120 150	μA
Supply Current LMV393	I_{CC}	$T_A = T_{LO}$ to T_{HIGH}		100	200 250	μA
Supply Current LMV339	I_{CC}	$T_A = T_{LO}$ to T_{HIGH}		170	300 350	μA
Output Leakage Current (Note 5)		$T_A = T_{LO}$ to T_{HIGH}		0.003	1	μA

5.0 V AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 5 V, R_L = 5.1 kΩ, V^- = 0 V unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Propagation Delay − High to Low	t_{PHL}	Input Overdrive = 10 mV Input Overdrive = 100 mV		1500 900		ns
Propagation Delay − Low to High	t_{PLH}	Input Overdrive = 10 mV Input Overdrive = 100 mV		800 200		ns

5. Guaranteed by design and/or characterization.
6. For LMV331, LMV393, LMV339: T_A = −40°C to 85°C
   For NCV331: T_A = −40°C to 125°C

TYPICAL CHARACTERISTICS

(V_{CC} = 5.0 V, T_A = 25°C, R_L = 5 kΩ unless otherwise specified)

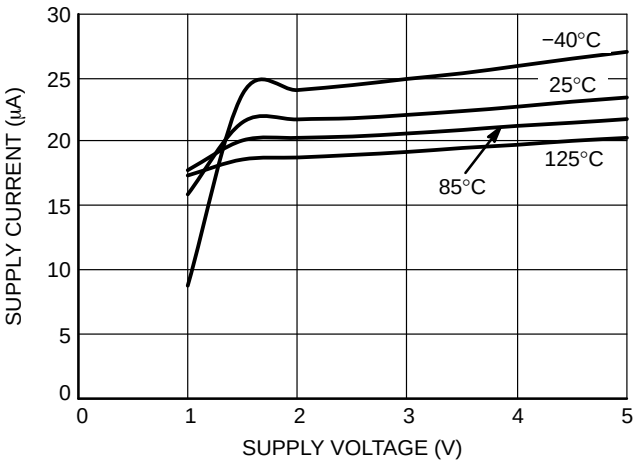


Figure 3. Supply Current vs. Supply Voltage (Output High)

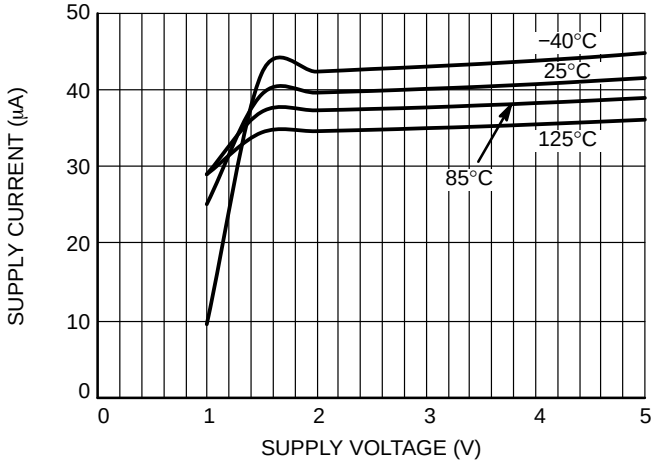


Figure 4. Supply Current vs. Supply Voltage (Output Low)

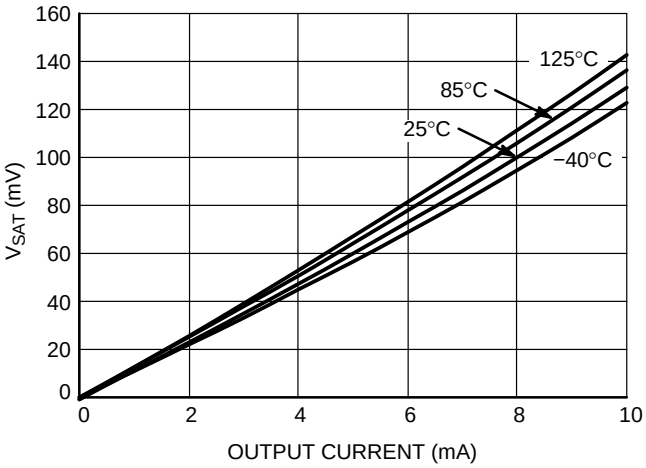


Figure 5. V_{SAT} vs. Output Current at V_{CC} = 2.7 V

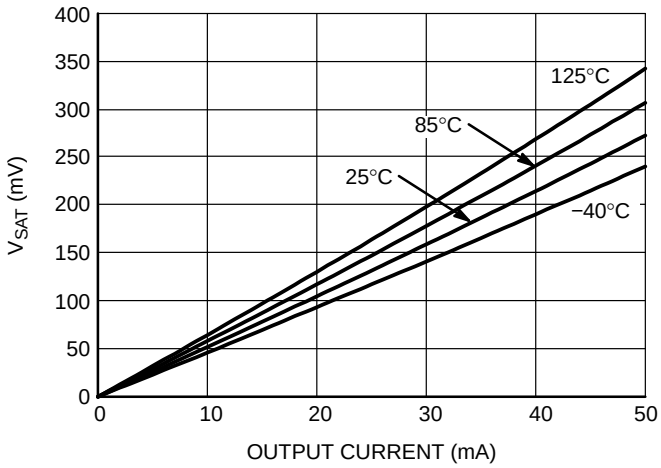


Figure 6. V_{SAT} vs. Output Current at V_{CC} = 5.0 V

NEGATIVE TRANSITION INPUT − V_{CC} = 2.7 V

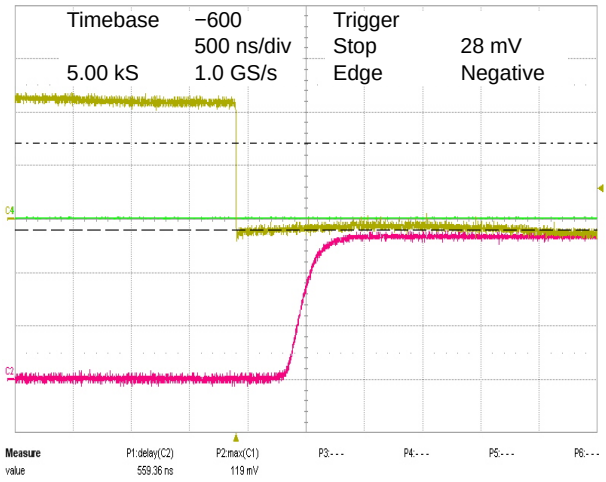


Figure 7. 10 mV Overdrive

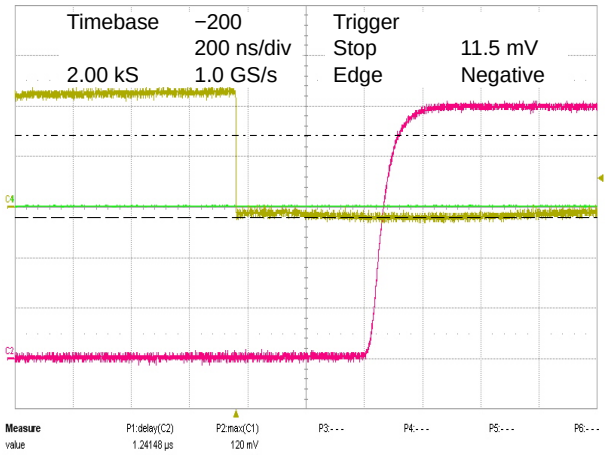


Figure 8. 20 mV Overdrive

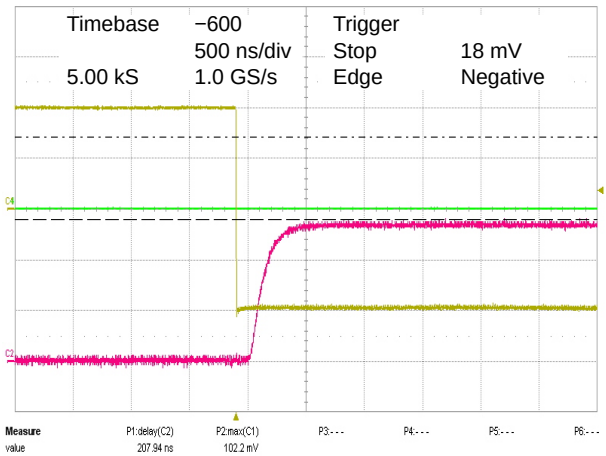


Figure 9. 100 mV Overdrive

POSITIVE TRANSITION INPUT − V_{CC} = 2.7 V

Figure 10. 10 mV Overdrive

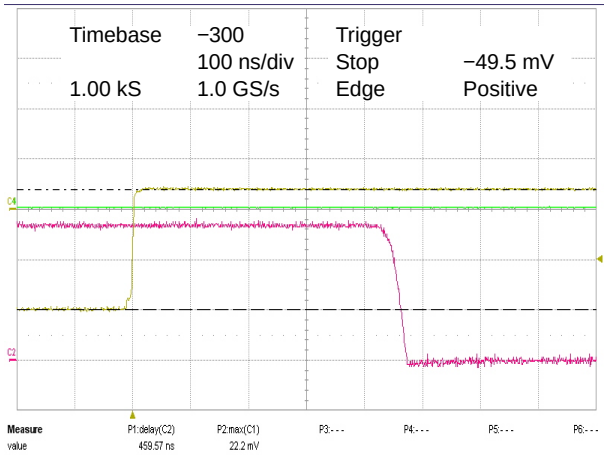


Figure 11. 20 mV Overdrive

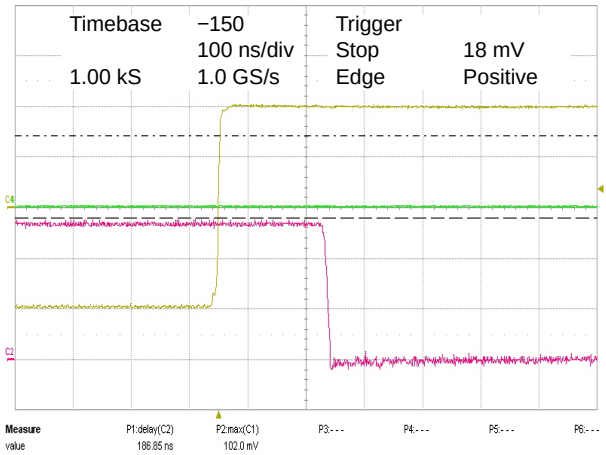


Figure 12. 100 mV Overdrive

NEGATIVE TRANSITION INPUT − V_{CC} = 5.0 V

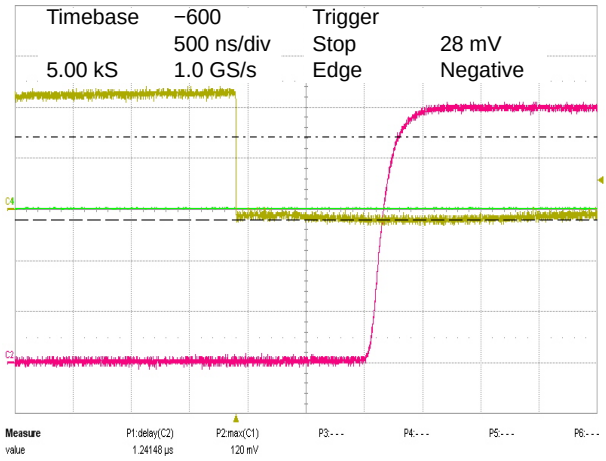


Figure 13. 10 mV Overdrive

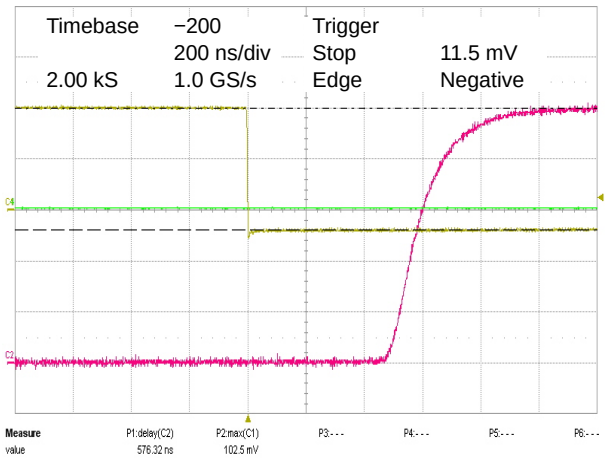


Figure 14. 20 mV Overdrive

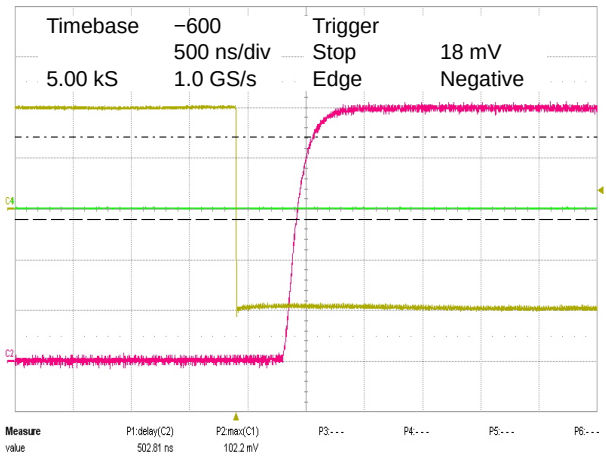


Figure 15. 100 mV Overdrive

POSITIVE TRANSITION INPUT − V_{CC} = 5.0 V

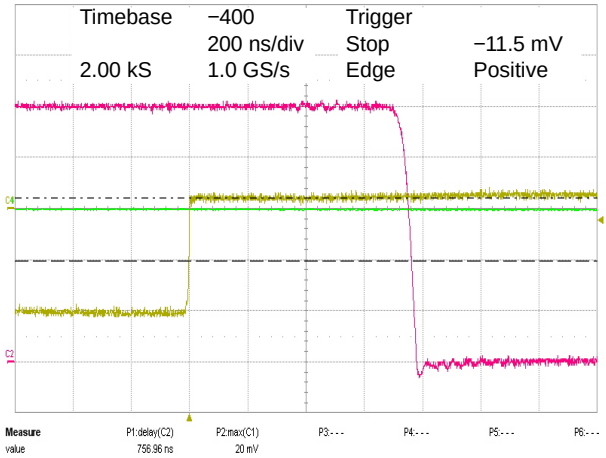


Figure 16. 10 mV Overdrive

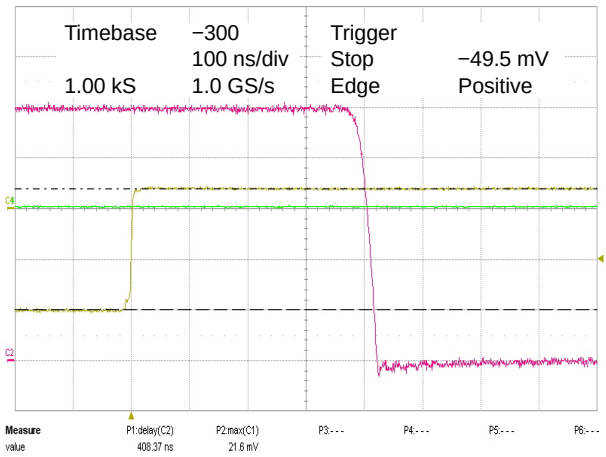


Figure 17. 20 mV Overdrive

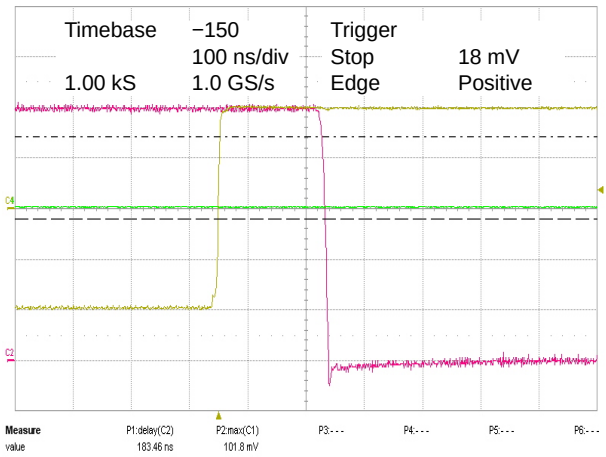


Figure 18. 100 mV Overdrive

APPLICATION CIRCUITS

Basic Comparator Operation

The basic operation of a comparator is to compare two input voltage signals, and produce a digital output signal by determining which input signal is higher. If the voltage on the non−inverting input is higher, then the internal output transistor is off and the output will be high. If the voltage on the inverting input is higher, then the output transistor will be on and the output will be low. The LMV331/393/339 has an open−drain output stage, so a pull−up resistor to a positive supply voltage is required for the output to switch properly.

The size of the pull−up resistor is recommended to be between 1 kΩ and 10 kΩ. This range of values will balance two key factors; i.e., power dissipation and drive capability for interface circuitry.

Figure 19 illustrates the basic operation of a comparator and assumes dual supplies. The comparator compares the input voltage (V_{IN}) on the non−inverting input to the reference voltage (V_{REF}) on the inverting input. If V_{IN} is less than V_{REF}, the output voltage (V_O) will be low. If V_{IN} is greater than V_{REF}, then V_O will be high.

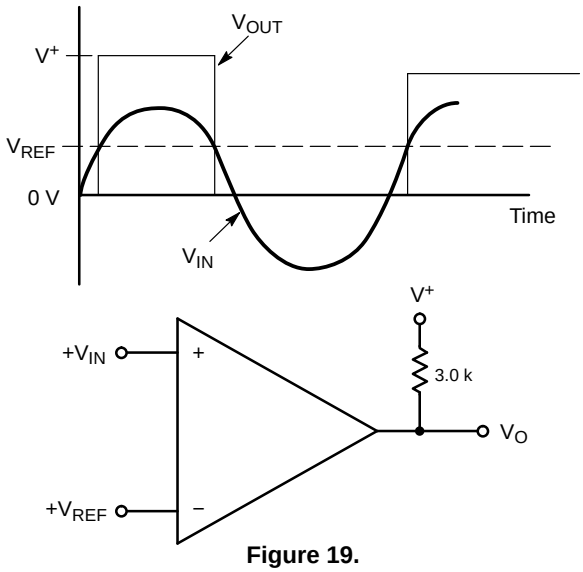


Figure 19.

Comparators and Stability

A common problem with comparators is oscillation due to their high gain. The basic comparator configuration in Figure 19 may oscillate if the differential voltage between the input pins is close to the device's offset voltage. This can happen if the input signal is moving slowly through the comparator's switching threshold or if unused channels are connected to the same potential for termination of unused channels. One way to eliminate output oscillations or 'chatter' is to include external hysteresis in the circuit design.

Inverting Configuration with Hysteresis

An inverting comparator with hysteresis is shown in Figure 20.

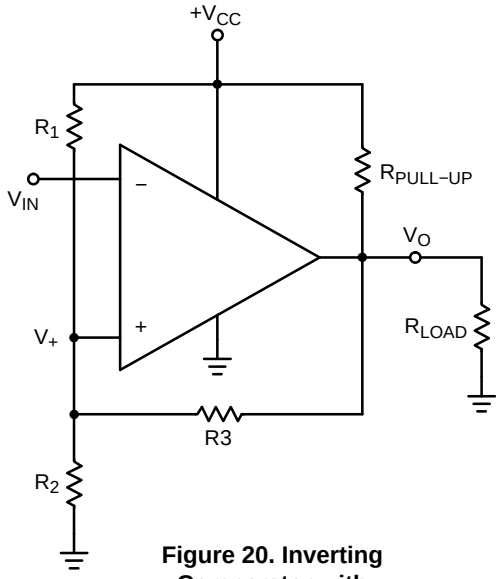


Figure 20. Inverting Comparator with Hysteresis

When V_{IN} is less than the voltage at the non−inverting node, V_+, the output voltage will be high. When V_{IN} is greater than the voltage at V_+, then the output will be low. The hysteresis band (Figure 21) created from the resistor network is defined as:

$$\Delta V_+ = V_{T1} - V_{T2}$$

where V_{T1} and V_{T2} are the lower and upper trip points, respectively.

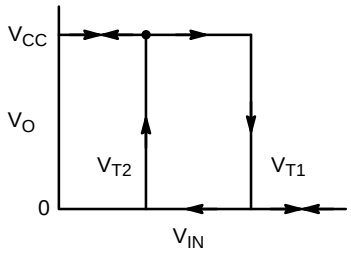


Figure 21.

V_{T1} is calculated by assuming that the output of the comparator is pulled up to supply when high. The resistances R_1 and R_3 can be viewed as being in parallel which is in series with R_2 (Figure 22). Therefore V_{T1} is:

$$V_{T1} = \frac{V_{CC}\, R_2}{(R_1 \parallel R_3) + R_2}$$

V_{T2} is calculated by assuming that the output of the comparator is at ground potential when low. The resistances R_2 and R_3 can be viewed as being in parallel which is in series with R_1 (Figure 23). Therefore V_{T2} is:

$$V_{T2} = \frac{V_{CC}(R_2 \parallel R_3)}{R_1 + (R_2 \parallel R_3)}$$

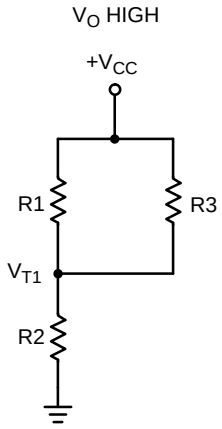


Figure 22.

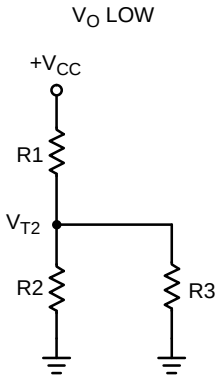


Figure 23.

Non−inverting Configuration with Hysteresis

A non−inverting comparator is shown in Figure 24.

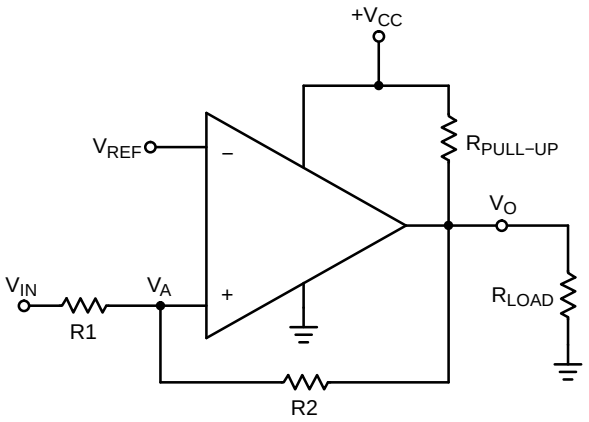


Figure 24.

The hysteresis band (Figure 25) of the non−inverting configuration is defined as follows:

$$\Delta V_{in} = V_{CC} R_1 / R_2$$

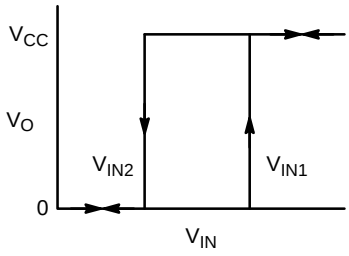


Figure 25.

When V_{IN} is much less than the voltage at the inverting input (V_{REF}), then the output is low. R_2 can then be viewed as being connected to ground (Figure 26). To calculate the voltage required at V_{IN} to trip the comparator high, the following equation is used:

$$V_{in1} = \frac{V_{ref}\,(R_1 + R_2)}{R_2}$$

When the output is high, V_{IN} must less than or equal to V_{REF} ($V_{IN} \le V_{REF}$) before the output will be low again (Figure 27). The following equation is used to calculate the voltage at V_{IN} to switch the output back to the low state:

$$V_{in2} = \frac{V_{ref}\,(R_1 + R_2) - V_{CC} R_1}{R_2}$$

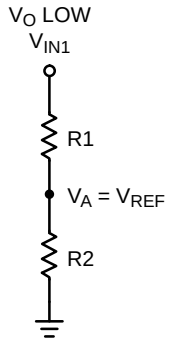


Figure 26.

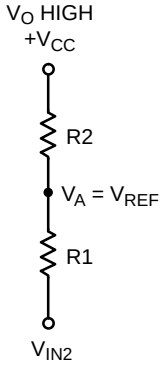


Figure 27.

Termination of Unused Inputs

Proper termination of unused inputs is a good practice to keep the output from ‘chattering.’ For example, if one channel of a dual or quad package is not being used, then the inputs must be connected to a defined state. The recommended connections would be to tie one input to V_{CC} and the other input to ground.

ORDERING INFORMATION

Order Number	Number of Channels	Specific Device Marking	Package Type	Shipping†
LMV331SQ3T2G	Single	CCA	SC−70 (Pb−Free)	3000 / Tape & Reel
LMV331SN3T1G	Single	3CA	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV331SN3T1G	Single	3CA	TSOP−5 (Pb−Free)	3000 / Tape & Reel
LMV393DMR2G	Dual	V393	Micro8 (Pb−Free)	4000 / Tape & Reel
LMV393DR2G	Dual	V393	SOIC−8 (Pb−Free)	2500 / Tape & Reel
LMV393MUTAG	Dual	CA	UDFN8 (Pb−Free)	3000 / Tape & Reel
LMV339DR2G	Quad	LMV339	SOIC−14 (Pb−Free)	2500 / Tape & Reel
LMV339DTBR2G	Quad	LMV 339	TSSOP−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Contact factory.

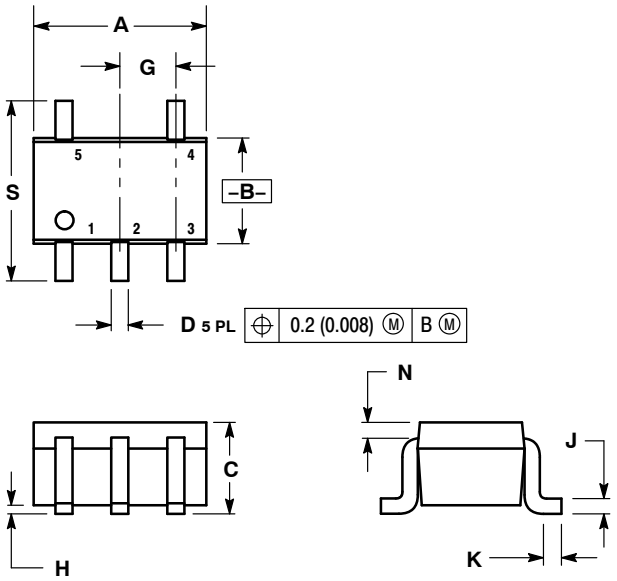
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L

SCALE 2:1

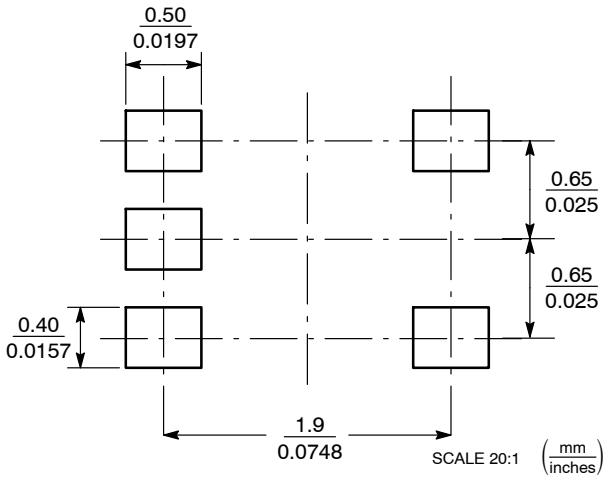
DATE 17 JAN 2013



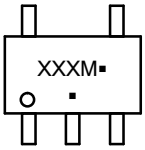
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

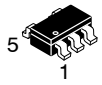
STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

DOCUMENT NUMBER:	98ASB42984B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SC−88A (SC−70−5/SOT−353)	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

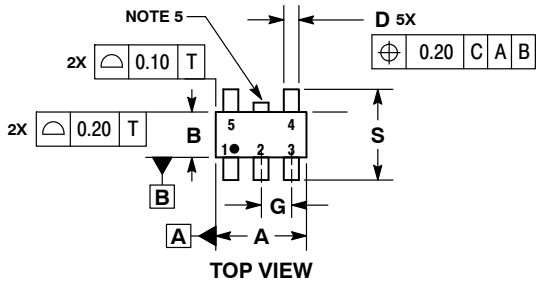
ON Semiconductor®



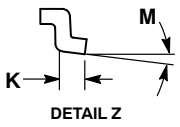
SCALE 2:1

TSOP−5
CASE 483
ISSUE N

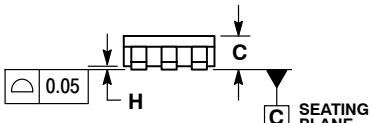
DATE 12 AUG 2020



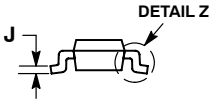
TOP VIEW



DETAIL Z



SIDE VIEW

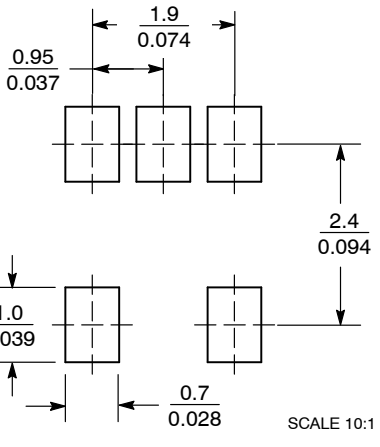


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

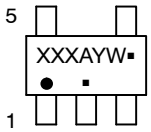
SOLDERING FOOTPRINT*



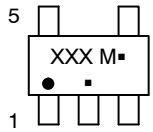
SCALE 10:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

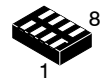
DOCUMENT NUMBER:	98ARB18753C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TSOP−5	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

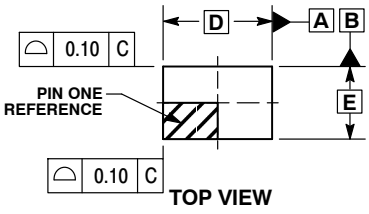
ON Semiconductor®

UDFN8 1.8x1.2, 0.4P
CASE 517AJ−01
ISSUE O

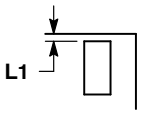
DATE 08 NOV 2006



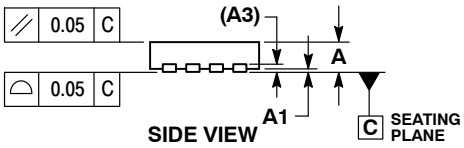
SCALE 4:1



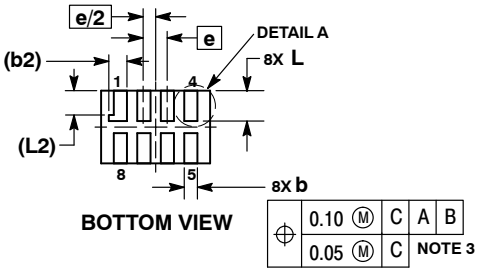
TOP VIEW



DETAIL A
NOTE 5



SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

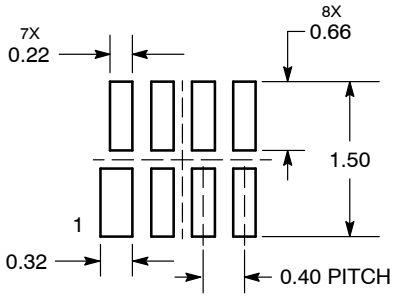
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
b2	0.30 REF	
D	1.80 BSC	
E	1.20 BSC	
e	0.40 BSC	
L	0.45	0.55
L1	0.00	0.03
L2	0.40 REF	

GENERIC MARKING DIAGRAM*

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

MOUNTING FOOTPRINT SOLDERMASK DEFINED



DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	**98AON23417D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**UDFN8 1.8X1.2, 0.4P**		**PAGE 1 OF 1**

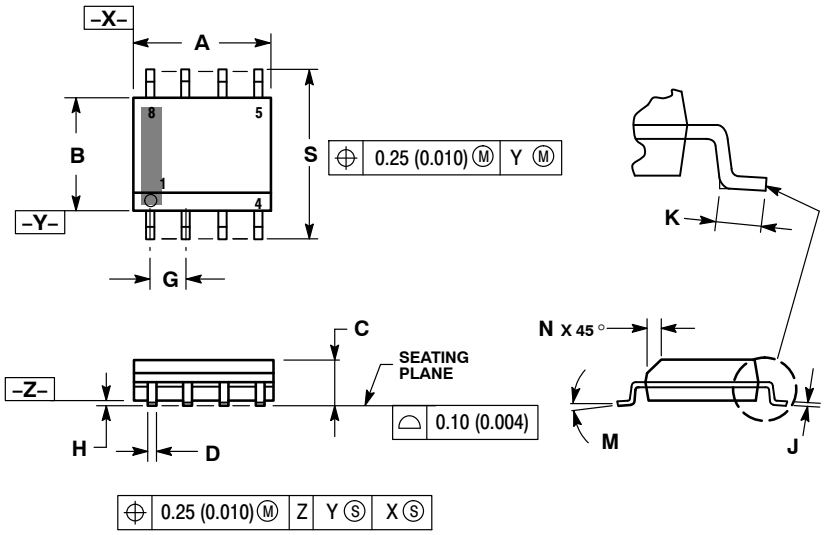
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

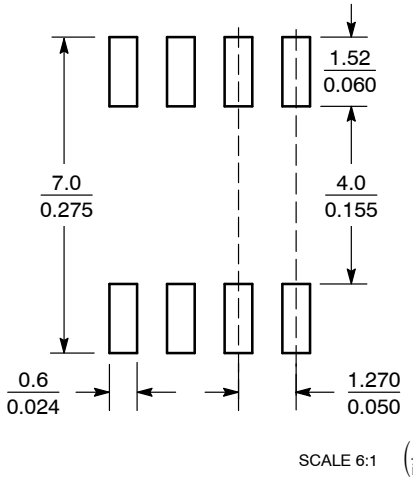
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

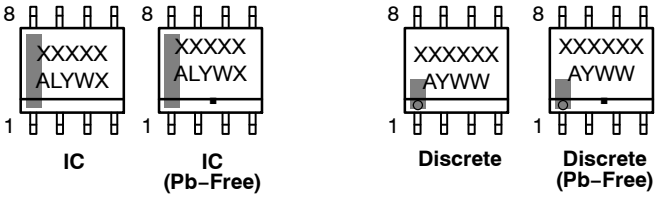
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

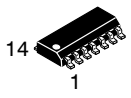
STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

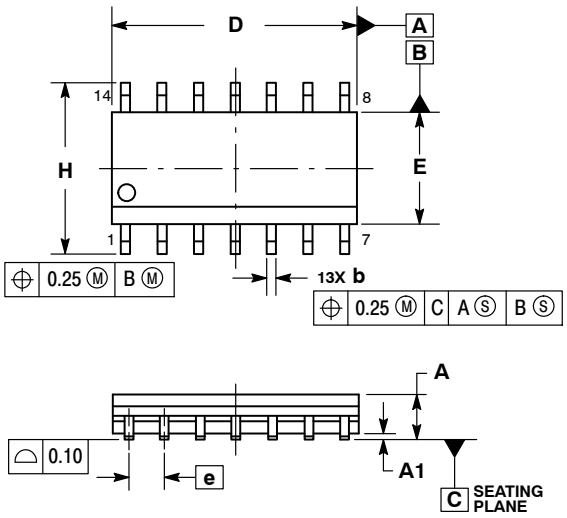
ON Semiconductor®

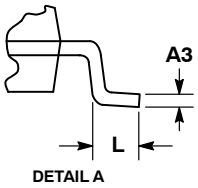


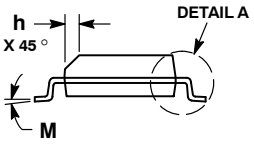
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



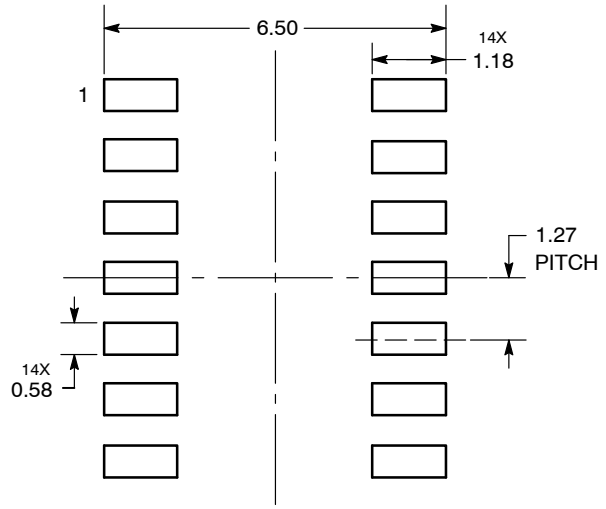




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

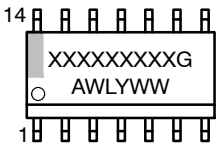
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

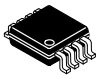
STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

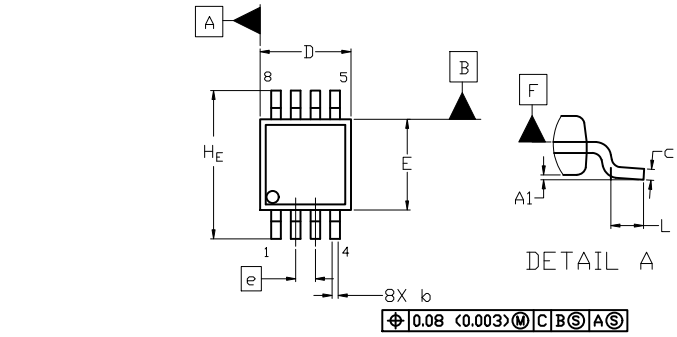
ON Semiconductor®

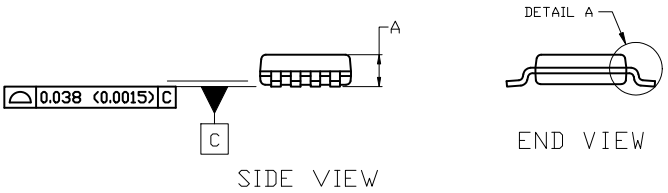


SCALE 2:1

Micro8
CASE 846A−02
ISSUE K

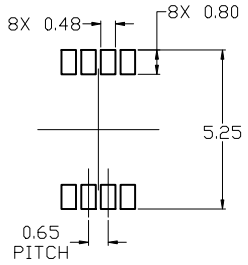
DATE 16 JUL 2020





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

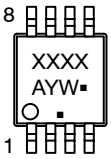


RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

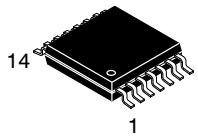
DOCUMENT NUMBER:	**98ASB14087C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**MICRO8**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

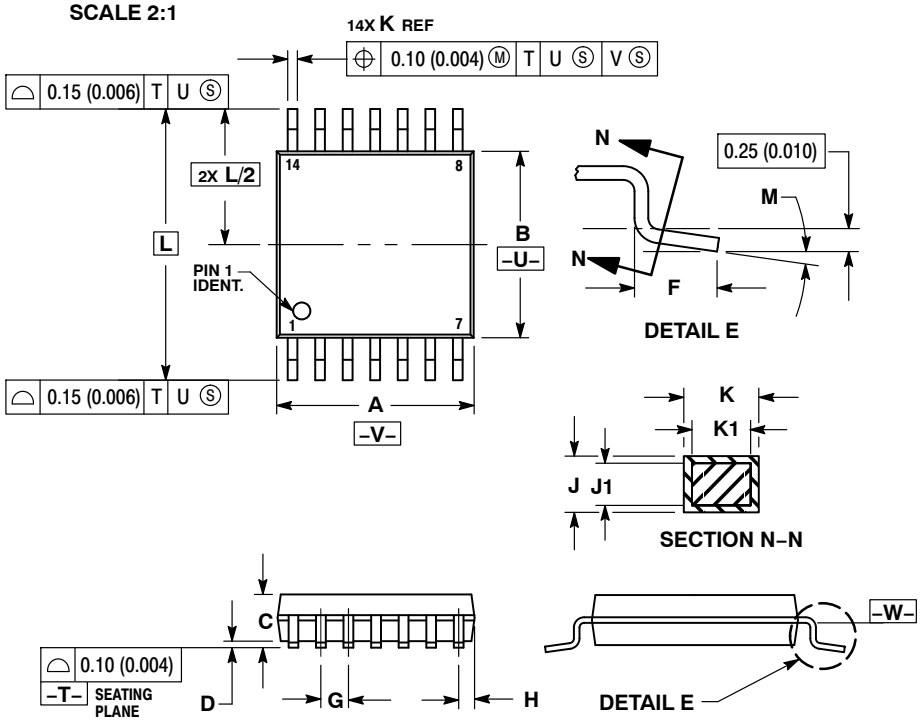
ON Semiconductor®

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



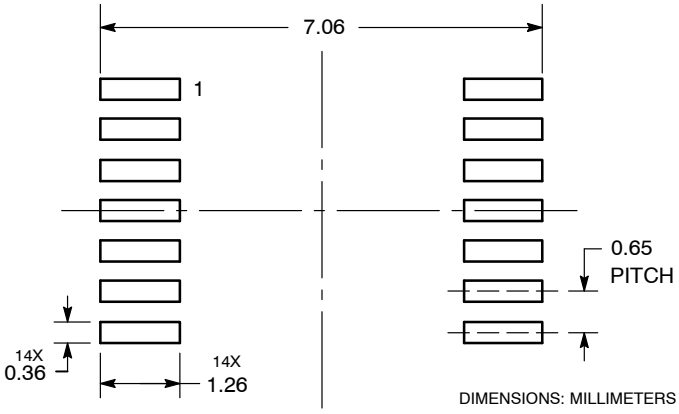
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

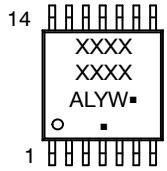
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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