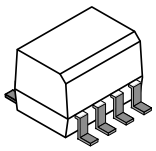
High Noise Immunity, 3.3 V / 5 V Logic Gate Optocoupler

FOD8001

ON Semiconductor®

www.onsemi.com



SOIC8
CASE 751DZ

Description

The FOD8001 is a 3.3 V / 5 V high−speed logic gate optocoupler, which supports isolated communications allowing digital signals to communicate between systems without conducting ground loops or hazardous voltages. It utilizes ON Semiconductor patented coplanar packaging technology, Optoplanar®, and optimized IC design to achieve high noise immunity, characterized by high common mode rejection and power supply rejection specifications.

This high−speed logic gate optocoupler, packaged in a compact 8−pin small outline package, consists of a high−speed AlGaAs LED driven by a CMOS buffer IC coupled to a CMOS detector IC. The detector IC comprises an integrated photodiode, a high−speed transimpedance amplifier and a voltage comparator with an output driver. The CMOS technology coupled to the high efficiency of the LED achieves low power consumption as well as very high speed (40ns propagation delay, 6ns pulse width distortion).

Features

- High Noise Immunity characterized by Common Mode Rejection (CMR) and Power Supply Rejection (PSR) Specifications
  - 20 kV/μs Minimum Static CMR @ Vcm = 1000 V
  - 25 kV/μs Typical Dynamic CMR @ Vcm = 1500 V, 20 MBaud Rate
  - PSR in Excess of 10% of the Supply Voltages across Full Operating Bandwidth
- High Speed:
  - 25 Mbit/s Date Rate (NRZ)
  - 40 ns max. Propagation Delay
  - 6 ns max. Pulse Width Distortion
  - 20 ns max. Propagation Delay Skew
- 3.3 V and 5 V CMOS Compatibility
- Extended Industrial Temperate Range, −40°C to 105°C Temperature Range
- Safety and Regulatory Pending Approvals:
  - UL1577, 3750 VACRMS for 1 min.
  - IEC60747−5−2 (pending)

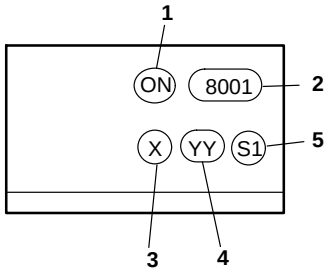
Applications

- Industrial Fieldbus Communications
  - Profibus, DeviceNet, CAN, RS485
- Programmable Logic Control
- Isolated Data Acquisition System

TRUTH TABLE

V_I	LED	V_O
HIGH	OFF	HIGH
LOW	ON	LOW

MARKING DIAGRAM

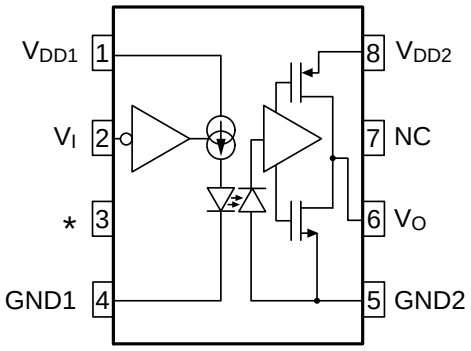


1. ON = ON Semiconductor Logo
2. 8001 = Device Number
3. X = One−Digit Year Code, e.g. ‘8’
4. YY = Two Digit Work Week Ranging from ‘01’ to ‘53’
5. S1 = Assembly Package Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

Functional Schematic



*: Pin 3 must be left unconnected

Figure 1. Functional Schematic

PIN DEFINITIONS

Pin Number	Pin Name	Pin Function Description
1	V_{DD1}	Input Supply Voltage
2	V_I	Input Data
3		LED Anode – Must be left unconnected
4	GND1	Input Ground
5	GND2	Output Ground
6	V_O	Output Data
7	NC	Not Connected
8	V_{DD2}	Output Supply Voltage

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	−40 to +125	°C
T_{OPR}	Operating Temperature	−40 to +105	°C
T_{SOL}	Lead Solder Temperature (Refer to Reflow Temperature Profile)	260 for 10 s	°C
V_{DD1}, V_{DD2}	Supply Voltage	0 to 6.0	V
V_I	Input Voltage	−0.5 to V_{DD1} + 0.5	V
I_I	Input DC Current	−10 to +10	μA
V_O	Output Voltage	−0.5 to V_{DD2} + 0.5	V
I_O	Average Output Current	10	mA
PD_I	Input Power Dissipation (Note 1)	90	mW
PD_O	Total Power Dissipation (Note 2)	70	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Derate linearly from 25°C at a rate of tbd W/°C
2. Derate linearly from 25°C at a rate of tbd mW/°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	−40	+105	°C
V_{DD1}, V_{DD2}	Supply Voltages (3.3 V Operation) (Note 3)	3.0	3.6	V
	Supply Voltages (5.0 V Operation) (Note 3)	4.5	5.5	
V_{IH}	Logic High Input Voltage	2.0	V_{DD}	V
V_{IL}	Logic Low Input Voltage	0	0.8	V
t_r, t_f	Input Signal Rise and Fall Time		1.0	ms

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
3. 0.1 μF bypass capacitor must be connected between Pin 1 and 4, and 5 and 8.

ISOLATION CHARACTERISTICS (Apply over all recommended conditions, typical value is measured at T_A = 25°C)

Symbol	Characteristics	Test Conditions	Min.	Typ.	Max.	Unit
V_{ISO}	Input−Output Isolation Voltage	f = 60 Hz, t = 1.0 min., $I_{I-O} \le$ 10 μA (Notes 4, 5)	3750			Vac_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500V (Note 4)	10^{11}			Ω
C_{ISO}	Isolation Capacitance	V_{I-O} = 0 V, f = 1.0MHz (Note 4)		0.2		pF

4. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
5. 3,750 VAC_{RMS} for 1 minute duration is equivalent to 4,500 VAC_{RMS} for 1 second duration.

ELECTRICAL CHARACTERISTICS (Apply over all recommended conditions, typical value is measured at V_{DD1} = V_{DD2} = +3.3 V, V_{DD1} = +3.3 V and V_{DD2} = +5.0 V, V_{DD1} = +5.0 V and V_{DD2} = +3.3 V, V_{DD1} = V_{DD2} = +5.0 V, T_A = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
INPUT CHARACTERISTICS						
I_{DD1L}	Logic Low Input Supply Current	V_I = 0 V		6.2	10.0	mA
I_{DD1H}	Logic High Input Supply Current	V_I = V_{DD1}		0.8	3.0	mA
I_{IA}, I_{IB}	Input Current		−10		+10	μA
OUTPUT CHARACTERISTICS						
I_{DD2L}	Logic Low Output Supply Current	V_I = 0 V		4.5	9.0	mA
I_{DD2H}	Logic High Output Supply Current	V_I = V_{DD1}		4.5	9.0	mA
V_{OH}	Logic High Output Voltage	I_O = −20 μA, V_I = V_{IH}, V_{DD2} = +3.3 V	2.9	3.3		V
		I_O = −4 mA, V_I = V_{IH}, V_{DD2} = +3.3 V	1.9	2.9		
		I_O = −20 μA, V_I = V_{IH}, V_{DD2} = +5.0 V	4.4	5.0		
		I_O = −4 mA, V_I = V_{IH}, V_{DD2} = +5.0 V	4.0	4.8		
V_{OL}	Logic Low Output Voltage	I_O = 20 μA, V_I = V_{IL}		0	0.1	V
		I_O = 4 mA, V_I = V_{IL}		0.3	1.0	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

SWITCHING CHARACTERISTICS (Apply over all recommended conditions, typical value is measured at V_{DD1} = V_{DD2} = +3.3 V, V_{DD1} = +3.3 V and V_{DD2} = +5.0 V, V_{DD1} = +5.0 V and V_{DD2} = +3.3 V, V_{DD1} = V_{DD2} = +5.0 V, T_A = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PHL}	Propagation Delay Time to Logic Low Output	C_L = 15 pF		25	40	ns
t_{PLH}	Propagation Delay Time to Logic High Output	C_L = 15 pF		25	40	ns
PWD	Pulse Width Distortion, $\lvert t_{PHL} - t_{PLH} \rvert$	PWD = 40 ns, C_L = 15 pF		2	6	ns
	Data Rate				25	Mb/s
t_{PSK}	Propagation Delay Skew	C_L = 15 pF (6)			20	ns
t_R	Output Rise Time (10%–90%)			6.5		ns
t_F	Output Fall Time (90%–10%)			6.5		ns
$\lvert CM_H \rvert$	Common Mode Transient Immunity at Output High	V_I = V_{DD1}, V_O > 0.8 V_{DD1}, V_{CM} = 1000 V (Note 7)	20	40		kV/μs
$\lvert CM_L \rvert$	Common Mode Transient Immunity at Output Low	V_I = 0 V, V_O < 0.8 V, V_{CM} = 1000 V (Note 7)	20	40		kV/μs
C_{PDI}	Input Dynamic Power Dissipation Capacitance (Note 8)			30		pF
C_{PDO}	Output Dynamic Power Dissipation Capacitance (Note 8)			3		pF

6. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
7. Common mode transient immunity at output high is the maximum tolerable positive dVcm/dt on the leading edge of the common mode impulse signal, Vcm, to assure that the output will remain high. Common mode transient immunity at output low is the maximum tolerable negative dVcm/dt on the trailing edge of the common pulse signal, Vcm, to assure that the output will remain low.
8. Unloaded dynamic power dissipation is calculated as follows: C_{PD} x V_{DD} x *f* + I_{DD} + V_{PD} where *f* is switched time in MHz.

TYPICAL PERFORMANCE CURVES

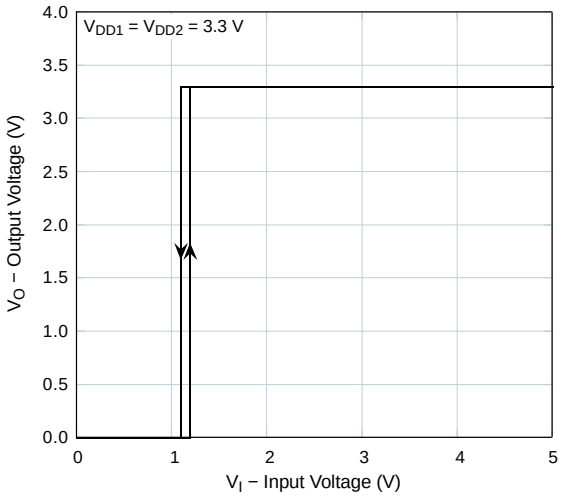


Figure 2. Typical Output Voltage vs. Input Voltage

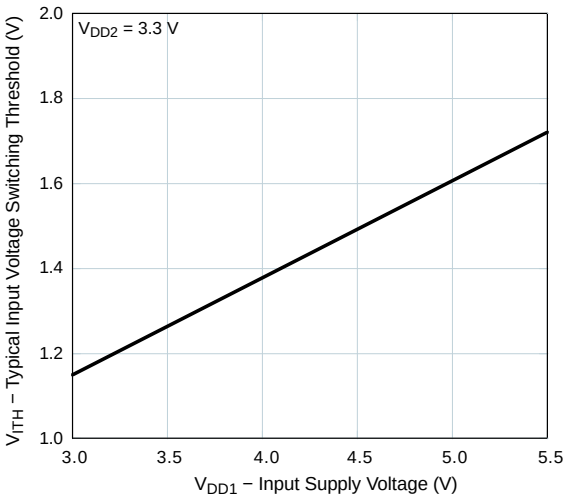


Figure 3. Input Voltage Switching Threshold vs. Input Supply Voltage

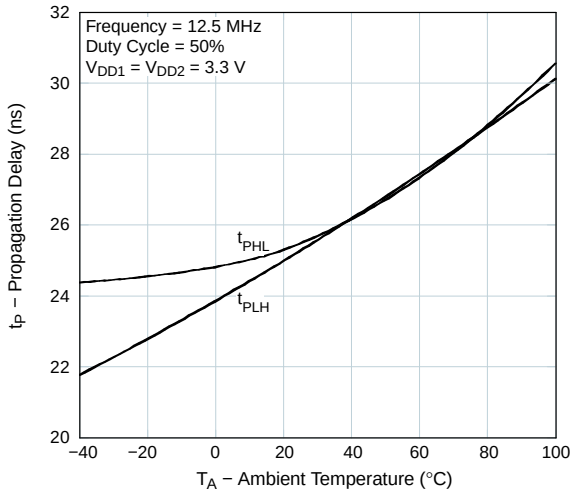


Figure 4. Propagation Delay vs. Ambient Temperature

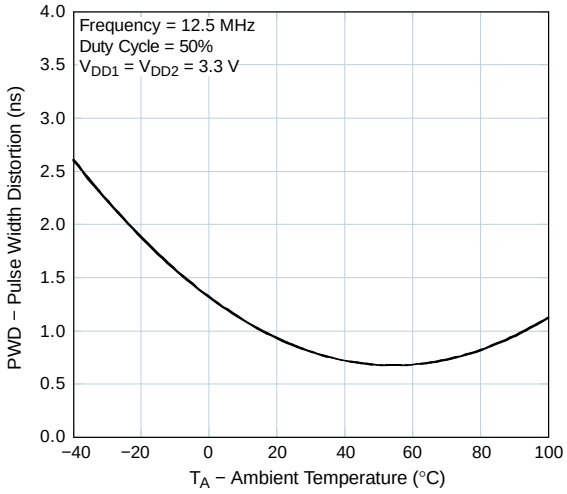


Figure 5. Pulse Width Distortion vs. Ambient Temperature

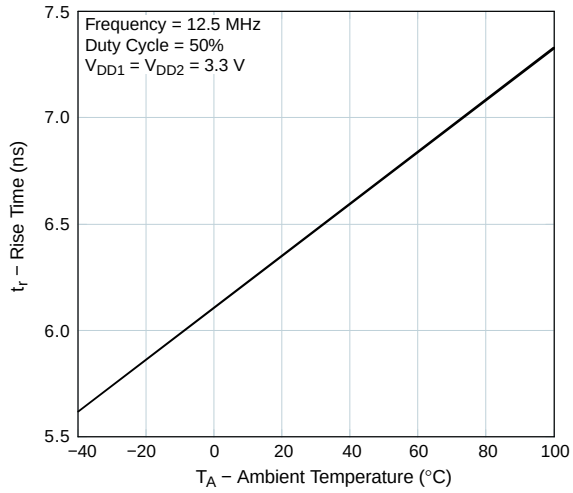


Figure 6. Typical Rise Time vs. Ambient Temperature

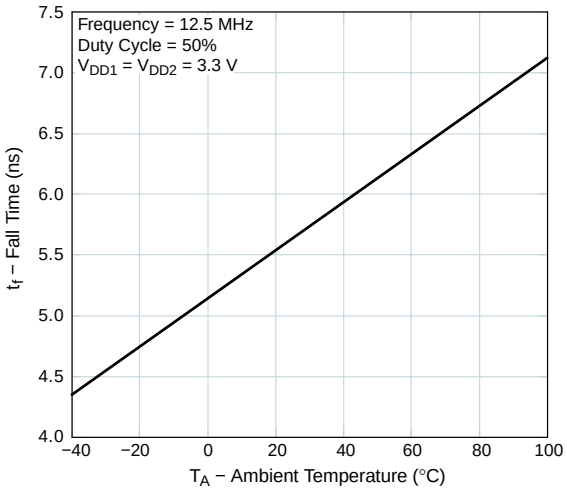


Figure 7. Typical Fall Time vs. Ambient Temperature

TYPICAL PERFORMANCE CURVES (Continued)

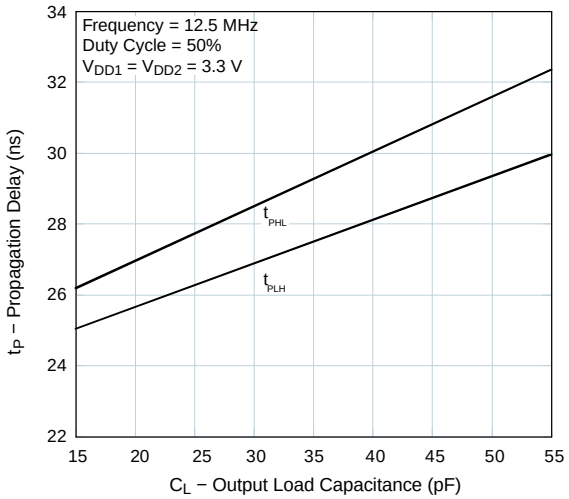


Figure 8. Typical Propagation Delay vs. Output Load Capacitance

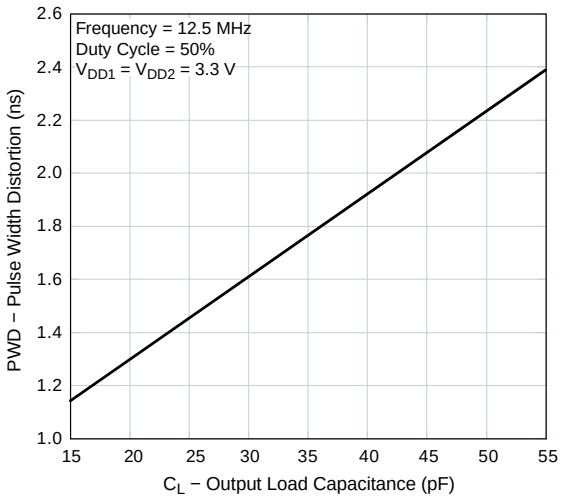


Figure 9. Typical Width Distortion vs. Output Load Capacitance

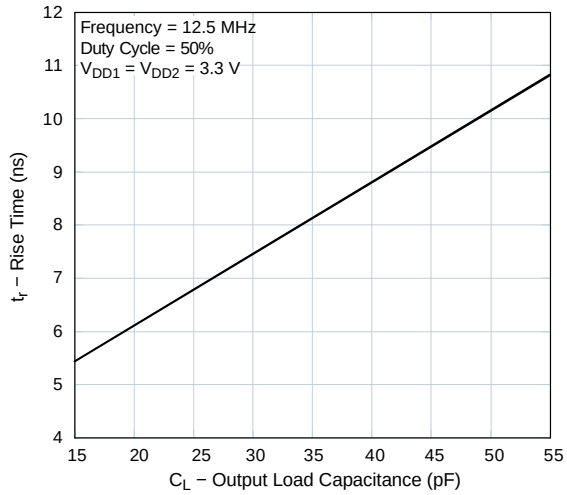


Figure 10. Typical Rise Time vs. Output Load Capacitance

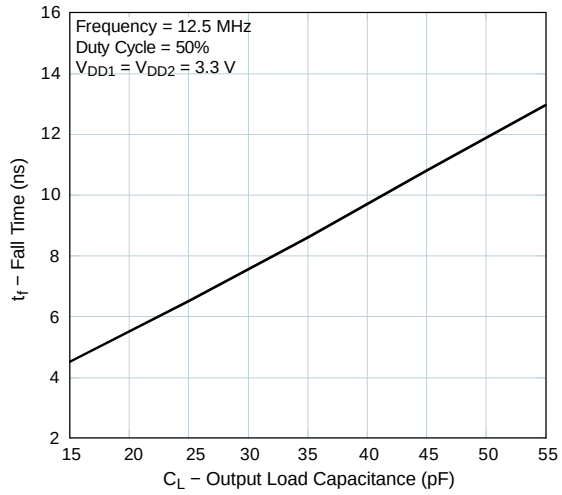


Figure 11. Typical Fall Time vs. Output Load Capacitance

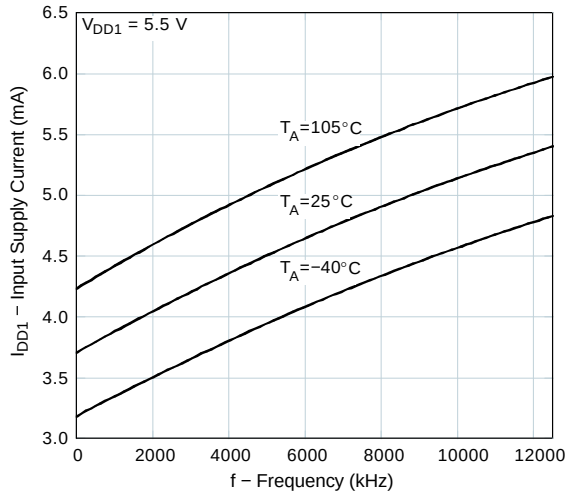


Figure 12. Input Supply Current vs. Frequency

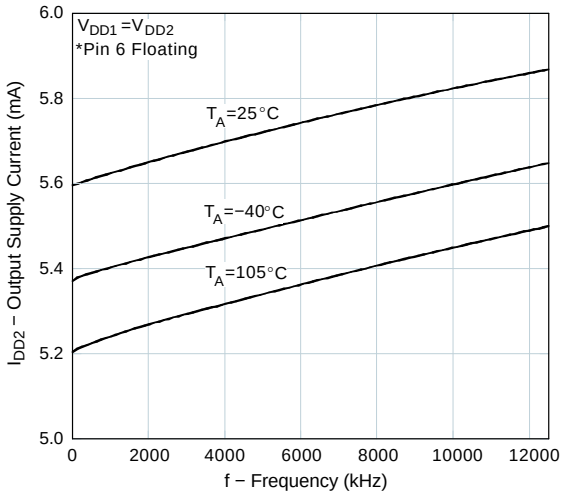


Figure 13. Output Supply Current vs. Frequency

TEST CIRCUITS

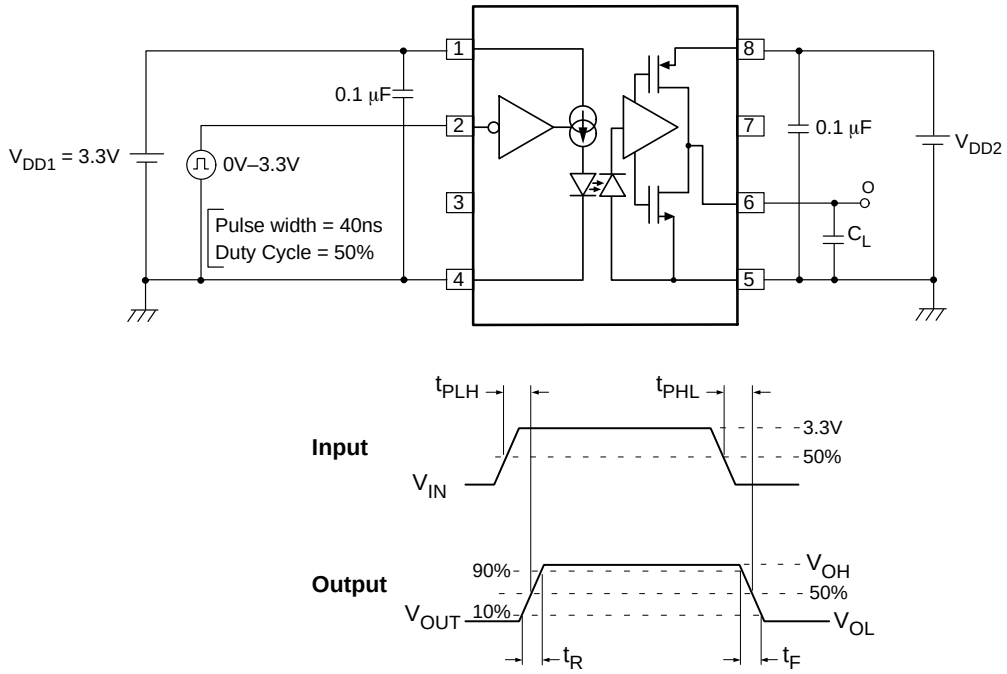


Figure 14. Test Circuit for Propagation Delay and Rise Time, Fall Time

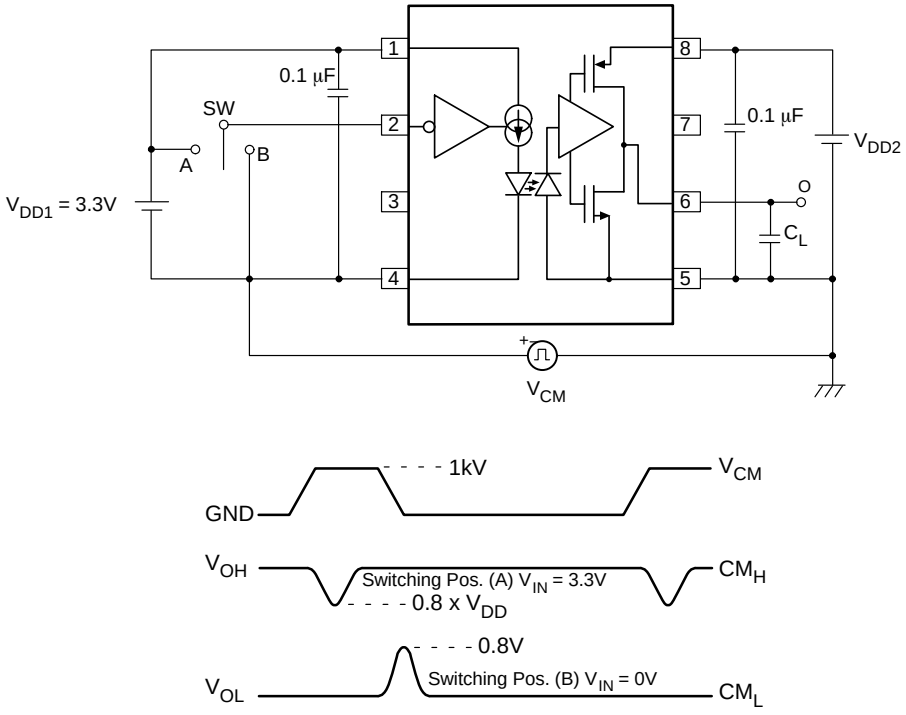


Figure 15. Test Circuit for Instantaneous Common Mode Rejection Voltage

APPLICATION INFORMATION

Noise is defined as any unwanted signal that degrades or interferes with the operation of a system or circuit. Input−output noise rejection is a key characteristic of an optocoupler, and the performance specification for this noise rejection is called, “Common Mode Transient Immunity or Common Mode Rejection, CMR”. The CMR test configuration is presented in high speed optocoupler datasheets, which tests the optocoupler to a specified rate of interfering signal (dv/dt), at a specified peak voltage (Vcm).

This defined noise signal is applied to the test device while the coupler is a stable logic high or logic low state. This test procedure evaluates the interface device in a constant or static logic state. This type of CMR can be referred to as “**Static CMR**”. ON Semiconductor high speed optocouplers, which use an optically transparent, electrically conductive shield, and offer active totem pole logic output have static CMR in excess of 50 kV/μs at peak amplitudes of 1.5 kV to 2.0 kV.

Dynamic Common Mode Rejection

The noise susceptibility of an interface while it is actively transferring data is a common requirement in serial data communication. However, the static CMR specification is not adequate in quantifying the electrical noise susceptibility for optocouplers used in isolating high speed data transfer.

A serial data communication network’s noise performance is usually quantified as the number of bit errors per second or as a ratio of the number of bits transmitted in a specified time frame. This describes Bit Error Rate, BER. Test equipment that evaluates BER is called a Bit Error Rate Tester, BERT. When a BERT system is combined with a CMR tester, the active or dynamic noise rejection of an isolated interface can then be quantified. This type of CMR is thus defined as “**Dynamic CMR**”. Therefore, evaluating the common mode rejection while the optocoupler is switching at high speed represents a realistic approach to understand noise interference.

Test circuit functions were built to interface a commercial pseudo−random bit sequence (PRBS) generator and error detector with a pair of high speed optocouplers, FOD8001, connected in a loop−back configuration. With a 10 MBaud PRBS serial data stream, no error was detected until the common mode voltage rose above 2.5 kV with a dv/dt of 45 kV/μs. And increasing the data rate beyond 10 Mbaud, the test was conducted at 20 MBaud, and no error was detected at dv/dt of 25 kV/μs at common mode voltage of 1.5 kV.

The test data for the dynamic CMR is comparable or better than the static CMR specifications found in the datasheet. These excellent noise rejection performances are results of the innovative circuit design and the patented coplanar assembly process.

Power Supply Noise Rejection

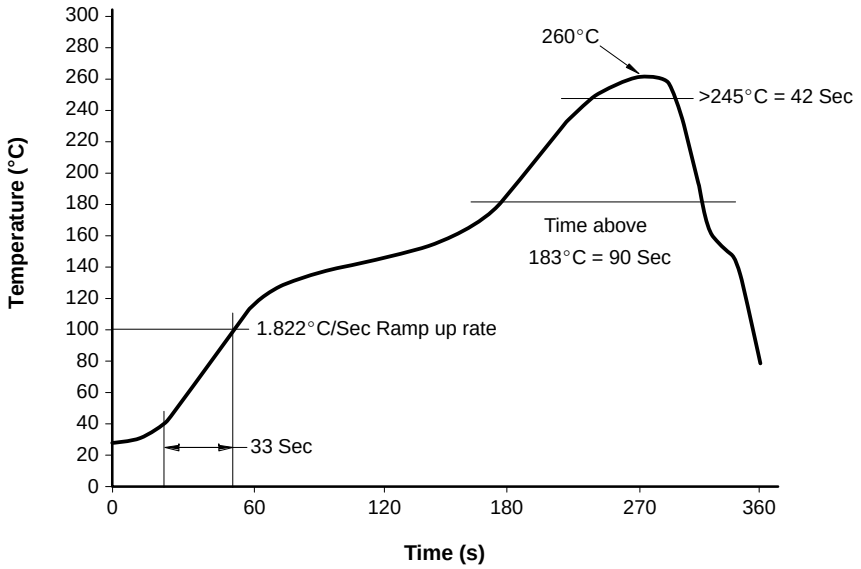
High levels of electrical noise can cause the optocoupler to register the incorrect logic state. The most commonly discussed noise signal is the common mode noise found between the input and output of the optocoupler. However, common mode noise is not the only path of noise into the input or output of the optocoupler. Due to the high gain and wide bandwidth of the transimpedance amplifier used for the photo detector circuits, power supply noise can cause the optocoupler to change state independent of the LED operation. Power supply noise is typically characterized as either random or periodic pulses with varying amplitudes and rates of rise and fall. The necessary tests have been conducted to understand the influence of the power supply noise and its effect of the proper operation of the FOD8001. The optocoupler under test offered power supply noise rejection in excess of 10% of the supply voltage for a frequency ranging from 100 kHz to 35 MHz, for logic high and logic low states.

ORDERING INFORMATION

Option	Order Entry Identifier	Package	Packing Method†
No Suffix	FOD8001	SOIC8 (Pb−Free)*	Tube (50 Units per Tube)
R2	FOD8001R2	SOIC8 (Pb−Free)*	Tape and Reel (2,500 Units per Reel)

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*All packages are lead free per JEDEC: J−STD−020B standard.

REFLOW PROFILE



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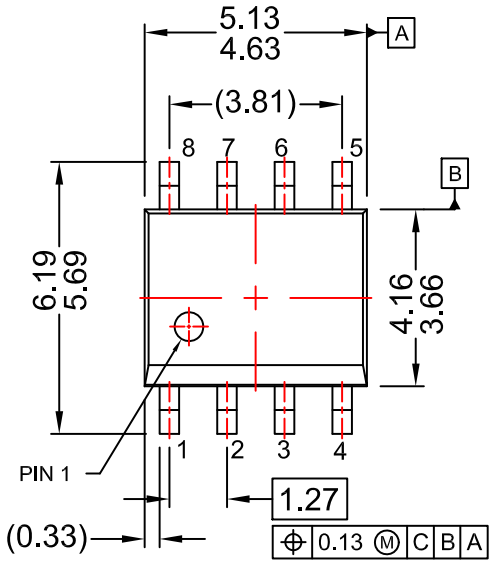
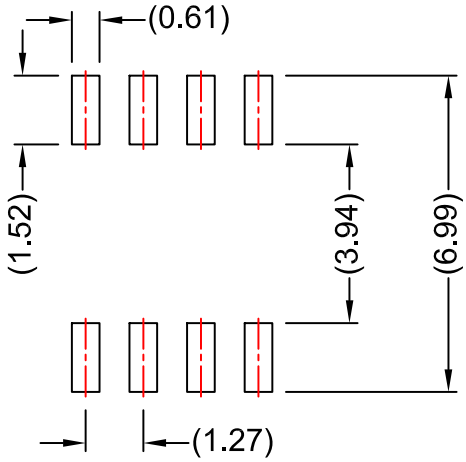
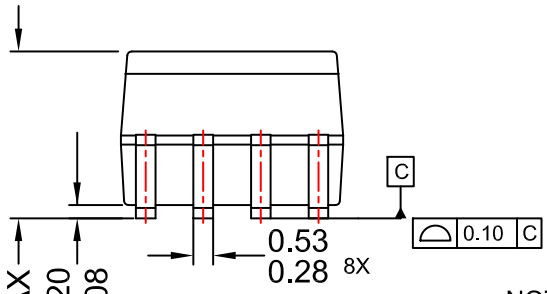
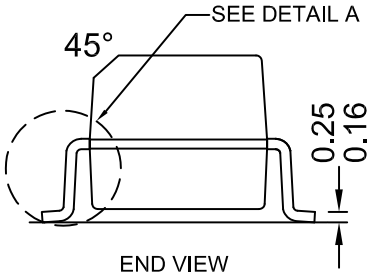
DATE 30 SEP 2016



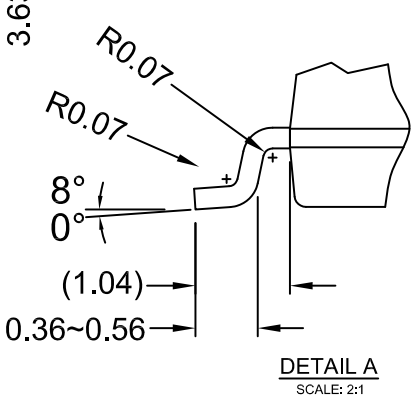


LAND PATTERN RECOMMENDATION





END VIEW



DETAIL A
SCALE: 2:1

NOTES:

A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.

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DESCRIPTION:	**SOIC8**		**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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For additional information, please contact your local Sales Representative

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