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May 2016

FL5150/60
IGBT and MOSFET AC Phase Cut Dimmer Controller

Features

- Selectable Earth Ground or Line-Hot Zero Cross Detection: Complies with UL1472 2015 2nd Edition for Addition of Ground Leakage Current for Flicker Reduction (North America)
- User Programmable Leading or Trailing Edge Dimming Control
- Dynamic Over-Current and Temperature Protection
- Powered from the AC Line
- Symmetric AC Current Control
- IGBT or MOSFET Gate Driver
- Gate Pulse Width Programmable from 0 to 100% t_{ON}
- 8 Bit ADC Input for Dimming Control with an Adjustable Resistor or 0 to 10 V DC Voltage
- 226 Dimming Pulse Widths with 25 μs Resolution and Built-in Ramp Up/Down Control for Smooth Dimming
- Automatically Maximum Gate Pulse Width Control (Auto Max.)
- Minimum External Components
- 600 μA Quiescent Current
- Precision Temperature Compensated 2% Internal Timer
- Low Power Electronic Off State Mode
- Space Savings SOIC 10-pin Package
- 50 Hz and 60 Hz Options

Applications

- Dimmer Switches
- AC Controls

Description

The FL5150 and FL5160 are controllers for varying the pulse width for AC loads. The FL5150 is for 50 Hz and the FL5160 is for 60 Hz applications. The FL5150/60 is powered from the AC line and generates a programmable gate drive for controlling the pulse width for external IGBT or MOSFET transistors. The pulse width can be user programmable with either an external resistor or 0 to 10 V DC signal or controlled by a μP with a logic signal. The pulse width can be controlled from 0 to 100% duty cycle to provide a wide AC symmetric dimming control function when biased with a 3-wire application. For 2-wire Line-Hot and Load-Hot applications, the pulse width can typically be varied from 0 to a maximum gate pulse so that the load voltage is >95% of the AC line voltage. The FL5150/60 will automatically override the pulse width control setting to allow maximum gate pulse width without flicker.

The FL5150/60 takes advantage of the UL1472 2015 2nd edition code revision that allows for up to 0.5 mA of ground leakage current when a neutral wire is not available in the switch box. This improves the flicker performance for non-resistive loads. If the application does not allow ground leakage current then the Line Hot signal can be used as the ZC signal.

The FL5150/60 has user programmable over-current and temperature protection. With external sense resistors, the maximum voltage drop across Q1 and Q2 can be set to limit the maximum current and transistor power dissipation.

The FL5150/60 can be programmed for trailing edge dimming when the DIM Mode pin is low at startup (pulse width starts at the zero-crossing) or leading edge dimming when the DIM Mode pin is connected to the VDD pin at startup (pulse width ends at the zero crossing). When an OFF state is selected (DIM Control pin is 0 V) the FL5150/60 will go into a low power electronic OFF state that reduces the power consumption to less than 100 mW if an external NPN transistor is used.

The FL5150/60 has an internal 8 bit ADC that allows for typically 226 selectable dimming pulse widths with a resolution of 25 μs per step. The FL5150/60 controls the dim pulse width rate of change so that the minimum to maximum dim ramp time is approximately 1 second. This feature allows for a smooth dim transition.

Internally, the FL5150/60 contains a 17 V shunt regulator, 5 V linear regulator, 8Bit ADC, detection comparators, control logic and an IGBT or MOSFET gate driver.

The 10-pin SOIC package provides for a low-cost, compact design and layout.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FL5150MX	-40°C to +85°C	10 Lead SOIC, JEDEC MS-012, 150” Narrow Body	Tape and Reel
FL5160MX			

Typical Applications

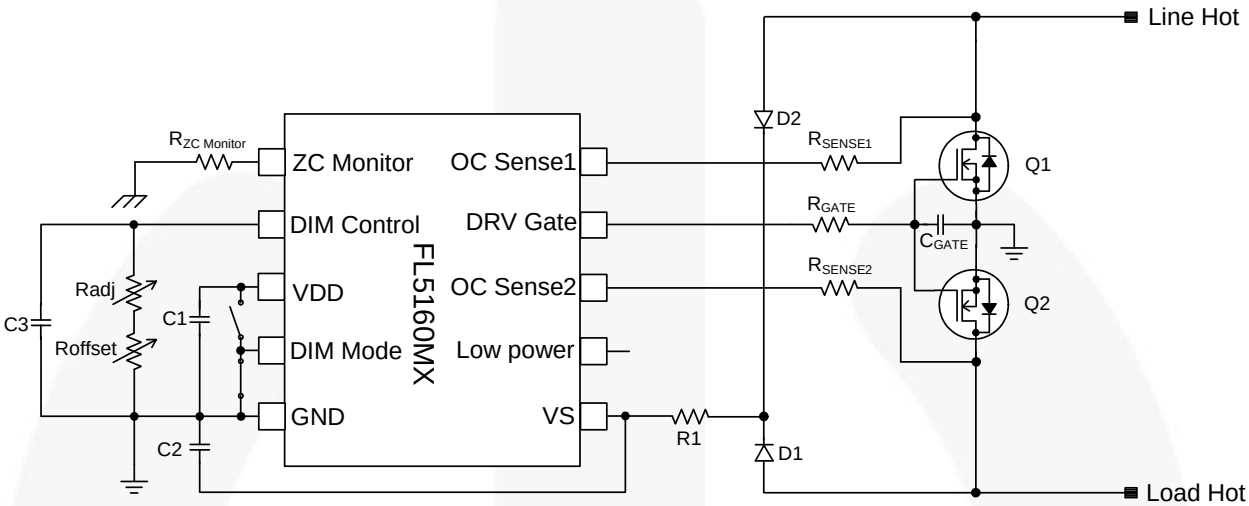

Figure 1. Typical 120 V_{AC} 60 Hz Application with Air Gap Switch (TE Mode Selected)

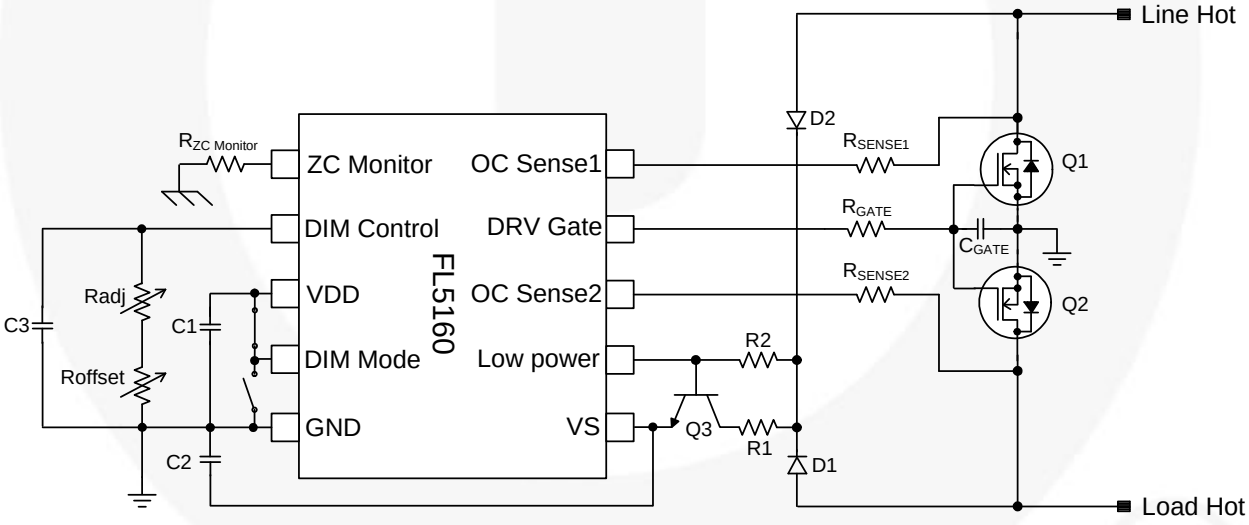

Figure 2. Typical 120 V_{AC} 60 Hz Low Power Application (LE Mode Selected)

Table 1. Typical Values

R1: 10 kΩ	R2: 150 kΩ	R_{ADJ}: 0 to 250 kΩ	R_{OFFSET}: 0 to 50 kΩ	$R_{ZC\ Monitor}$: 1 MΩ	R_{GATE}: 1 kΩ
R_{SENSE1}: 1 MΩ	R_{SENSE2}: 1 MΩ	C1: 100 nF	C2: 2.5 μF	C3: 100 nF	
C_{GATE}: 22 nF	Q1: FDPF33N25	Q2: FDPF33N25	Q3: KSP44		

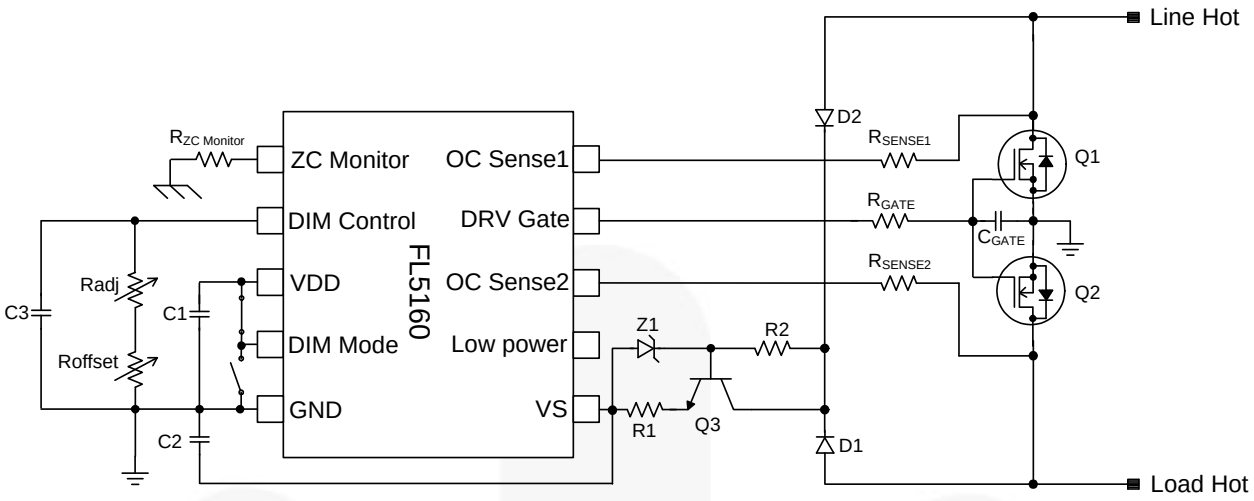

Figure 3. 120 V_{AC} 60 Hz Application with Current Mirror for R1 Lower Power Dissipation (LE Mode Selected)

Table 2. Typical Values

R1: 2 kΩ	R2: 150 kΩ	R_{ADJ}: 0 to 250 kΩ	R_{OFFSET}: 0 to 50 kΩ	$R_{ZC\ Monitor}$: 1 MΩ	R_{GATE}: 1 kΩ
R_{SENSE1}: 1 MΩ	R_{SENSE2}: 1 MΩ	C1: 100 nF	C2: 2.5 μF	C3: 100 nF	C_{GATE}: 22 nF
Z1: 7.5 V	Q1: FDPF33N25	Q2: FDPF33N25	Q3: KSP44		

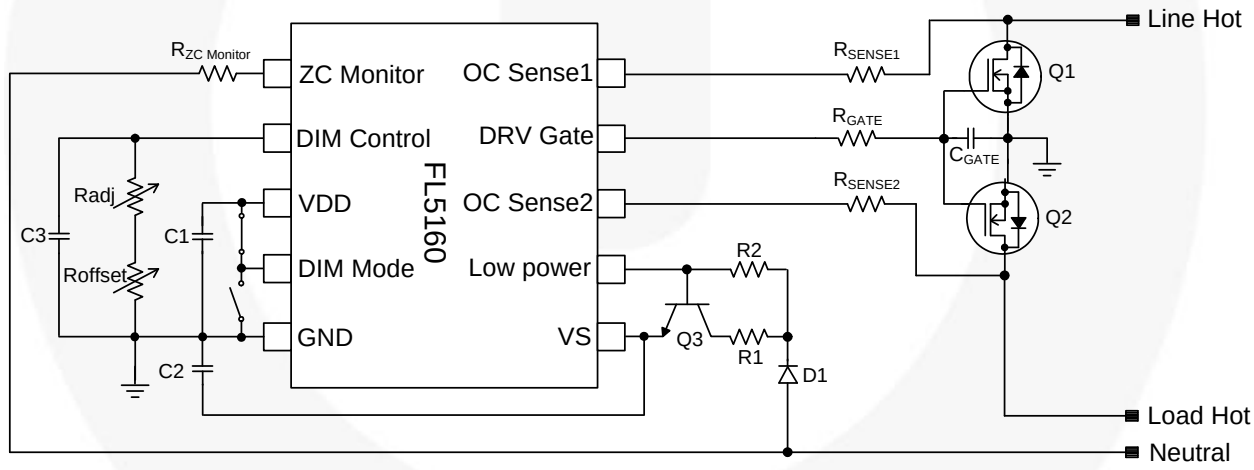

Figure 4. Typical 120 V_{AC} 60 Hz Low Power 3-Wire Application

Table 3. Typical Values

R1: 30 kΩ	R_{ADJ}: 0 to 250 kΩ	R2: 150 kΩ	$R_{ZC\ Monitor}$: 1 MΩ	R_{GATE}: 1 kΩ	R_{SENSE1}: 1 MΩ
R_{SENSE2}: 1 MΩ	C1: 100 nF	C2: 4.7 μF	C_{GATE}: 22 nF	C3: 100 nF	
Q1: FDPF33N25	Q2: FDPF33N25	Q3: KSP44			

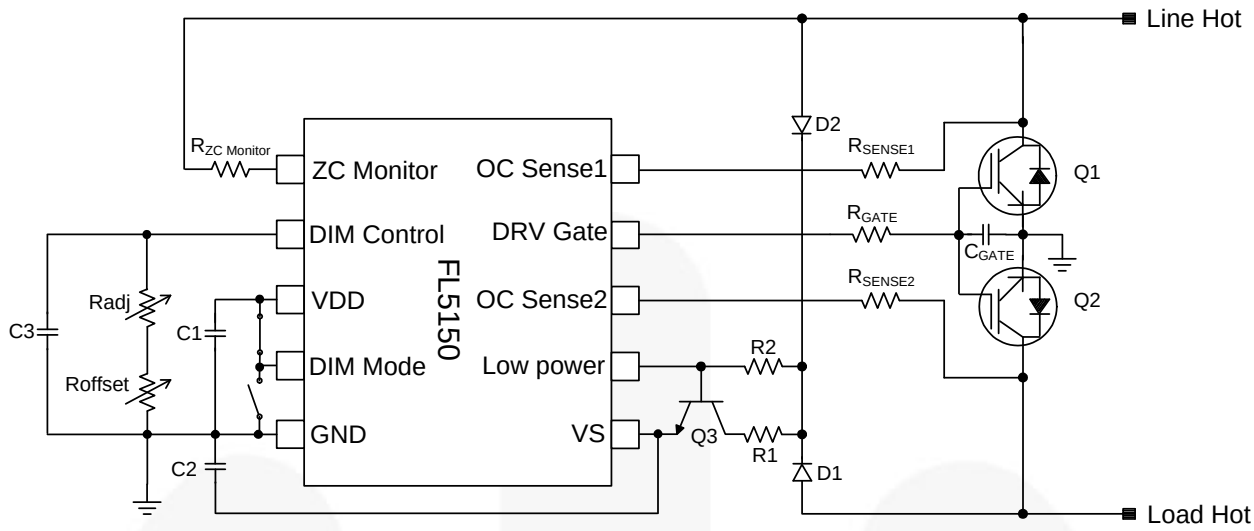

Figure 5. Typical 230 V_{AC} 50 Hz 2-Wire Application (LE Mode Shown)

Table 4. Typical Values

R1: 35 kΩ	R_{ADJ}: 0 to 250 kΩ	R2: 350 kΩ	$R_{ZC\ Monitor}$: 2 MΩ	R_{GATE}: 1 kΩ	R_{SENSE1}: 2 MΩ
R_{SENSE2}: 2 MΩ	C1: 100 nF	C2: 3 μF	C_{GATE}: 22nF	C3: 100 nF	
Q1:NGTB10N60FG	Q2: NGTB10N60FG	Q3: KSP44			

Block Diagram

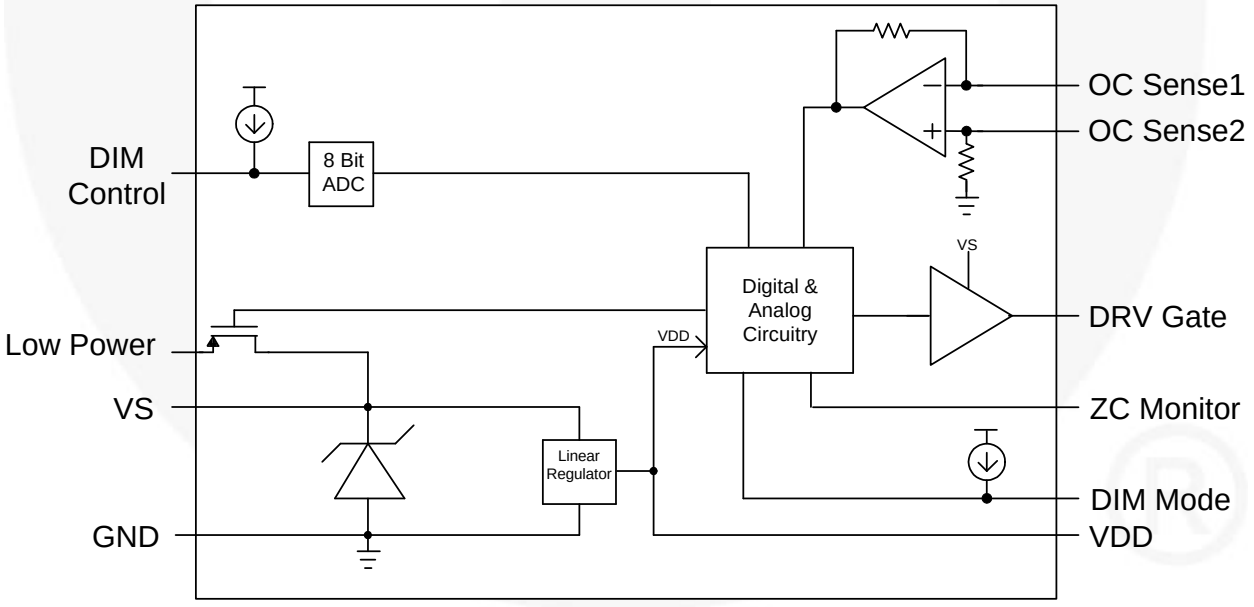

Figure 6. Block Diagram

Pin Configuration

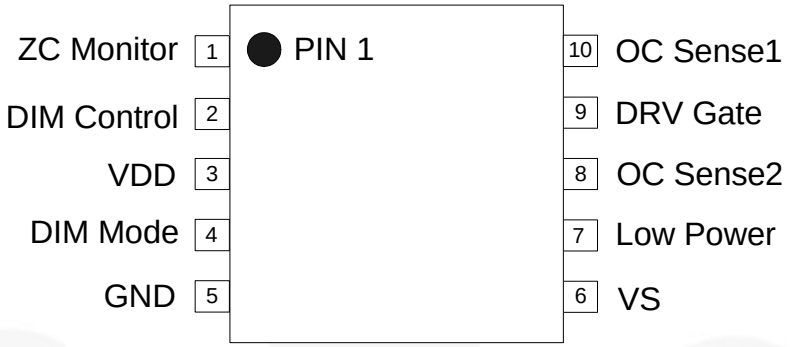

Figure 7. Pin Assignments

Pin Definitions

Pin#	Name	Description
1	ZC Monitor	**ZC Monitor** This signal is used for the zero crossing threshold.
2	DIM Control	**DIM Control** The voltage at this pin is the input for an 8 Bit ADC with a 2.5 V reference. Table 5 shows the pulse width selection per DIM Control pin voltage. This pin sources 10 μA of current so that with an external adjustable resistor, the dim pulse width can be selected. With a 4 to 1 resistor divided, a 0 to 10 V DC (Ground reference to pin 5) signal can be used to control the dim pulse width.
3	VDD	**VDD** The internal 5 V supply for the digital logic
4	DIM Mode	**DIM Mode** This pin selects either trailing edge or leading edge pulse width dimming. When a Power-On-Reset (POR) occurs, this pin will be monitored for its logic level. If it is connected to GND then trailing edge dimming will be selected. If it is connected to VDD then leading edge dimming will be selected. The DIM Mode state is latched at startup (60 ms) and will remain in its selected DIM Mode until a POR signal occurs.
5	GND	**GND** Supply input for the FL5150/60 circuitry
6	VS	**VS** Supply input for the FL5150/60 circuitry. An internal shunt regulator will clamp this pin at 17 V.
7	Low Power	**Low Power** When an off state is selected (DIM Control pin at 0 V) an internal PMOS transistor will be enabled which shorts this pin to VS. If an external NPN transistor is used per Figure 2, the FL5150/60 power consumption will be reduced to typically 100 mW.
8	OC Sense2	**OC Sense2** An external resistor connected to the collector/drain of Q2 sets the maximum voltage difference across Q1 and Q2 for both positive and negative half cycles.
9	DRV Gate	**DRV Gate** Gate drive signal for external IGBT or MOSFET transistors.
10	OC Sense1	**OC Sense1** An external resistor connected to the collector/drain of Q1 sets the maximum voltage difference across Q1 and Q2 for both positive and negative half cycles.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Condition	Min.	Max.	Unit
IS	Supply Current	Continuous Current, VS to GND		25	mA
VS	Supply Voltage	Continuous Voltage, VS to GND	-0.8	20.0	V
DRVG LP	DRV Gate and Low Power	Continuous Voltage to GND	-0.8	20.0	V
OCSen1 OCSen2	Sense1, Sense2	Continuous Voltage to GND	-0.8	5.0	V
	All other pins	Continuous Voltage to GND	-0.8	6.0	
T_{STG}	Storage Temperature Range		-65	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		2	kV
		Charged device Model, JESD22-C101		2	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the data sheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings. Unless otherwise specified, refer to Figure 1 to Figure 5. T_A=25°C, I_{SHUNT}=5 mA, and phase=60 Hz.

Symbol	Parameter		Conditions		Min.	Typ.	Max.	Unit
FL5150/60 Electrical Parameters (T_A=25°C, I_{shunt}=5 mA, unless otherwise specified)								
VS	Power Supply Shunt Regulator Voltage		VS to GND		16	17	18	V
UVLO	Under-Voltage Lockout (Power-on-Reset)		VS to GND, Rising Enable FL5160/50		9.2	9.5	9.8	V
			VS to GND, Falling Hysteresis Terminate DRV Gate Pulse			0.5		
			VS to GND, Falling Hysteresis Disable FL5150/60			2.2		
I_Q	Quiescent Current		VS to GND = 12 V			600	800	µA
VDD	VDD Supply Voltage		VPW Control = 0		4.5	5.0	5.5	V
$OCSen1_{VH}$ $OCSen2_{VH}$	Sense1&2 Clamp High		IH = 350 µA				4.0	V
$OCSen1_{VL}$ $OCSen2_{VL}$	Sense1&2 Clamp Low		IL = -350 µA		-0.7			V
$ZCMon_{VH}$	ZC Monitor Clamp High		IH = 350 µA				4.0	V
$ZCMon_{VL}$	ZC Monitor Clamp Low		IH = -350 µA		-0.7			V
OSC	Internal Timer	FL5160	VDIM Control = 0		194	200	206	kHz
		FL5150			161.7	166.7	171.7	
$DIMCN_{ISOURCE}$	DIM Control Source Current		VDIM Control = 0		9.4	10.0	10.6	µA
$DIMCN_{VFORCE}$	DIM Control 100% Duty Cycle		VDIM Control		VDD – 0.5			V
$VREF_{ADC}$	ADC Reference Voltage		VADC (8-Bit)			2.56		V
$DRVG_{VH}$	DRV Gate High		RADJ Open (VS=17 V)		16.0	17.0		V
$DRVG_{VL}$	DRV Gate Low		RADJ Connected to GND				100	mV
$DRVG_{TLH}$	DRV Gate L to H		CLoad = 3 nF, 10 to 90%			150	250	ns
$DRVG_{THL}$	DRV Gate H to L		CLoad = 3 nF, 10 to 90%			50	100	ns
DM_{VL}	DIM Mode Logic Low (Select Trailing Edge)		VL				1.0	V
DM_{VH}	DIM Mode Logic High (Select Leading Edge)		VH		VDD - 1.0			V
$DM_{ISOURCE}$	DIM Mode Source Current		IDIM Mode		7	10	13	µA
DM_{TSEL}	DIM Mode Selection Time after Under-Voltage lock Out Enable Threshold		FL5160			60		ms
			FL5150			72		
LPM_{TEN}	LP Mode Enable Time		FL5160, VDIM Control = 0			100		ms
			FL5150, VDIM Control = 0			120		
OC_{VTH}	Over-Current Threshold, Trailing Edge R_{SENSE}1,2 =1 MΩ I Q1DRAIN – Q2DRAIN I		Half Cycle Phase Angle	0 to 43°		3.5		V
				43° to 65°		2.9		
				65° to 86°		2.4		
				86° to 180°		2.0		

Table 5. DIM Control Voltage Pulse Width Selection[1]

		DIM Mode=0	DIM Mode=0	DIM Mode=1	DIM Mode=1
		Trailing Edge	Trailing Edge	Leading Edge	Leading Edge
DIM_Control Voltage (mV)	$VOUT_{RMS}$(V)[2]	t_{ON} (Rising) μs	t_{ON} (Falling) μs	t_{OFF} (Rising) μs	t_{OFF} (Falling) μs
0	0	0	0	>8333	>8333
0	0	0	0	>8333	>8333
0	0	0	0	>8333	>8333
0	0	0	0	>8333	>8333
40	0	0	0	>8333	>8333
50	0	0	500	>8333	7800
60	0	0	500	>8333	7800
70	0	0	500	>8333	7800
80	0	0	500	>8333	7800
90	0	0	500	>8333	7800
100	4.5	500	500	7800	7800
110	5.3	550	550	7750	7750
120	6.1	600	600	7700	7700
130	6.9	650	650	7650	7650
140	7.7	700	700	7600	7600
150	8.5	750	750	7550	7550
160	9.4	800	800	7500	7500
170	10.3	850	850	7450	7450
180	11.2	900	900	7400	7400
190	12.1	950	950	7350	7350
200	13	1000	1000	7300	7300
210	14	1050	1050	7250	7250
220	15	1100	1100	7200	7200
230	16	1150	1150	7150	7150
240	17	1200	1200	7100	7100
250	18	1250	1250	7050	7050
260	18.5	1275	1275	7025	7025
270	19	1300	1300	7000	7000
280	19.5	1325	1325	6975	6975
290	20	1350	1350	6950	6950
300	20.5	1375	1375	6925	6925
310	21	1400	1400	6900	6900
320	21.5	1425	1425	6875	6875
330	22	1450	1450	6850	6850
340	22.5	1475	1475	6825	6825
350	23	1500	1500	6800	6800

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Table 5. DIM Control Voltage Pulse Width Selection[1] (Continued)

		DIM Mode=0	DIM Mode=0	DIM Mode=1	DIM Mode=1
		Trailing Edge	Trailing Edge	Leading Edge	Leading Edge
DIM_Control Voltage (mV)	$VOUT_{RMS}$(V)[2]	t_{ON} (Rising) µs	t_{ON} (Falling) µs	t_{OFF} (Rising) µs	t_{OFF} (Falling) µs
360	23.6	1525	1525	6775	6775
370	24.2	1550	1550	6750	6750
380	24.8	1575	1575	6725	6725
390	25.4	1600	1600	6700	6700
400	26	1625	1625	6675	6675
410	26.6	1650	1650	6650	6650
420	27.2	1675	1675	6625	6625
430	27.8	1700	1700	6600	6600
440	28.4	1725	1725	6575	6575
450	29	1750	1750	6550	6550
460	29.6	1775	1775	6525	6525
470	30.2	1800	1800	6500	6500
480	30.8	1825	1825	6475	6475
490	31.4	1850	1850	6450	6450
500	32	1875	1875	6425	6425
510	32.6	1900	1900	6400	6400
520	33.2	1925	1925	6375	6375
530	33.8	1950	1950	6350	6350
540	34.4	1975	1975	6325	6325
550	35	2000	2000	6300	6300
560	35.6	2025	2025	6275	6275
570	36.2	2050	2050	6250	6250
580	36.8	2075	2075	6225	6225
590	37.4	2100	2100	6200	6200
600	38	2125	2125	6175	6175
610	38.6	2150	2150	6150	6150
620	39.2	2175	2175	6125	6125
630	39.8	2200	2200	6100	6100
640	40.4	2225	2225	6075	6075
650	41	2250	2250	6050	6050
660	41.6	2275	2275	6025	6025
670	42.2	2300	2300	6000	6000
680	42.8	2325	2325	5975	5975
690	43.4	2350	2350	5950	5950
700	44	2375	2375	5925	5925
710	44.6	2400	2400	5900	5900

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Table 5. DIM Control Voltage Pulse Width Selection[1] (Continued)

		DIM Mode=0	DIM Mode=0	DIM Mode=1	DIM Mode=1
		Trailing Edge	Trailing Edge	Leading Edge	Leading Edge
DIM_Control Voltage (mV)	$VOUT_{RMS}$(V)[2]	t_{ON} (Rising) µs	t_{ON} (Falling) µs	t_{OFF} (Rising) µs	t_{OFF} (Falling) µs
720	45.2	2425	2425	5875	5875
730	45.8	2450	2450	5850	5850
740	46.4	2475	2475	5825	5825
750	47	2500	2500	5800	5800
760	47.6	2525	2525	5775	5775
770	48.2	2550	2550	5750	5750
780	48.8	2575	2575	5725	5725
790	49.4	2600	2600	5700	5700
800	50	2625	2625	5675	5675
810	50.6	2650	2650	5650	5650
820	51.2	2675	2675	5625	5625
830	51.8	2700	2700	5600	5600
840	52.4	2725	2725	5575	5575
850	53	2750	2750	5550	5550
860	53.6	2775	2775	5525	5525
870	54.2	2800	2800	5500	5500
880	54.8	2825	2825	5475	5475
890	55.4	2850	2850	5450	5450
900	56	2875	2875	5425	5425
910	56.6	2900	2900	5400	5400
920	57.2	2925	2925	5375	5375
930	57.8	2950	2950	5350	5350
940	58.4	2975	2975	5325	5325
950	59	3000	3000	5300	5300
960	59.6	3025	3025	5275	5275
970	60.2	3050	3050	5250	5250
980	60.8	3075	3075	5225	5225
990	61.4	3100	3100	5200	5200
1000	62	3125	3125	5175	5175
1010	62.6	3150	3150	5150	5150
1020	63.2	3175	3175	5125	5125
1030	63.8	3200	3200	5100	5100
1040	64.4	3225	3225	5075	5075
1050	65	3250	3250	5050	5050
1060	65.6	3275	3275	5025	5025
1070	66.2	3300	3300	5000	5000

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Table 5. DIM Control Voltage Pulse Width Selection[1] (Continued)

		DIM Mode=0	DIM Mode=0	DIM Mode=1	DIM Mode=1
		Trailing Edge	Trailing Edge	Leading Edge	Leading Edge
DIM_Control Voltage (mV)	$VOUT_{RMS}$(V)[2]	t_{ON} (Rising) µs	t_{ON} (Falling) µs	t_{OFF} (Rising) µs	t_{OFF} (Falling) µs
1080	66.8	3325	3325	4975	4975
1090	67.4	3350	3350	4950	4950
1100	68	3375	3375	4925	4925
1110	68.6	3400	3400	4900	4900
1120	69.2	3425	3425	4875	4875
1130	69.8	3450	3450	4850	4850
1140	70.4	3475	3475	4825	4825
1150	71	3500	3500	4800	4800
1160	71.6	3525	3525	4775	4775
1170	72.2	3550	3550	4750	4750
1180	72.8	3575	3575	4725	4725
1190	73.4	3600	3600	4700	4700
1200	74	3625	3625	4675	4675
1210	74.6	3650	3650	4650	4650
1220	75.2	3675	3675	4625	4625
1230	75.8	3700	3700	4600	4600
1240	76.4	3725	3725	4575	4575
1250	77	3750	3750	4550	4550
1260	77.5	3775	3775	4525	4525
1270	78	3800	3800	4500	4500
1280	78.5	3825	3825	4475	4475
1290	79	3850	3850	4450	4450
1300	79.5	3875	3875	4425	4425
1310	80	3900	3900	4400	4400
1320	80.5	3925	3925	4375	4375
1330	81	3950	3950	4350	4350
1340	81.5	3975	3975	4325	4325
1350	82	4000	4000	4300	4300
1360	82.5	4025	4025	4275	4275
1370	83	4050	4050	4250	4250
1380	83.5	4075	4075	4225	4225
1390	84	4100	4100	4200	4200
1400	84.5	4125	4125	4175	4175
1410	85	4150	4150	4150	4150
1420	85.5	4175	4175	4125	4125
1430	86	4200	4200	4100	4100

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Table 5. DIM Control Voltage Pulse Width Selection[1] (Continued)

		DIM Mode=0	DIM Mode=0	DIM Mode=1	DIM Mode=1
		Trailing Edge	Trailing Edge	Leading Edge	Leading Edge
DIM_Control Voltage (mV)	$VOUT_{RMS}$(V)[2]	t_{ON} (Rising) μs	t_{ON} (Falling) μs	t_{OFF} (Rising) μs	t_{OFF} (Falling) μs
1440	86.5	4225	4225	4075	4075
1450	87	4250	4250	4050	4050
1460	87.5	4275	4275	4025	4025
1470	88	4300	4300	4000	4000
1480	88.5	4325	4325	3975	3975
1490	89	4350	4350	3950	3950
1500	89.5	4375	4375	3925	3925
1510	90	4400	4400	3900	3900
1520	90.5	4425	4425	3875	3875
1530	91	4450	4450	3850	3850
1540	91.5	4475	4475	3825	3825
1550	92	4500	4500	3800	3800
1560	92.4	4525	4525	3775	3775
1570	92.8	4550	4550	3750	3750
1580	93.2	4575	4575	3725	3725
1590	93.6	4600	4600	3700	3700
1600	94	4625	4625	3675	3675
1610	94.4	4650	4650	3650	3650
1620	94.8	4675	4675	3625	3625
1630	95.2	4700	4700	3600	3600
1640	95.6	4725	4725	3575	3575
1650	96	4750	4750	3550	3550
1660	96.4	4775	4775	3525	3525
1670	96.8	4800	4800	3500	3500
1680	97.2	4825	4825	3475	3475
1690	97.6	4850	4850	3450	3450
1700	98	4875	4875	3425	3425
1710	98.4	4900	4900	3400	3400
1720	98.8	4925	4925	3375	3375
1730	99.2	4950	4950	3350	3350
1740	99.6	4975	4975	3325	3325
1750	100	5000	5000	3300	3300
1760	100.4	5025	5025	3275	3275
1770	100.8	5050	5050	3250	3250
1780	101.2	5075	5075	3225	3225
1790	101.6	5100	5100	3200	3200

Continued on the following page…

Table 5. DIM Control Voltage Pulse Width Selection[1] (Continued)

		DIM Mode=0	DIM Mode=0	DIM Mode=1	DIM Mode=1
		Trailing Edge	Trailing Edge	Leading Edge	Leading Edge
DIM_Control Voltage (mV)	$VOUT_{RMS}$(V)[2]	t_{ON} (Rising) μs	t_{ON} (Falling) μs	t_{OFF} (Rising) μs	t_{OFF} (Falling) μs
1800	102	5125	5125	3175	3175
1810	102.4	5150	5150	3150	3150
1820	102.8	5175	5175	3125	3125
1830	103.2	5200	5200	3100	3100
1840	103.6	5225	5225	3075	3075
1850	104	5250	5250	3050	3050
1860	104.4	5275	5275	3025	3025
1870	104.8	5300	5300	3000	3000
1880	105.2	5325	5325	2975	2975
1890	105.6	5350	5350	2950	2950
1900	106	5375	5375	2925	2925
1910	106.4	5400	5400	2900	2900
1920	106.8	5425	5425	2875	2875
1930	107.2	5450	5450	2850	2850
1940	107.6	5475	5475	2825	2825
1950	108	5500	5500	2800	2800
1960	108.3	5525	5525	2775	2775
1970	108.6	5550	5550	2750	2750
1980	108.9	5575	5575	2725	2725
1990	109.2	5600	5600	2700	2700
2000	109.5	5625	5625	2675	2675
2010	109.8	5650	5650	2650	2650
2020	110.1	5675	5675	2625	2625
2030	110.4	5700	5700	2600	2600
2040	110.7	5725	5725	2575	2575
2050	111	5750	5750	2550	2550
2060	111.3	5775	5775	2525	2525
2070	111.6	5800	5800	2500	2500
2080	111.9	5825	5825	2475	2475
2090	112.2	5850	5850	2450	2450
2100	112.5	5875	5875	2425	2425
2110	112.8	5900	5900	2400	2400
2120	113.1	5925	5925	2375	2375
2130	113.4	5950	5950	2350	2350
2140	113.7	5975	5975	2325	2325
2150	113	6000	6000	2300	2300

Continued on the following page…

Table 5. DIM Control Voltage Pulse Width Selection[1] (Continued)

		DIM Mode=0	DIM Mode=0	DIM Mode=1	DIM Mode=1
		Trailing Edge	Trailing Edge	Leading Edge	Leading Edge
DIM_Control Voltage (mV)	$VOUT_{RMS}$(V)[2]	t_{ON} (Rising) µs	t_{ON} (Falling) µs	t_{OFF} (Rising) µs	t_{OFF} (Falling) µs
2160	113.2	6025	6025	2275	2275
2170	113.4	6050	6050	2250	2250
2180	113.6	6075	6075	2225	2225
2190	113.8	6100	6100	2200	2200
2200	114	6125	6125	2175	2175
2210	114.2	6150	6150	2150	2150
2220	114.4	6175	6175	2125	2125
2230	114.6	6200	6200	2100	2100
2240	114.8	6225	6225	2075	2075
2250	115	6250	6250	2050	2050
2260	115.2	6275	6275	2025	2025
2270	115.4	6300	6300	2000	2000
2280	115.6	6325	6325	1975	1975
2290	115.8	6350	6350	1950	1950
2300	116	6375	6375	1925	1925
2310	116.2	6400	6400	1900	1900
2320	116.4	6425	6425	1875	1875
2330	116.6	6450	6450	1850	1850
2340	116.8	6475	6475	1825	1825
2350	117	6500	6500	1800	1800
2360	117.2	6525	6525	1775	1775
>4000[3]	119	8.333	8.333	0	0

Notes:

1. The pulse width times shown in Table 5 are reference to the ZC threshold. For trailing edge DIM mode, the pulse width time is the gate t_{ON} time. For leading edge DIM mode, the pulse width time is the gate t_{OFF} time. The shown pulse width time is typical for the FL5160. For the FL5150, the values will be scaled by +20%.
2. $VOUT_{RMS}$ typical value with a 60 W incandescent Load and 120 V_{RMS} input.
3. If the DIM Control voltage is >4 V a 100% duty cycle is selected and the DRV Gate will be on 100%. However, a 100% duty cycle can only occur for a 3-wire application. If a 2-wire application is used and the DIM Control pin voltage is >4 V a POR will occur

Description

(Refer to Figure 1 to Figure 5)

Present AC controls or dimmer switches typically use TRIAC circuits to generate the AC symmetric chopped or phase cut current function. The TRIAC is basically two back to back SCR transistors that allow for symmetric AC operation in both the positive and negative half cycles. The TRIAC dimmer circuit controls the AC voltage pulse width to the load by turning off the TRIAC when its holding current is below the minimum threshold level. This occurs near the AC zero-crossing. The TRIAC is turned on at a selected phase angle during the half cycle. The TRIAC minimum holding current can become an issue for newer low wattage lighting products. In addition, newer lighting products typically have capacitive load impedance so the current and voltage phases are shifted. This can cause problems for the detection of the AC zero-cross signal and lead to unwanted flickering.

The FL5150/60 controller addresses these issues by controlling back to back MOSFET or IGBT transistors which can be turned on or off at any time during the AC half cycle. In addition, the FL5160 can use the earth ground leakage current to better determine the zero-cross threshold for non-resistive loads. Up to 500 µA of ground leakage current is now allowed per the UL1472 2nd edition specification for 2-wire applications.

The FL5160 product is for North America 120 V_{AC}, 60 Hz applications and the FL5150 product is for 230 V_{AC}, 50 Hz applications. The internal timing oscillator is selected for 50 Hz for the FL5150 and 60 Hz for the FL5160. For the below description, the timing information is in reference to the FL5160 60 Hz option. For the FL5150 option, the t_{ON} pulse width is scaled by +20%.

The FL5160 has a selectable DIM Mode pin that allows for either Trailing Edge or Leading Edge dimming modulation. At startup when an under-voltage lockout enable signal is detected (POR) the DIM Mode pin is monitored for its logic state and after 60ms this state will be latched and program the FL5160 for either trailing edge dimming if this pin is low or leading edge dimming if this pin is high. The DIM Mode pin enables a 10 µA pull up current source after Power-on-Reset (POR). Once the dimming mode is latched, this pin will be disabled until a POR enable signal occurs. For trailing edge dimming, the gate pulse is enabled at the ZC signal and disabled after the t_{ON} pulse width per Table 5. For leading edge dimming, the gate pulse is disabled at the ZC signal and enabled after the t_{OFF} pulse width per Table 5.

The gate pulse width is determined by the value of the voltage at the DIM Control pin. The DIM Control pin sources a 10 µA current. The voltage at this pin is connected to an 8 Bit ADC with an internal full scale reference of 2.56 V so the ADC step size is ~10 mV. Table 5 shows the gate pulse width versus the DIM Control pin voltage for a 60 Hz FL5160 application. If the DIM Control pin is connected to VDD a force 100% duty cycle will be selected. However, if the VS voltage drops to the POR voltage threshold a logic reset will occur. A 100% duty cycle can only be selected for a 3-wire application (Neutral wire present).

When the voltage on the DIM Control pin is changed, the FL5160 will increase or decrease the dim steps by one step every 4.17 ms (or two steps per half cycle). This provides for a smooth dim pulse width transition. From minimum to maximum pulse width, the FL5160 will control the dim ramp rate to about 1 second.

The FL5160 has an internal difference amplifier which measures the voltage difference across Q1 and Q2. With the external OC Sense 1&2 resistors, this diff amp will measure the voltage difference across the collectors or drains of Q1 and Q2 when the DRV Gate signal is high. If the maximum voltage threshold is exceeded for longer than 50µs the gate pulse will be disabled until the next AC zero-crossing. This feature will limit the maximum load current and also limit the power dissipation for Q1 and Q2. If 16 consecutive over current pulses occur (*see Figure 12*) the FL5160 will disable the DRV gate and require a POR to reset the disable state. The OC (over-current) trip threshold is dynamic: it is a function of the V_{AC} phase angle. The OC threshold is higher at startup to allow for higher transient currents during startup typical of incandescent bulbs.

The desired steady state (phase angle> 90°) over-current threshold can be programmed with the following equation:

$$\begin{aligned} &| Q1_{VD} - Q2_{VD} | = 2 \times R_{SENSE} \\ &I_{OC} \times R_{DSON} + V_F = 2 \times R_{SENSE} \end{aligned} \quad (1)$$

Where:
R_{DSON} = MOSFET drain to source resistance
V_F = MOSFET body diode

So,

$$\begin{aligned} &I_{OC} = (2 \times R_{SENSE} - VF) / R_{DSON} \\ &\text{note: } R_{SENSE} \text{ in M}\Omega \end{aligned} \quad (2)$$

For the FDPF33N25 transistor,

$$\begin{aligned} &R_{DSON}= 94\ m\Omega \text{ and } V_F = 0.7\ V\ @25°C \\ &R_{DSON}= 170\ m\Omega \text{ and } V_F = 0.6\ V\ @100°C \end{aligned} \quad (3)$$

So,

$$\begin{aligned} &I_{OC} = 13.8\ A\ @25°C \text{ with } R_{SENSE} = 1\ M\Omega \\ &I_{OC} = 8.2\ A\ @100°C \text{ with } R_{SENSE} = 1\ M\Omega \end{aligned} \quad (4)$$

The FL5160 has a low power electronic off state feature. If an external NPN transistor is connected per Figure 2, the power consumption for the OFF state can be significantly reduced. When an OFF state is selected (DIM Control pin at 0 V) an internal 100 ms timer starts. After the timer expires, the FAN5160 will enable an internal PMOS transistor which shorts the Low power and VS pins. This will turn off Q3 which de-biases R1. The FL5160 is now biased by R2. This reduces the electronic off state power consumption from 1 W to 100 mW for a 120 V_{AC} input.

Figure 4 shows a typical 3 wire application. For a three wire application, the neutral wire is available in addition to the Line Hot and Load Hot connections. External components D1, R1 and C2 provide for the DC bias of the FL5160. During the AC half cycle when Line Neutral is positive, the C2 capacitor will charge positive and be clamped to 17 V by the FL5160's shunt regulator connected to VS. The gate driver circuit is supplied from the VS pin. During the AC half cycle when Line Neutral is negative, the FL5160 is biased by the capacitor C2. Figure 8 shows the VS, DRV Gate and load current waveforms for a LED load. The pulse width can be controlled from 0 to 100% duty cycle with a 3-wire application. The R_{ZC} Monitor resistor detects the AC zero crossing. The typical value for this resistor is 1 MΩ for 120 V_{AC} applications.

Figure 1 shows a typical 120 V_{AC} 2-wire application. This 2-wire application does not have the neutral wire available, which is typical for most switch box applications in North America: only the Line Hot, Load Hot and earth ground wires are available. The FL5160 is powered from the AC line by D1, D2, R1 and C2.

Capacitor C2 charges when the Q1 & Q2 transistors are off. When Q1 and Q2 are on, C2 provides the bias for the FAN5160. Since C2 can only charge when both Q1 and Q2 are off, a 100% duty cycle is not possible. The maximum duty cycle is determined by the load; however, because the FL5160 has a low quiescent current, an output voltage typically >95% of the AC Line voltage is possible. Figure 9 shows the VS, DRV Gate and load current waveforms for a LED load. For the R1 and C2 values shown, a maximum gate pulse of 6.5 ms is possible. However, some LED loads will not allow a 6.5 ms maximum gate pulse. The FL5160 has a DIM Control override feature for LED loads that do not support a maximum gate pulse of 6.5 ms (Auto Max.). The FL5160 detects when the maximum gate pulse width occurs and overrides the DIM Control voltage to provide the maximum Load voltage without flicker. This feature automatically adjusts per the Load impedance.

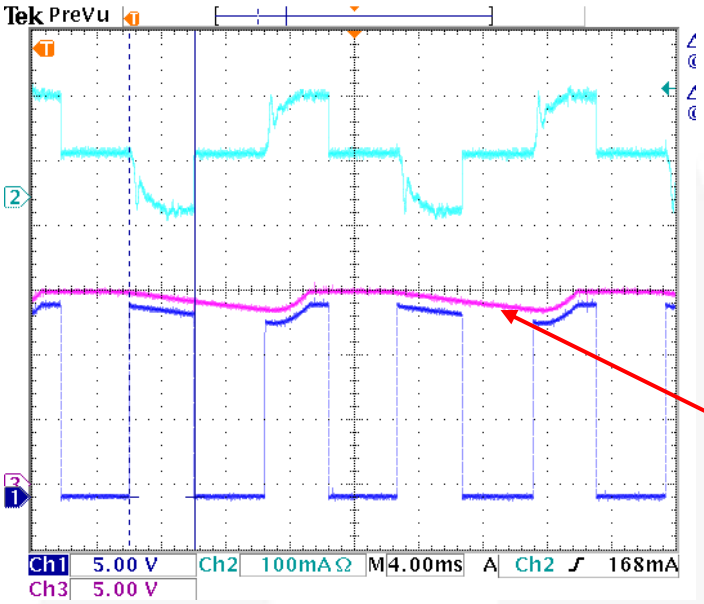
The power dissipation for R1 (Figure 1) is highest when an off state is selected. To reduce the power dissipation for R1, an emitter follower current mirror circuit can be used as shown per Figure 3. Zener Z1 (7.5 V) will bias R1 so ~3.5 mA flows through R1, independent of the VAC voltage. The power dissipation for R1 will be ~25 mW. The power dissipation for Q3 will be ~425 mW.

The above description refers predominantly to the FL5160 functionality. The FL5150 controller is the same as the FL5160 except the internal timer is trimmed for a 50 Hz AC frequency.

Whereas the above applications refer to V_{AC} input voltages of 120 and 230, other AC voltages can be used as long as the discrete components are correctly scaled.

Typical Performance Characteristics

Unless otherwise specified, T_A=25°C and according to Figure 1 to Figure 5.



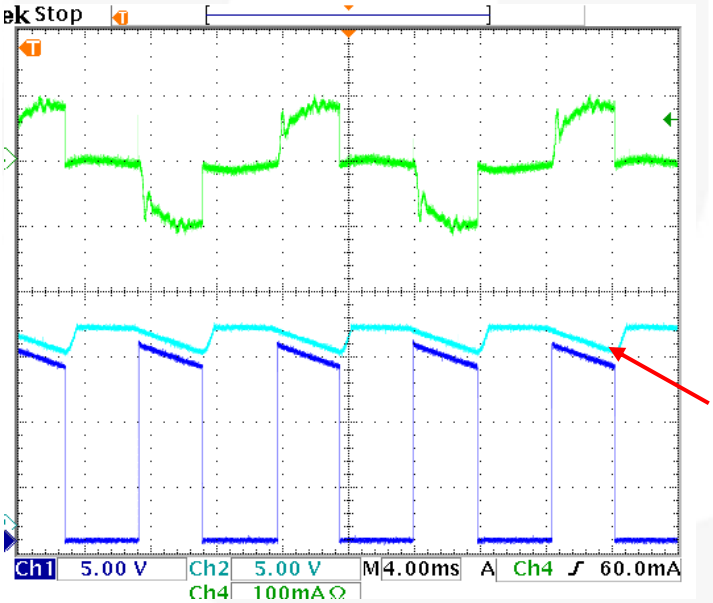
Ch1: DRV Gate (Pin 9) 5 V/Div

Ch2: Load Current 100 mA/Div

Ch3: VS (Pin 6) 5 V/Div

VS discharges during the positive half cycle.

Figure 8. Typical 120 V_{AC} 60 Hz 3-Wire Waveforms with an 8 W LED Load (TE Mode)



Ch1: DRV Gate (Pin 9) 5 V/Div

Ch2: VS (Pin 6) 5 V/Div

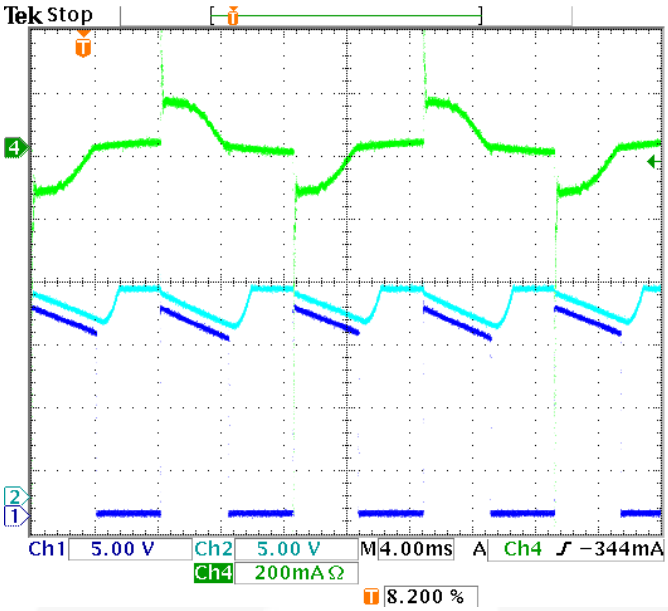
Ch4: Load Current 100 mA/Div

VS discharges when Q1 & Q2 are on.

Figure 9. Typical 120 V_{AC} 60 Hz 2-Wire Waveforms with an 8 W LED Load (TE Mode)

Typical Performance Characteristics (Continued)

Unless otherwise specified, T_A=25°C and according to Figure 1 to Figure 5.

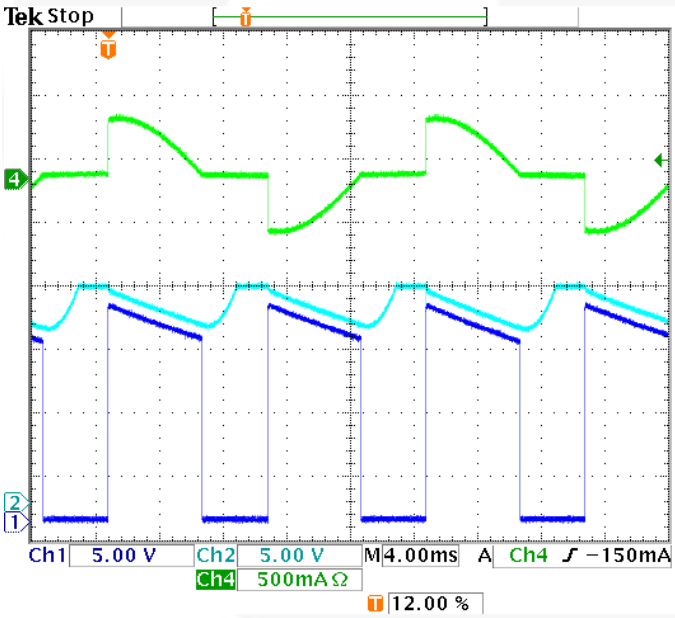


Ch1: DRV Gate (Pin 9) 5 V/Div

Ch4: Load Current 200 mA/Div

Ch2: VS (Pin6) 5 V/Div

Figure 10. Typical 120 V_{AC} 60 Hz 2-Wire Waveforms with an 11 W LED Load (LE Mode)



Ch1: DRV Gate (Pin 9) 5 V/Div

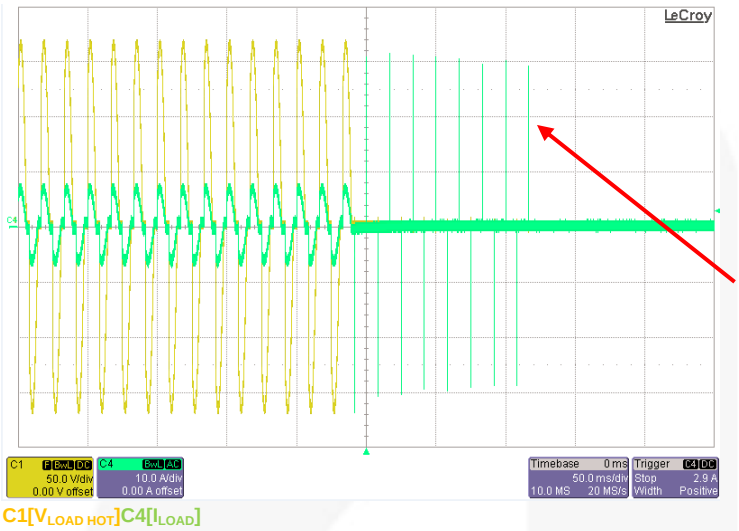
Ch4: Load Current 500 mA/Div

Ch2: VS (Pin 6) 5 V/Div

Figure 11. Typical 230 V_{AC} 50 Hz 2-Wire Waveforms with a 60 W Incandescent Load (LE Mode)

Typical Performance Characteristics (Continued)

Unless otherwise specified, T_A=25°C and according to Figure 1 to Figure 5.



Ch1: $V_{LOAD\ HOT}$ 50 V/Div

Ch4: I_{LOAD} 10 A/Div

Shown is a steady state 600 W incandescent Load

An additional 300 W incandescent Load is added to the 600 W Load. The peak current is limited to ~30 A for 50 µs and after 16-consecutive over-current pulses the DRV Gate signal is disabled

Figure 12. Over-Current Protection

Typical Temperature Characteristics

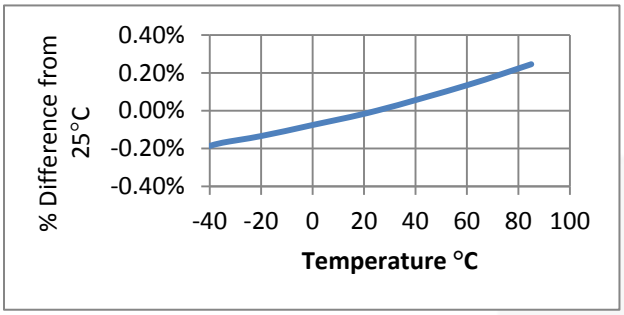


Figure 13. Shunt Regulator Voltage vs. Temperature

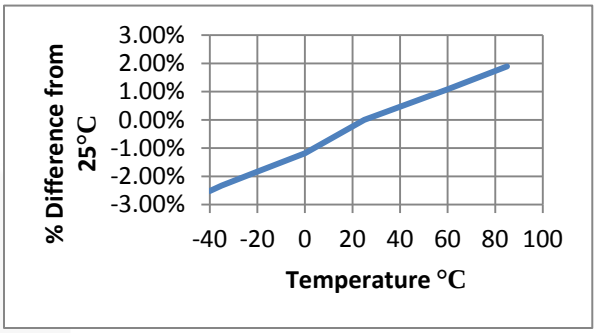


Figure 14. Quiescent Current vs. Temperature

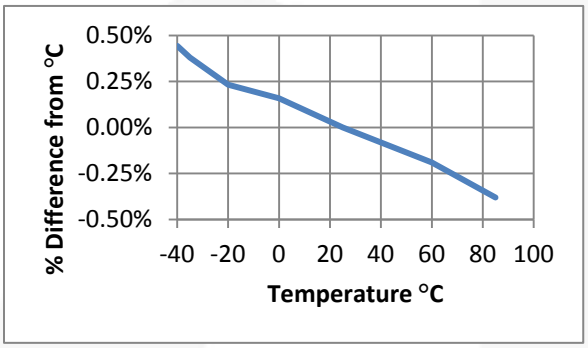


Figure 15. Under-Voltage Lockout Rising vs. Temperature

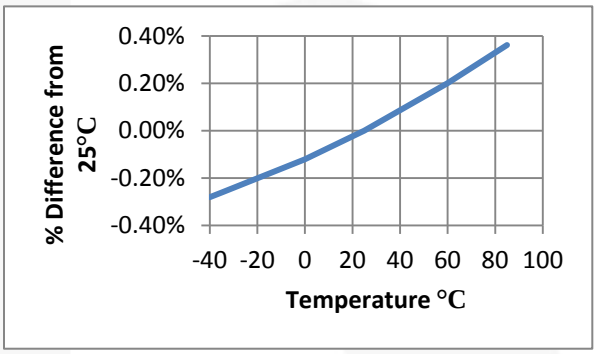


Figure 16. VDD vs. Temperature

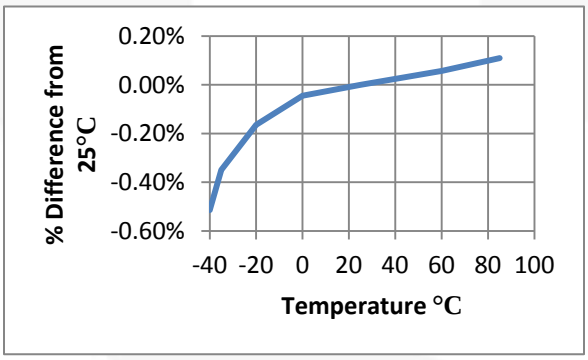


Figure 17. Oscillator Frequency vs. Temperature

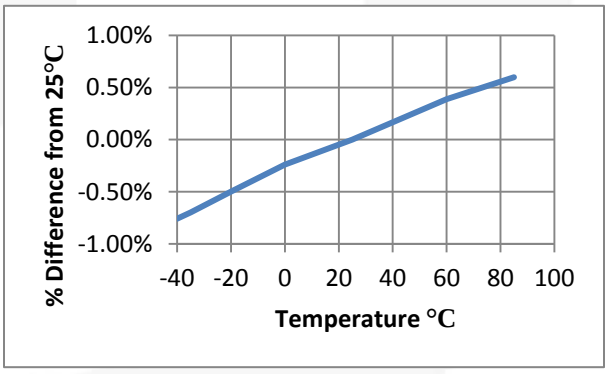
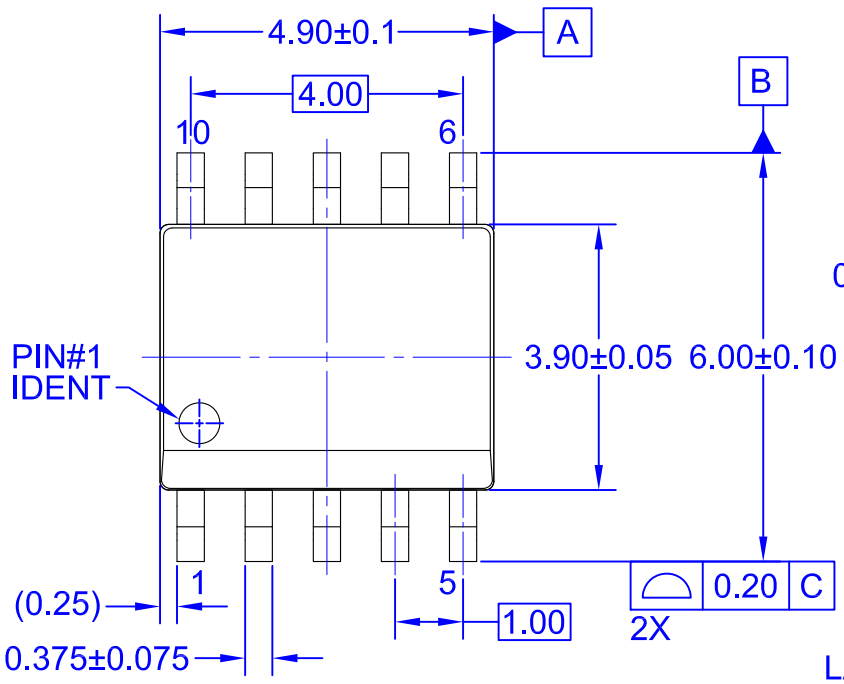
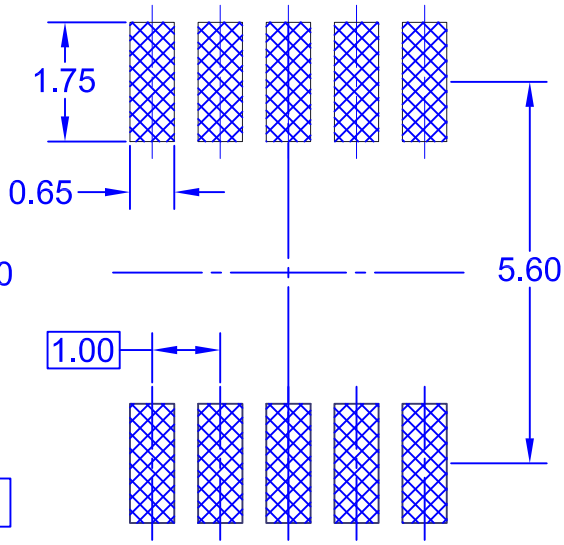


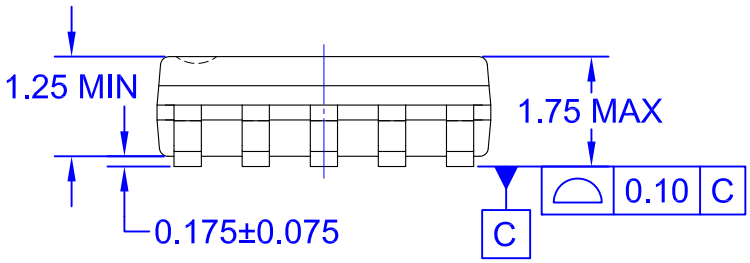
Figure 18. DIM Control Source Current vs. Temperature



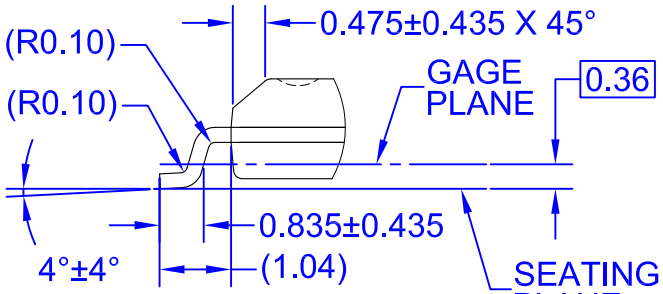
TOP VIEW



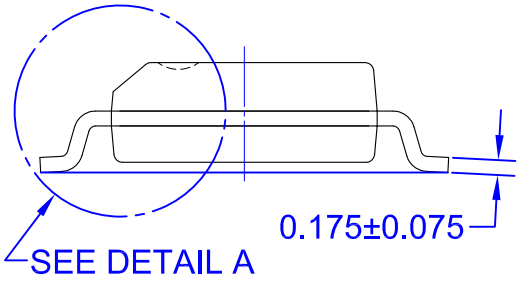
LAND PATTERN RECOMMENDATION



SIDE VIEW



DETAIL A



FRONT VIEW

NOTES:
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