P-Channel POWERTRENCH® MOSFET

-40 V, -100 A, 4.4 m Ω

Features

- Typical $R_{DS(on)} = 3.3 \text{ m}\Omega$ at $V_{GS} = -10 \text{ V}$, $I_D = -80 \text{ A}$
- Typical $G_{g(tot)} = 110 \text{ nC}$ at $V_{GS} = -10 \text{ V}$, $I_D = -80 \text{ A}$
- UIS Capability
- Qualified to AEC Q101
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electrical Power Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems

MAXIMUM RATINGS ($T_A = 25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain-to-Source Voltage	-40	V
V _{GS}	Gate-to-Source Voltage	±16	V
I _D	Drain Current – Continuous, $(V_{GS} = -10 \text{ V}) T_C = 25^{\circ}\text{C} \text{ (Note 1)}$	-100 te 1)	
	Pulsed Drain Current, T _C = 25°C	(See Figure 4)	Α
E _{AS}	Single Pulse Avalanche Energy (Note 2)	259	mJ
P _D	Power Dissipation	227	W
Derate Above 25°C		1.52	W/°C
T _J , T _{STG}	Operating and Storage Temperature	–55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

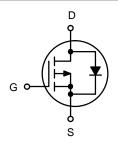
- 1. Current is limited by bondwire configuration.
- 2. Starting $T_J = 25^{\circ}C$, L = 0.1 mH, $I_{AS} = -72$ A, $V_{DD} = -40$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche.



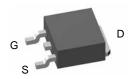
ON Semiconductor®

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V _{DSS}	R _{DS(ON)} MAX I _D MA	
-40 V	4.4 mΩ @ –10 V	–100 A

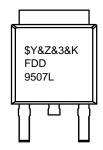


P-CHANNEL MOSFET



DPAK3 (TO-252) CASE 369AS

MARKING DIAGRAM



- \$Y = ON Semiconductor Logo &Z = Assembly Plant Code
- &3 = Numeric Date Code &K = Lot Code
- FDD9507L = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{ heta JC}$	Thermal Resistance, Junction to Case	0.66	°C/W
$R_{ heta JA}$	Thermal Resistance, Junction to Ambient (Note 3)	52	

R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

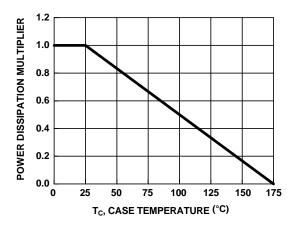
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
OFF CHARA	ACTERISTICS					
BV _{DSS}	Drain-to-Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-40	-	-	V
I _{DSS}	Drain-to-Source Leakage Current	$V_{DS} = -40 \text{ V}, V_{GS} = 0 \text{ V}$ $T_{J} = 25^{\circ}\text{C}$ $T_{J} = 175^{\circ}\text{C (Note 4)}$	<u>-</u>	_ _	1	μA mA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±16 V	-	-	±100	nA
ON CHARA	CTERISTICS					
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	-1	-2	-3	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = -4.5 \text{ V}, I_D = -80 \text{ A}, T_J = 25^{\circ}\text{C}$	_	4.9	7.2	mΩ
		$V_{GS} = -10 \text{ V}, I_D = -80 \text{ A}$ $T_J = 25^{\circ}\text{C}$ $T_J = 175^{\circ}\text{C (Note 4)}$	- -	3.3 5.3	4.4 7.1	
DYNAMIC C	HARACTERISTICS					
C _{iss}	Input Capacitance	V _{DS} = -20 V, V _{GS} = 0 V, f = 1 MHz		6250	-	pF
C _{oss}	Output Capacitance			2640	-	pF
C _{rss}	Reverse Transfer Capacitance			61	-	pF
R _g	Gate Resistance	f = 1 MHz	_	19.3	-	Ω
Q _{g(tot)}	Total Gate Charge	$V_{GS} = 0 \text{ V to } -10 \text{ V}, V_{DD} = -20 \text{ V}, I_D = -80 \text{ A}$	_	100	130	nC
Q _{g(-4.5)}	Total Gate Charge	$V_{GS} = 0 \text{ V to } -4.5 \text{ V}, V_{DD} = -20 \text{ V}, I_D = -80 \text{ A}$	_	46	-	nC
Q _{g(th)}	Threshold Gate Charge	$V_{GS} = 0 \text{ V to } -2 \text{ V}, V_{DD} = -20 \text{ V}, I_D = -80 \text{ A}$	-	13	-	nC
Q _{gs}	Gate to Source Charge	V _{DD} = -20 V, I _D = -80 A	_	22	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	V _{DD} = -20 V, I _D = -80 A	-	13	-	nC
SWITCHING	CHARACTERISTICS					
t _{on}	Turn-On Time	$V_{DD} = -20 \text{ V}, I_{D} = -80 \text{ A}, V_{GS} = -10 \text{ V},$ $R_{GEN} = 6 \Omega$		-	21	ns
t _{d(on)}	Turn-On Delay			10	-	ns
t _r	Rise Time			6	-	ns
t _{d(off)}	Turn-Off Delay			400	-	ns
t _f	Fall Time			132	-	ns
t _{off}	Turn-Off Time			-	710	ns
DRAIN-SOU	RCE DIODE CHARACTERISTICS					
V _{SD}	Source to Drain Diode Forward Voltage	I _{SD} = -80 A, V _{GS} = 0 V	-	-0.9	-1.3	V
		I _{SD} = -40 A, V _{GS} = 0 V	-	-0.85	-1.2	
t _{rr}	Reverse Recovery Time	$I_F = -80 \text{ A}, dI_{SD}/dt = 100 \text{ A}/\mu\text{s}$	-	87	113	ns
Q _{rr}	Reverse Recovery Charge]	_	115	150	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

^{4.} The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS



200 CURRENT LIMITED V_{GS} = -10 V BY SILICON -ID, DRAIN CURRENT (A) 160 120 80 **CURRENT LIMITED** BY PACKAGE 40 0 25 100 125 150 175 T_C, CASE TEMPERATURE(°C)

Figure 1. Normalized Power Dissipation vs. Case Temperature

Figure 2. Maximum Continuous Drain Current vs.

Case Temperature

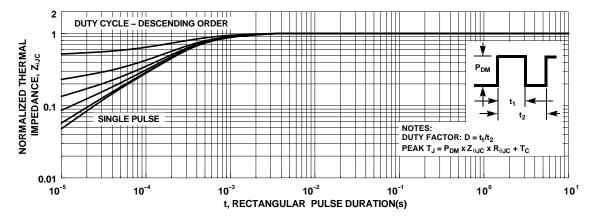


Figure 3. Normalized Maximum Transient Thermal Impedance

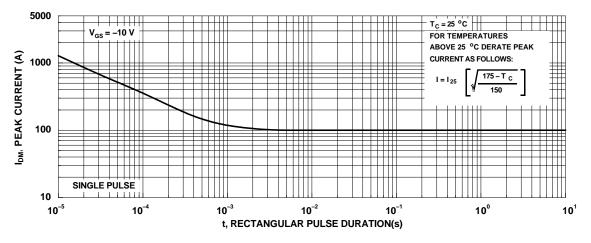


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

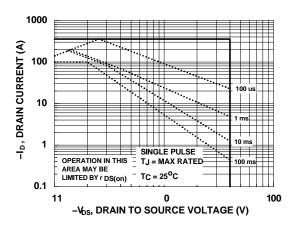


Figure 5. Forward Bias Safe Operating Area

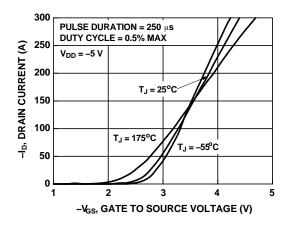


Figure 7. Transfer Characteristics

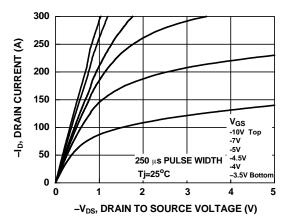


Figure 9. Saturation Characteristics

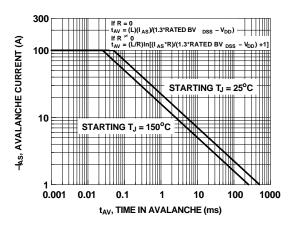


Figure 6. Unclamped Inductive Switching Capability

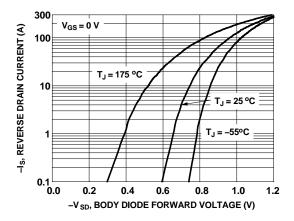


Figure 8. Forward Diode Characteristics

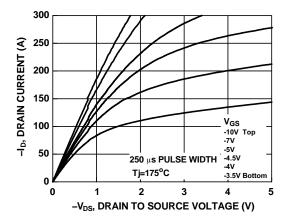


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

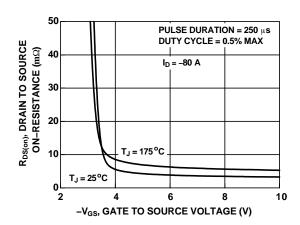


Figure 11. R_{DS(on)} vs. Gate Voltage

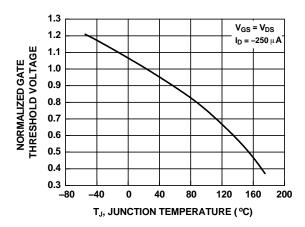


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

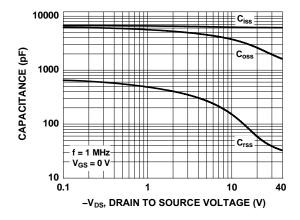


Figure 15. Capacitance vs. Drain to Source Voltage

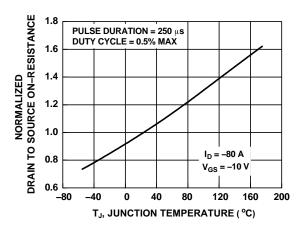


Figure 12. Normalized R_{DS(on)} vs. Junction Temperature

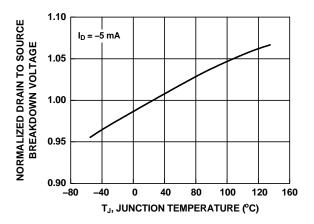


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

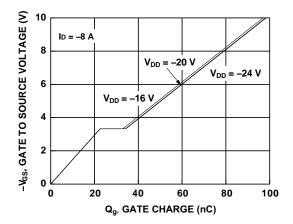


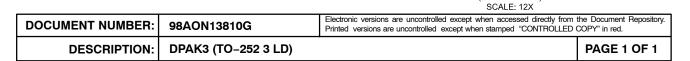
Figure 16. Gate Charge vs. Gate to Source Voltage

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ORDERING INFORMATION

Device	Marking	Package	Reel Size	Tape Width	Quantity
FDD9507L-F085	FDD9507L	DPAK3 (TO-252) (Pb-Free / Halogen Free)	13″	16 mm	2500 Units

DPAK3 (TO-252 3 LD) CASE 369AS **ISSUE O DATE 30 SEP 2016** 6.73 6.35 5,46 5.55 MIN-6.50 MIN 6.40 Ċ 0.25 MAX PLASTIC BODY STUB MIN DIODE PRODUCTS VERSION (0.59)-1.25 MIN 0.89 ⊕ 0.25 M AM C 2.29 2.28 4.56 4.57 LAND PATTERN RECOMMENDATION NON-DIODE PRODUCTS VERSION В 2.39 SEE 2.18 4.32 MIN **NOTE D** 0.58 0.45 5.21 MIN 10.41 9.40 SEE DETAIL A 2 3 NON-DIODE PRODUCTS VERSION DIODE PRODUCTS VERSION ○ 0.10 B 0,51 **GAGE PLANE** NOTES: UNLESS OTHERWISE SPECIFIED 0.61 0.45 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, (1.54)ISSUE C, VARIATION AA. B) ALL DIMENSIONS ARE IN MILLIMETERS. C) DIMENSIONING AND TOLERANCING PER 10° ASME Y14.5M-2009. D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED 1 78 CORNERS OR EDGE PROTRUSION.



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E TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS

G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

F) DIMENSIONS ARE EXCLUSSIVE OF BURSS,

MOLD FLASH AND TIE BAR EXTRUSIONS.

0.127 MAX

DETAIL A (ROTATED -90°)

SEATING PLANE

1,40

(2.90)

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