NCP3902

High-Current Bidirectional Load Switch with Dual Input Support

ON Semiconductor®

www.onsemi.com

WLCSP20
CASE 567PM

Description

The NCP3902 is a high voltage, high current, bidirectional load switch. It provides input overvoltage and surge protection as well as reverse−blocking of output voltage. The logic control of the device is designed to interact with both a system controller and a wireless charging receiver which allows creating a dual input charger application with a single switch.

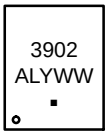
Features

- DC Input Voltage Operating Range from 3.0 V to 20 V
- 28 V DC Absolute Maximum Input Voltage
- Pin−selectable Overvoltage Protection (13 V / 17 V)
- Surge Protection Compliant with IEC61000−4−5 at 100 V
- Input Voltage Sense Output with Selectable Clamp (16 V / 20 V)
- Reverse Blocking Protection from OUT to USBIN
- Switch On−resistance of 23 mΩ Typical
- 3 A DC Nominal and 5 A Maximum Current Capability
- Autonomous Mode and Slave Mode Operation
- 50 ms Input Supply Detect Deglitcher in Autonomous Mode
- 50 ms Break−before−make Timing with Discharge
- Bi−directional Status Indicator and OTG Enable Pin
- Device Enable Input (active low)
- Wireless Enable Output (active low)
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Smart Phone
- Handheld Devices
- Tablets

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 19 of this data sheet.

TYPICAL APPLICATION DIAGRAM

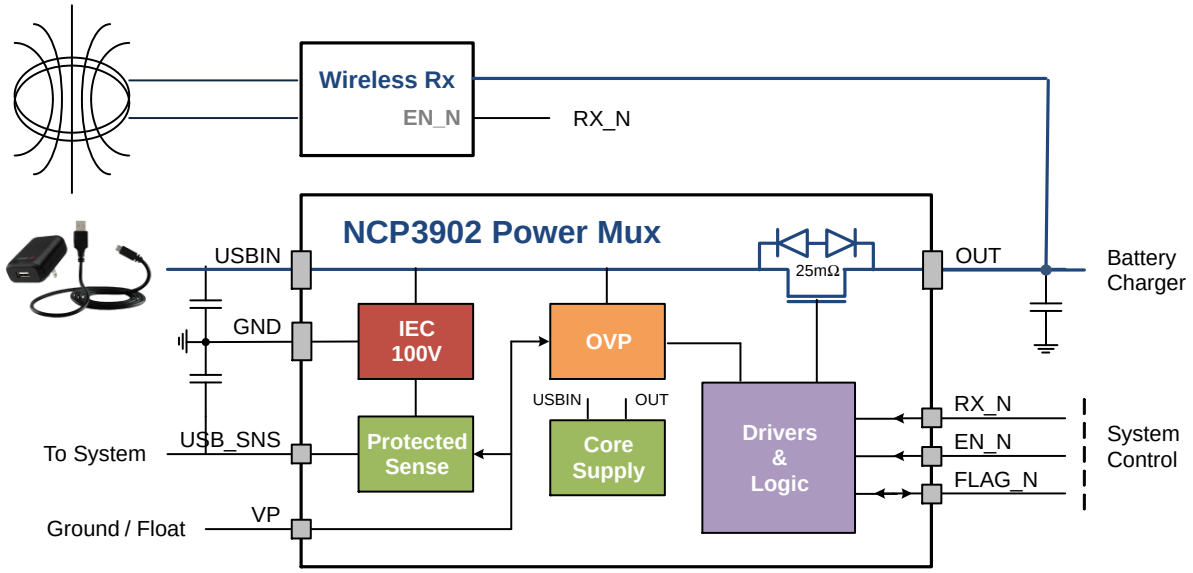


Figure 1. Application Schematic

PIN OUT (TOP VIEW)

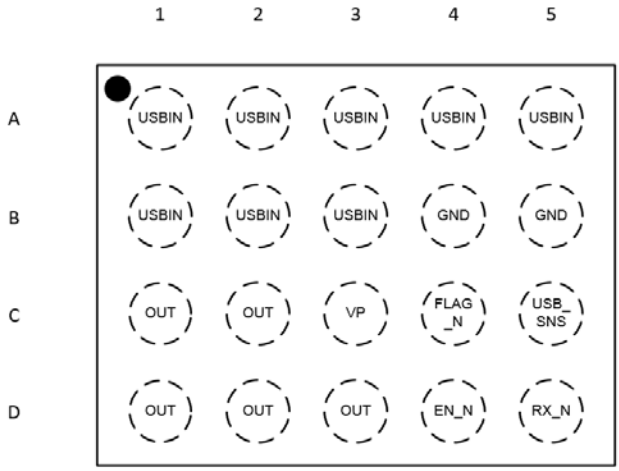


Figure 2. Pin out − Top View

Table 1. PIN FUNCTION DESCRIPTION

Pin out	Name	Type	Function
A1, A2, A3, A4, A5	USBIN	Power	Load switch input
C1, C2	OUT	Power	Load switch output
C5	USB_SNS	Analog Output	Clamped USBIN sense output
C3	VP	Digital Input	Overvoltage protection setting
D4	EN_N	Digital Input	Active Low logic enable
D5	RX_N	Digital Output	Wireless receiver active
C4	FLAG_N	Digital Input	OTG enable input
		Digital Output	Ready for OTG output
B4, B5	GND	Ground	Ground

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
USBIN (Note 1)	USBIN	−0.3 to 28	V
USBIN (Note 2)		100	V
USB_SNS (Note 1)	USB_SNS	−0.3 to 20	V
OUT (Note 1)	V_{OUT}	−0.3 to 20	V
VP,EN_N,RX_N,FLAG_N (Note 1)	V_{CTRL}	−0.3 to 6	V
Storage Temperature Range	T_{STG}	−65 to 150	°C
Maximum Junction Temperature (Note 3)	T_J	−40 to TSD	°C
Moisture Sensitivity (Note 4)	MSL	Level 1	
Human Body Model (HBM) ESD Rating (JEDEC standard: JESD22−A114)	ESD HBM	2500	V
Charged Device Model (CDM) ESD Rating (JEDEC standard: JESD22−A114)	ESD CDM	1000	V
Latch up Current @ 25°C (JEDEC standard: JESD78 class II):	ILU	120	mA
Latch up Current @ 85°C (JEDEC standard: JESD78 class II):		100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. With Respect to GND. According to JEDEC standard JESD22−A108
2. With Respect to GND. According to standard IEC61000−4−5 1.2/50 μs
3. A thermal shutdown protection avoids irreversible damage on the device due to power dissipation
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020

Table 3. OPERATING CONDITION

Symbol	Parameter	Condition	Min	Typ	Max	Unit
USBIN	Operational Power Supply on USBIN		0		28	V
VP, EN_N, RX_N, FLAG_N	Operational Supply		0		5.5	V
I_{OUT}	Operational Output Current		0		3	A
V_{OUT}	Operational Supply on OUT	OTG mode, USBIN = 0 V	0		5.5	V
C_{IN}				1		μF
C_{INSNS}				1		μF
C_{OUT}			0.1			μF
$R_{\theta JA}$		(Notes 3 and 5)		45		°C/W
T_J			−40	25	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. The $R_{\theta JA}$ is dependent on the PCB heat dissipation. Board used to drive this data was a 2s2p JEDEC PCB standard.

Table 4. ELECTRICAL CHARACTERISTICS
Unless otherwise noted, min & max limits apply for a T_A between −40°C and +85°C, T_J up to +125°C. Typical values are referenced to T_J = +25°C. Supply conditions USBIN = 5 V, OUT = 5 V. Capacitor values (DC Bias 0 V) C_{USBIN} = 1 μF, C_{OUT} = 1 μF, C_{USB_SNS} = 1 μF,

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{UVLO_USB}	Under Voltage Lockout at USBIN	Rising	2.55	2.8	3.0	V
		Falling	2.45	2.6	2.8	V
V_{UVLO_OUT}	Under Voltage Lockout at OUT	Rising	2.55	2.8	3.0	V
		Falling	2.45	2.6	2.8	V
V_{CORE}	Core Voltage	On−chip core voltage	2.45	3.4	4.5	V
V_{OVP}	Over Voltage Lockout at USBIN	Rising, VP to ground (Note 6)	16	17	18	V
		Rising, VP left floating (Note 6)	12	13	14	V
V_{OVP_hyst}	Over Voltage Lockout hysteresis		−	300	−	mV
R_{DSON}	Switch On Resistance	From USBIN to OUT, TA = 25 ⍰C	−	23	35	mΩ
R_{USB}	Termination Resistance at USBIN	Always connected	120	200	260	kΩ
R_{DIS_USB}	Discharge Resistance at USBIN	During discharge states	−	500	−	Ω
V_{LK_USBIN}	Switch input to output leakage	Switch not conducting, USBIN = 28V, OUT not loaded	−	−	0.4	V
R_{OUT}	Termination Resistance at OUT	Always connected	120	200	260	kΩ
V_{LK_OUT}	Switch output to input leakage	Switch not conducting, OUT = 16V, USBIN not loaded	−	−	0.4	V
R_{DIS_OUT}	Discharge Resistance at OUT	During discharge states	−	500	−	Ω
$V_{SNSCLMP}$	Voltage Clamp at USB_SNS	Rising, VP to ground (Note 6)	16	−	20	V
		Rising, VP left floating (Note 6)	12	−	16	V
dV_{SNS}	Voltage Drop at USB_SNS	Referenced to USBIN, Load 20 mA	−	20	37	mV
I_{Q_USBIN}	Input quiescent current	Switch not conducting, USBIN = 5 V	−	110	200	μA
I_{DD_USBIN}	Input operating current	Switch conducting, USBIN = 5 V	−	140	250	μA
I_{Q_OUT}	Output quiescent current	Switch not conducting, OUT = 5 V	−	110	200	μA
I_{DD_OUT}	Output operating current	Switch conducting, OUT = 5 V	−	140	250	μA
V_{IH}	Input logic high level	EN_N, FLAG_N, VP	1.4	−	5.5	V
V_{IL}	Input logic low level	EN_N, FLAG_N, VP	0	−	0.4	V
I_{LK_EN}	Input leakage current EN_N	EN_N = 5 V, VUSBIN = 0 V, VOUT = 0 V	−	−	1	μA
		EN_N = 5 V, VUSBIN = 5 V, VOUT = 0 V	−	−	1	μA
V_{OL}	Output logic low level	FLAG_N, RX_N, Sink 2 mA	−	−	0.2	V
R_{FL}	Logic high pull−up FLAG_N	FLAG_N to VCORE	400	500	600	kΩ
R_{RX}	Logic high pull−up RX_N	RX_N to VCORE	400	500	600	kΩ
R_{VP}	Logic high pull−up VP	VP to VCORE	400	500	600	kΩ
T_{IHEN}	Input logic high debounce	EN_N (Note 8)	−	40	−	us
T_{ILEN}	Input logic low debounce	EN_N (Note 8)	−	40	−	us
T_{IHFL}	Input logic high debounce	FLAG_N (Note 8)	−	40	−	us
T_{ILFL}	Input logic low debounce	FLAG_N (Note 8)	−	40	−	us
T_{DEBUSB}	Supply debounce period	Debounce of USBIN (Note 8)	−	50	−	ms
T_{DEBOUT}	Supply debounce period	Debounce of OUT (Note 8)	−	40	−	us
T_{DIS}	Supply discharge period	Discharge of USBIN and OUT	−	50	−	ms
dT	Timing accuracy	(Note 7)	−20	−	+20	%
T_{INIT}	Power up and initialization period	Upon USBIN or OUT crossing UVLO	−	150	−	us

Table 4. ELECTRICAL CHARACTERISTICS
Unless otherwise noted, min & max limits apply for a T_A between −40°C and +85°C, T_J up to +125°C. Typical values are referenced to T_J = +25°C. Supply conditions USBIN = 5 V, OUT = 5 V. Capacitor values (DC Bias 0 V) C_{USBIN} = 1 μF, C_{OUT} = 1 μF, C_{USB_SNS} = 1 μF,

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{SNS}	Startup time USB_SNS	USBIN = 5 V, USB_SNS from 0 V to 4.5 V, not loaded	−	−	500	us
T_{SSTART}	Switch soft−start timing	USBIN = 5 V, OUT from 10 % to 90 % of USBIN	−	0.35	1	ms
		OUT = 5 V, USBIN from 10 % to 90 % of OUT	−	0.35	1	ms
T_{UVLO}	Input falling disable delay	Delay from UVLO falling edge to disabling the load switch	−	10	20	μs
T_{OVP}	Input rising disable delay	Delay from OVLO rising edge to disabling the load switch	−	100	−	ns
T_{SD}	Thermal Shutdown	Rising	−	150	−	°C
		Falling	−	115	−	

6. Includes DC operation as well as USBIN from 0 V to 28 V in 3 V/μs, USBIN from 5 V to 28 V in 1.5 V/μs and 100 V surge holdoff (IEC 61000−4−5) 1.2/50μs and 5/20μs
7. Timing accuracy valid for T_{IHEN}, T_{ILEN}, T_{IHFL}, T_{ILFL}, T_{DEBUSB}, T_{DEBOUT}, T_{DIS} through internal clock measurement
8. Functionality covered by scan tests

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

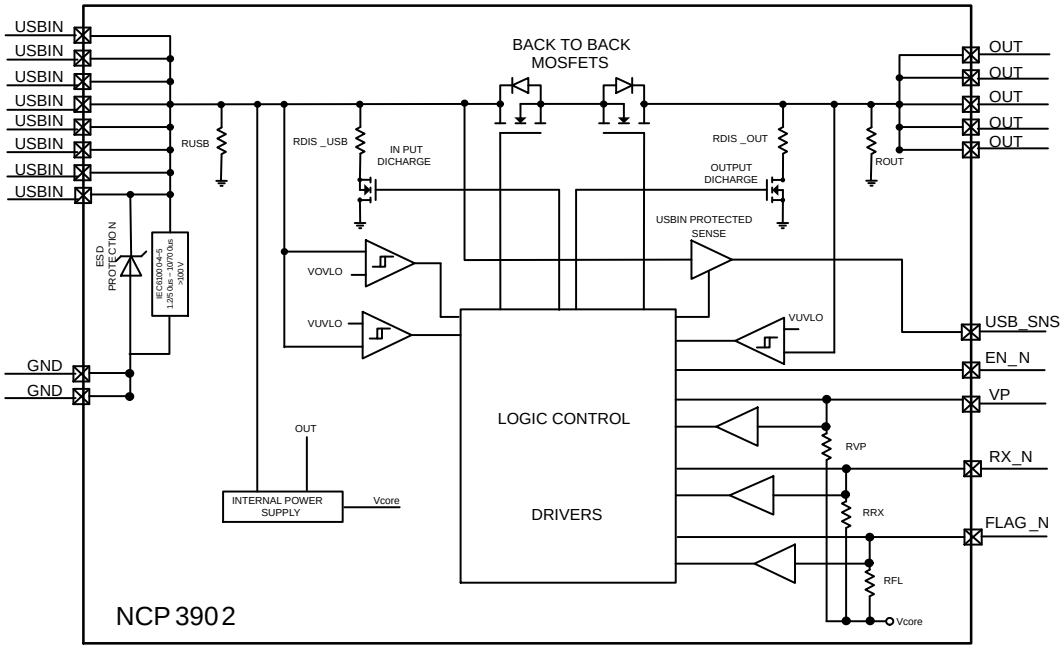


Figure 3. Block Diagram

PRODUCT OVERVIEW

Main Functionality

Traditionally mobile phones and other portable equipment can get charged form a single power source such as USB. With the growing popularity of wireless charging, consumers like to be able to charge from both USB and a wireless source. Most mobile phone chipsets are not capable to natively charge from these two sources. In order to accommodate those chipsets, an input selector switch or multiplexer can be added such as the NCP3901. However, in combination with some wireless charger receivers a single switch could suffice. This is the case if the wireless receiver can be disabled and if it provides reverse blocking of the voltage coming from USB. The NCP3902 perfectly fits to this application. Compared to the NCP3901 the NCP3902 provides a lower switch resistance thus capable of handling higher currents. Both the NCP3901 and the NCP3902 provide overvoltage protection and surge protection on the USB input.

Voltage Protection

The voltage protection includes surge protection, overvoltage protection, and a voltage protected sense output.

The surge protection at USBIN protects the application against surges that may occur on the USB input. The protection level is in compliance with the IEC 61000−4−5 1.2/50 μs and 5/20 μs surge waveforms up to 100 V. The ground balls GND should be solidly routed to the ground plane to guarantee robustness.

To protect the system against too high DC or transient voltages, the switch of the NCP3902 is opened when an overvoltage is detected. The switch is opened a−synchronously to and has no direct influence on the state machine. The overvoltage detection level is selectable by means of the VP pin. With VP to ground, the highest overvoltage protection level is selected. With VP left floating the lowest setting is selected.

The voltage at the USB port is to be sensed by the system. However, for the very same reasons as listed above, the voltage at the sense pin of the system will have to be limited. For this purpose, USB_SNS provides a voltage protected version of USBIN. USB_SNS pin accurately tracks the voltage at USBIN but is clamped to a maximum level that is selected with the VP pin.

Operating Modes

System wise the NCP3902 can operate autonomously or be used as a slave.

In autonomous mode the switch is opened and closed based on the presence of USBIN. For autonomous mode the EN_N pin should be connected to ground or forced low by other means. The RX_N pin is connected to the wireless receiver and FLAG_N connected to the system.

A break before make mechanism will ensure proper initialization of the system. If no USBIN is present, the RX_N pin will be low and the wireless receiver enabled. Upon USBIN detection the wireless receiver is disabled by making RX_N high by pulling this pin up to the core voltage through an on−chip resistor. After having actively discharged OUT, the switch will be closed. When the voltage at USBIN is removed the device will power down and the wireless receiver will automatically be re−enabled.

For OTG operation the bi−directional FLAG_N pin is used. Under normal situations, the FLAG_N pin is actively pulled low by the device. When the system applies a valid voltage to OUT the device will verify if no USB voltage is present. In absence of a valid USB voltage, FLAG_N will be released and pulled up through an on−chip resistor to the core voltage. The system can now close the switch by forcing FLAG_N low which will provide the voltage at OUT to USBIN. The USB peripheral connected will get supplied while at the same time the device makes the RX_N pin high, disabling the wireless receiver. The system can re−open the switch by releasing the FLAG_N which will also make the RX_N pin low again.

In slave mode the switch is opened and closed by controlling the EN_N pin. The RX_N and FLAG_N pins are not connected to the system and can be connected to ground or be left floating. The state of both RX_N and FLAG_N will follow the same scheme as applied for the autonomous mode. For slave mode to be detected the EN_N pin should be high at the instant USBIN or OUT is applied or should be made high shortly after, see also the flow diagram below.

The wireless receiver can provide a regulated 5V to OUT, not only for supplying the system but also to support OTG operation. This is referred to as concurrent OTG mode and force the RX_N to low.

Flow Diagram

Below flow diagram reflects the operation of the state machine of the NCP3902. In combination with the label definitions as listed in the table afterwards, it provides more details on the above described behavior.

The state machine can only operate if the core of the NCP3902 is sufficiently supplied from either USBIN or OUT. In both cases, the voltage will have to be above the undervoltage threshold. In case the core is not or no longer supplied, the state machine is in the OFF state. This may typically occur upon removal of a supplied USB cable.

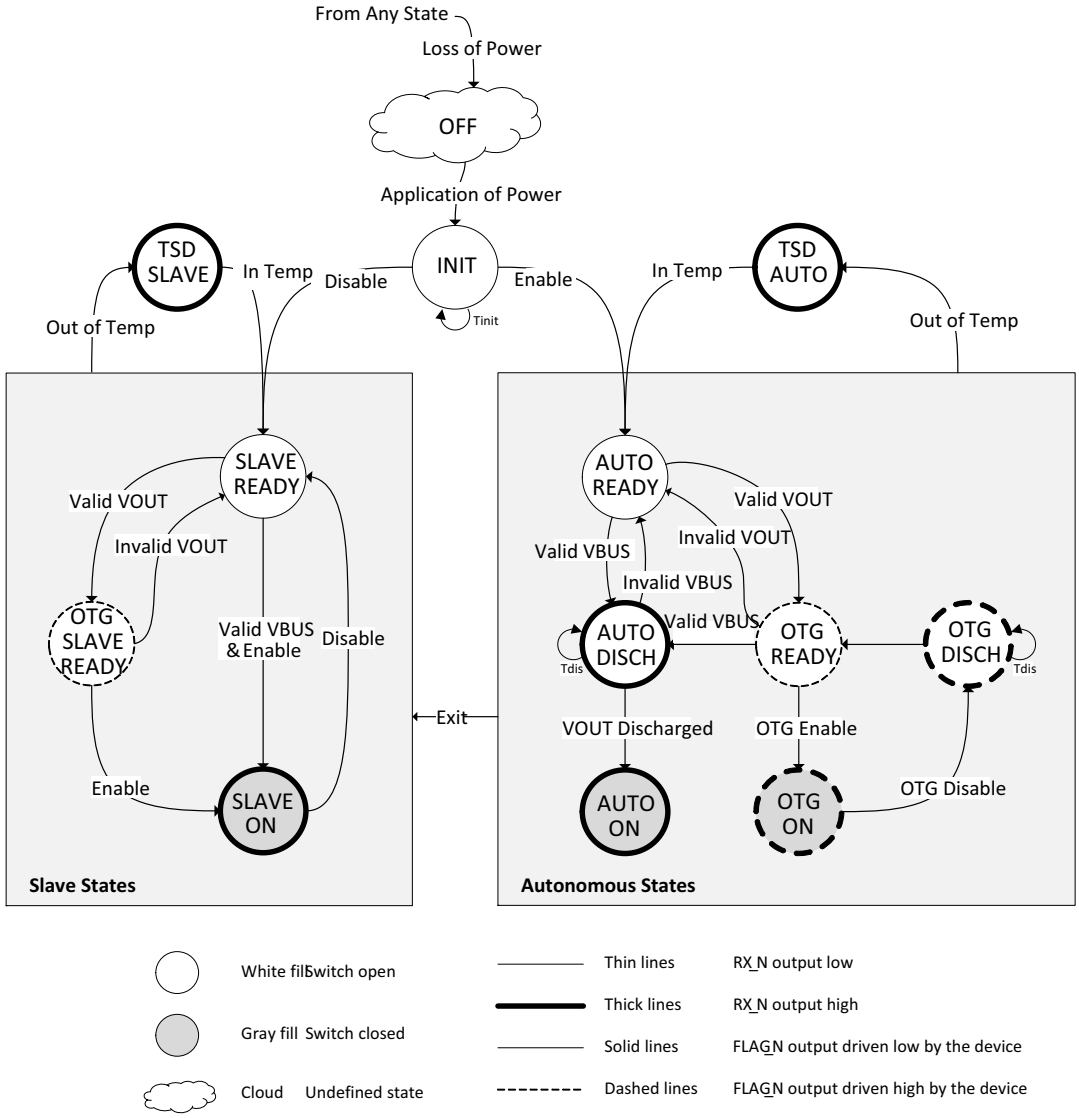


Figure 4. Flow Diagram

Table 5. ACRONYMS AND DEFINITIONS

Label	Description
Loss of Power	Both USBIN and OUT below the UVLO threshold
Application of Power	USBIN and/or OUT above the UVLO threshold
Enable	EN_N pin is low, debounced for Tilen
Disable	EN_N pin is high, debounced for Tihen
Valid VBUS	USBIN above the UVLO threshold debounced for Tdebusb, the voltage at OUT is a don't care
Invalid VBUS	Inverted signal of 'Valid VBUS'
Valid VOUT	OUT above the UVLO threshold debounced for Tdebout and no 'Valid VBUS'
Invalid VOUT	Inverted signal of 'Valid VOUT'
VOUT Discharged	OUT below the UVLO threshold, no debounce
OTG Enable	FLAG_N pin is forced low by the system while FLAG_N was pulled high by the device, debounced for Tilfl
OTG Disable	FLAG_N pin is released by the system and FLAG_N is pulled up by the device, debounced for Tihfl
Out of Temp	Die temperature exceeds thermal shutdown threshold
In Temp	Die temperature falls below thermal shutdown threshold
Tinit	Power up and initialization duration
Tdis	Discharge duration
OFF	Device is not powered
INIT	EN_N don't care, Switch open, RX_N and FLAG_N low. Startup of the device including analog and digital blocks and reading of OTP fuses. Duration Tinit.
TSD SLAVE	EN_N don't care, Switch open, RX_N high, FLAG_N low Entered from any slave state at Out of Temp condition
TSD AUTO	EN_N low, Switch open, RX_N high, FLAG_N low Entered from any autonomous state at Out of Temp condition
AUTO READY	EN_N low, Switch open, RX_N and FLAG_N low. Autonomous mode is detected during INIT state. Can also be entered from AUTO DISCH (if invalid VBUS).
AUTO DISCH	EN_N low, Switch open, RX_N high, FLAG_N low. A 'Valid VBUS' is detected, discharge load activated on OUT and USBIN, minimum duration Tdis. The 'VOUT Discharged' condition must be met before exiting for AUTO ON (verification done for safety reasons)
AUTO ON	EN_N low, Switch closed, RX_N high, FLAG_N low. Under normal conditions this state is only exited upon loss of power (eg. USB removal).
OTG READY	EN_N low, Switch open, RX_N low, FLAG_N high. A 'Valid VOUT' is detected.
OTG ON	EN_N low, Switch closed, RX_N high, FLAG_N forced low by the system. An 'OTG enable' condition is detected
OTG DISCH	EN_N low, Switch open, RX_N high, FLAG_N high (no longer forced low by the system). Discharge load activated on OUT and USBIN, duration Tdis, exited for OTG READY
SLAVE READY	EN_N high, Switch open, RX_N and FLAG_N low. Slave mode is detected during INIT state. Can also be entered from certain autonomous states if EN_N was initially low upon exiting the INIT state.
OTG SLAVE READY	EN_N high, Switch open, RX_N low, FLAG_N high. A 'Valid VOUT' is detected.
SLAVE ON	EN_N low, Switch closed, RX_N high, FLAG_N low.
Exit	While in one of the autonomous states, EN_N is made high leading to an Exit to a slave state. The mapping of the states is as follows: AUTO READY, AUTO DISCH → SLAVE READY AUTO ON, OTG ON, OTG DISCH → SLAVE READY OTG READY → OTG SLAVE READY

9. Overvoltage detection does not have a direct influence on the state machine, it will only open the switch

TIMING DIAGRAMS

The below timing diagrams reflect the behavior of the state machine described above. They are intended for illustration purposes only. Note: timing are not on scale.

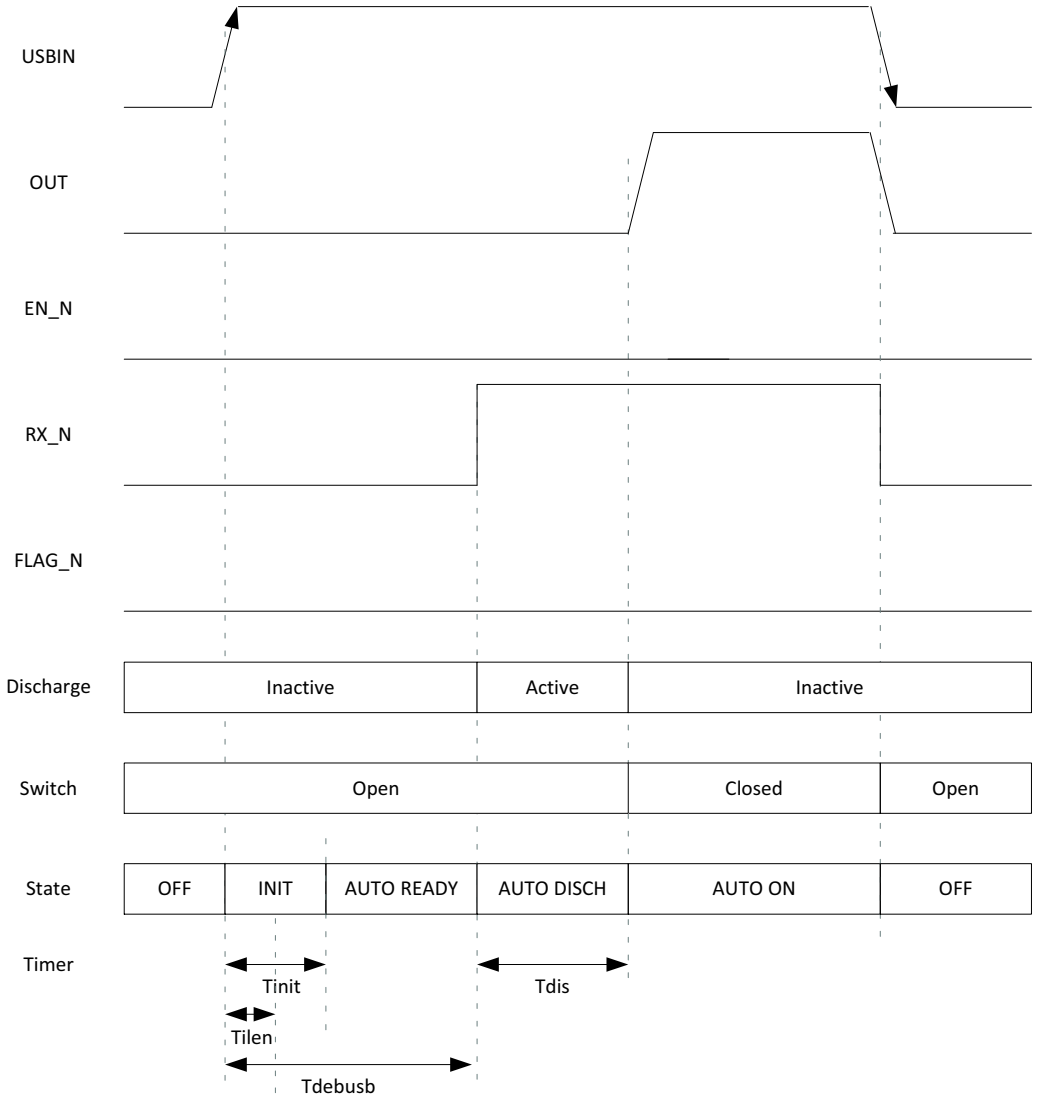


Figure 5. Autonomous Configuration. Application of VBUS with System Turned Off, Removal of VBUS

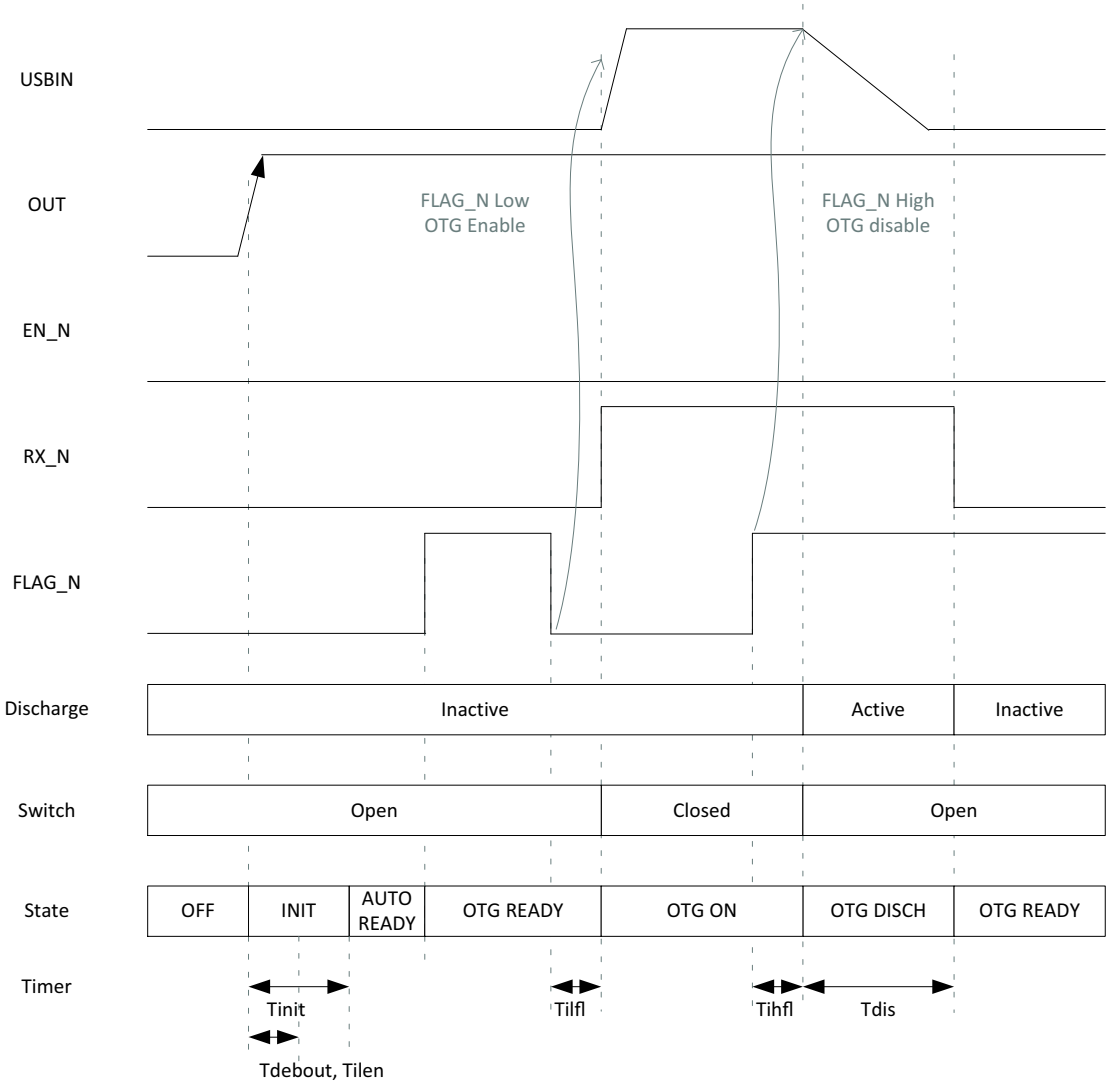


Figure 6. Autonomous Configuration. Application of VOUT, Enabling (OTG), Disabling

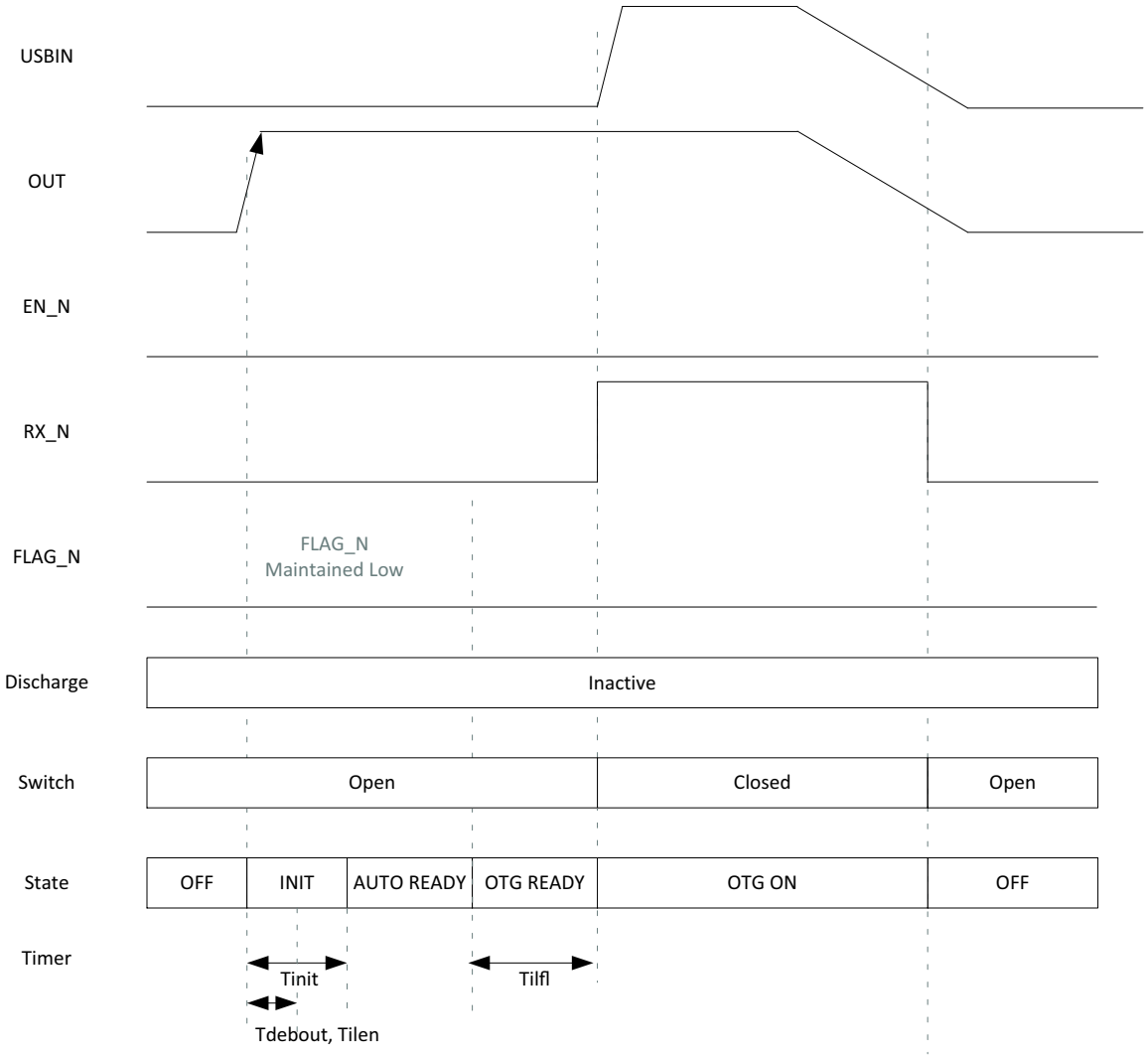


Figure 7. Autonomous Configuration. Application of VOUT

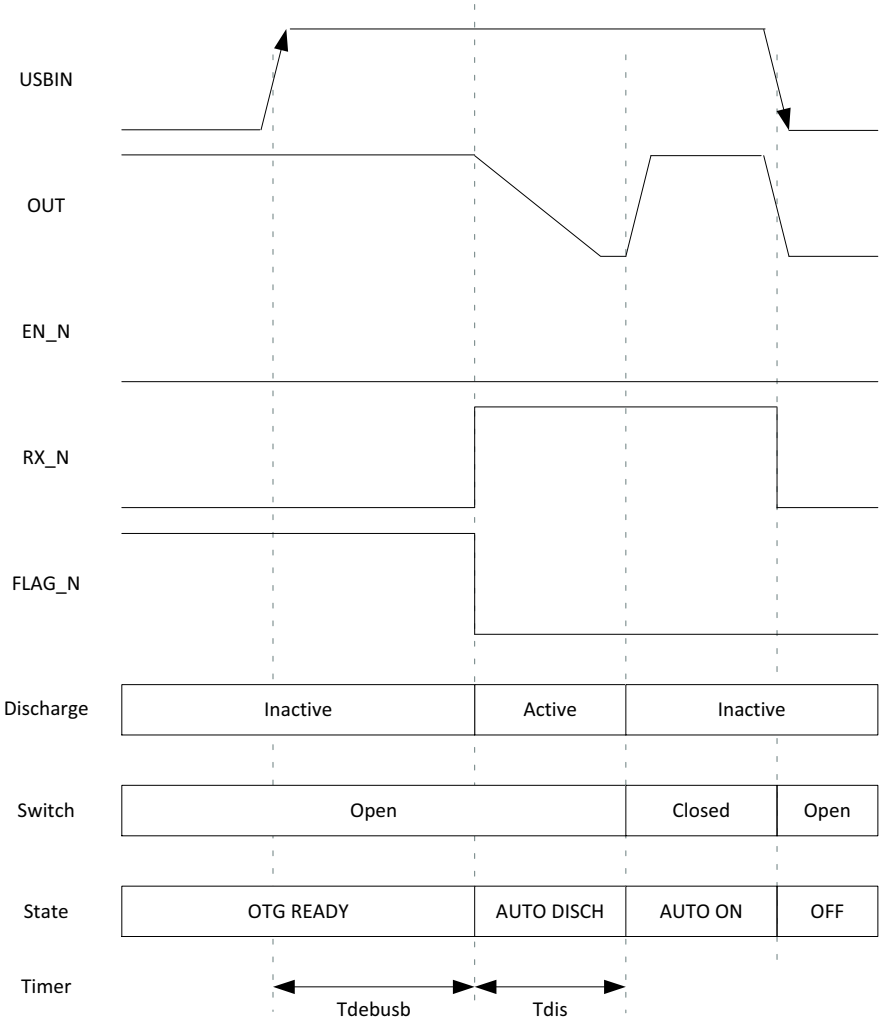


Figure 8. Autonomous Configuration. Application of VBUS with VOUT Present, Removal of VBUS

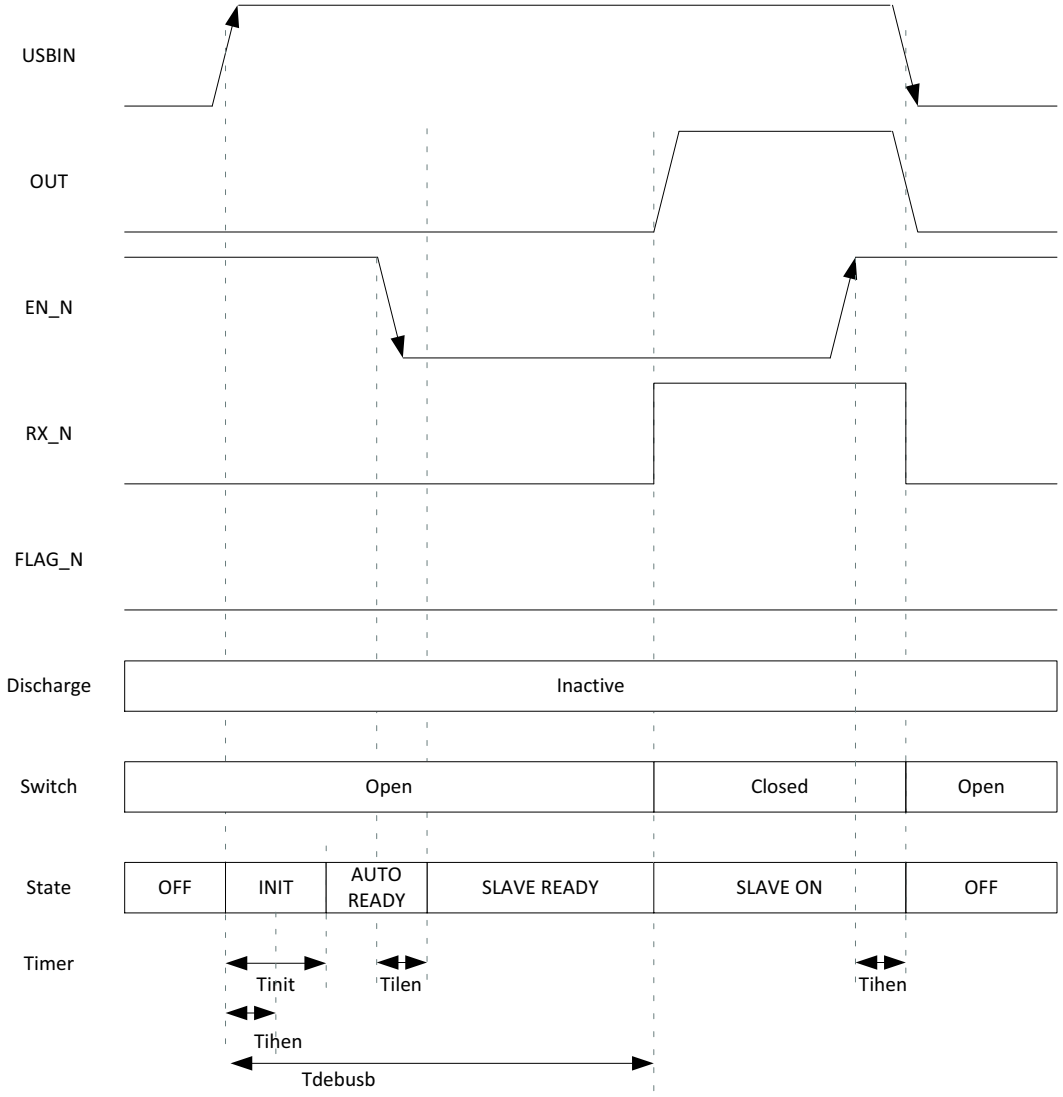


Figure 9. Slave Configuration. Application of VBUS with System Turned Off, Enabling, Disabling

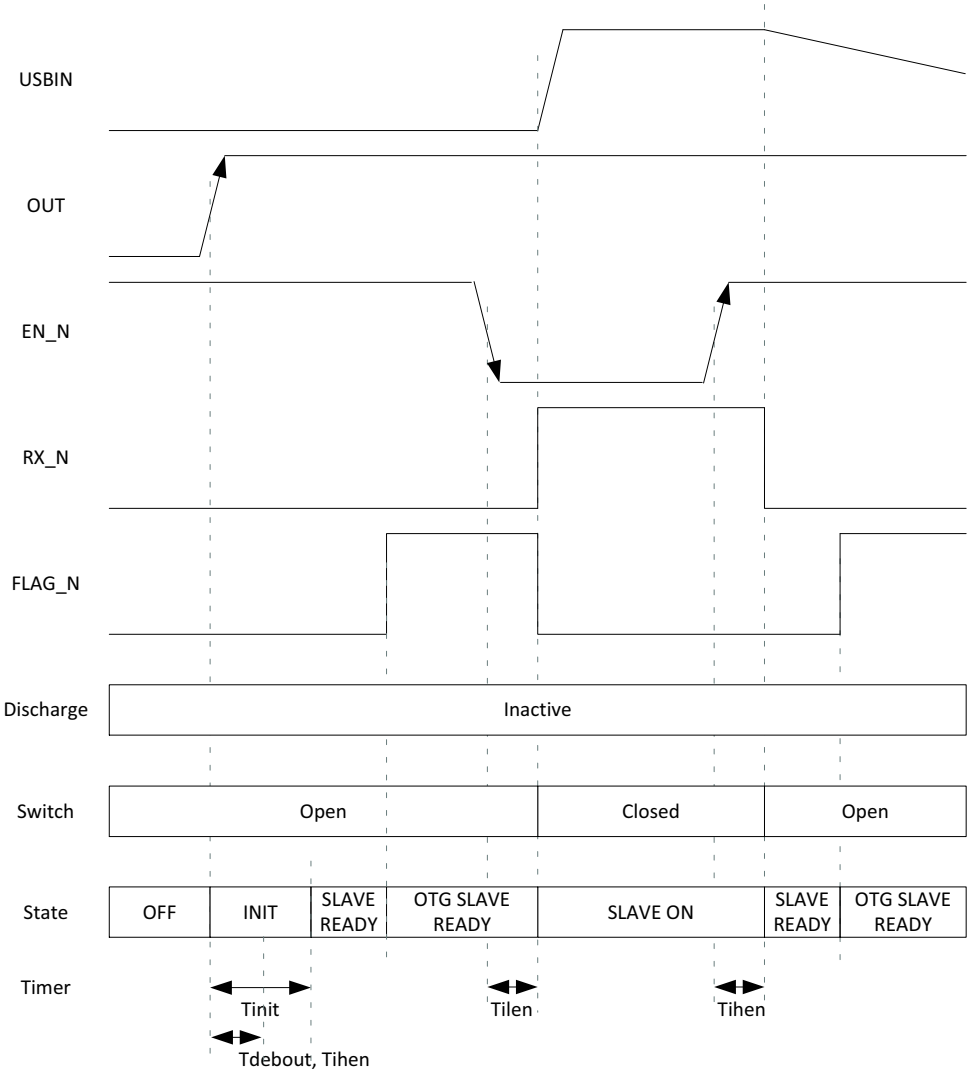


Figure 10. Slave Configuration. Application of VOUT, Enabling (OTG), Disabling

TYPICAL CHARACTERISTICS

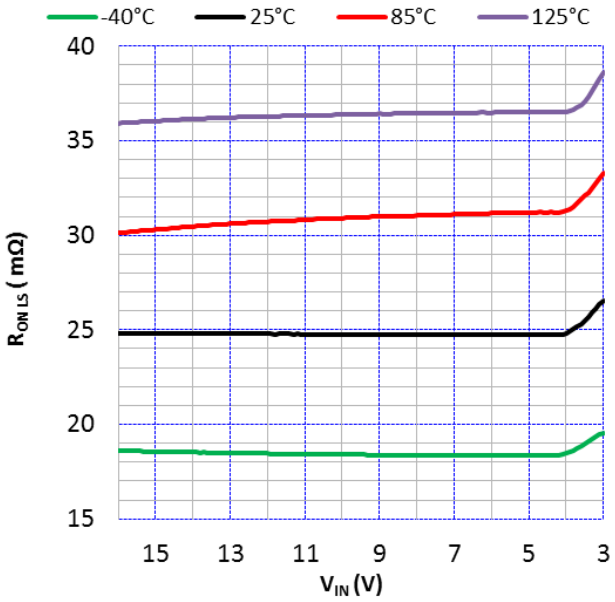


Figure 11. USBIN to OUT MOSFET RESISTANCE vs. VIN and Temperature, No Load

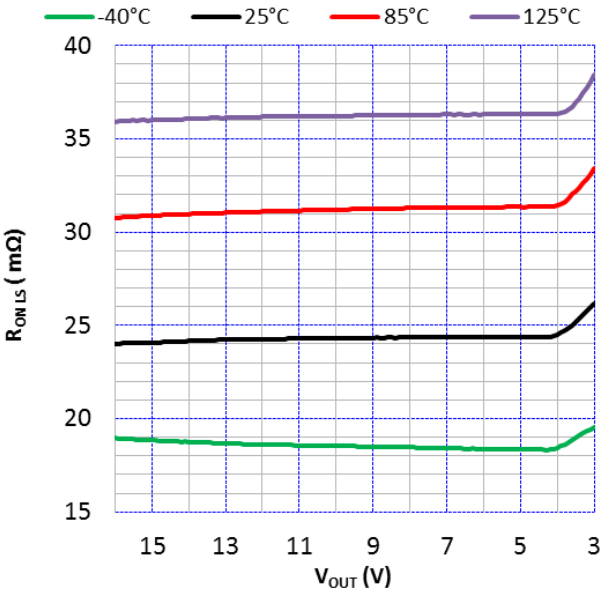


Figure 12. OUT to USBIN Mosfet Resistance vs. VOUT and Temperature No Load

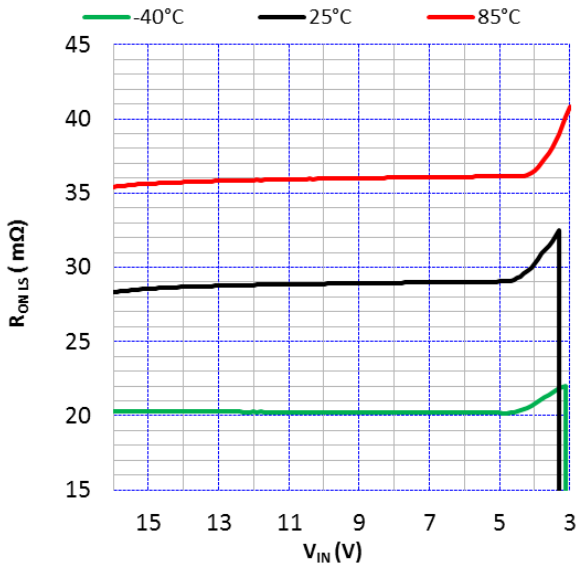


Figure 13. USBIN to Out Mosfet Resistance vs. VIN and Temperature 5 A Load

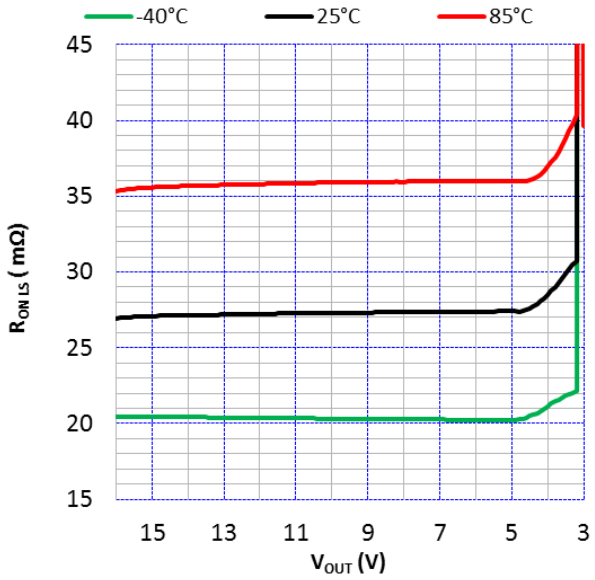


Figure 14. OUT to USBIN Mosfet Resistance vs. Vout and Temperature No Load

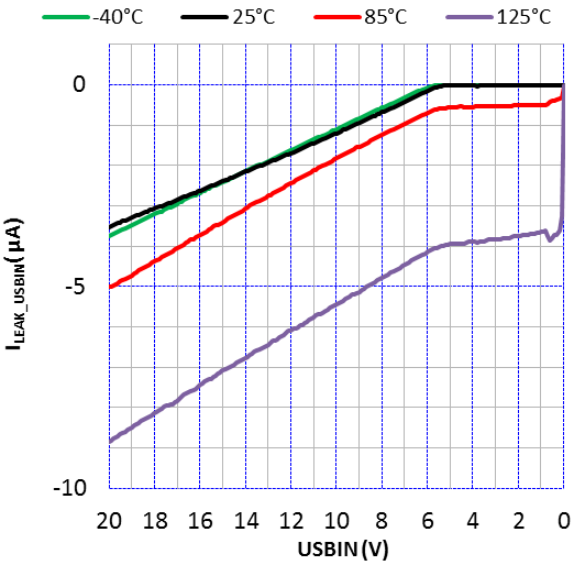


Figure 15. USBIN to Out Mosfet Leakages, vs. USBIN and Temperature

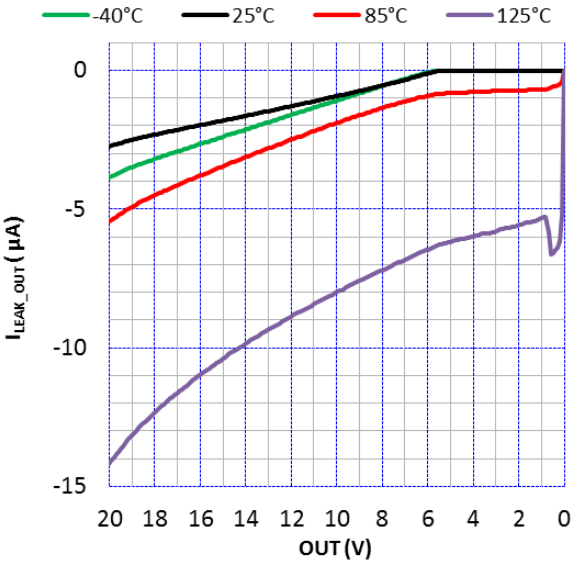


Figure 16. OUT to USBIN Mosfet Leakages, vs. OUT and Temperature

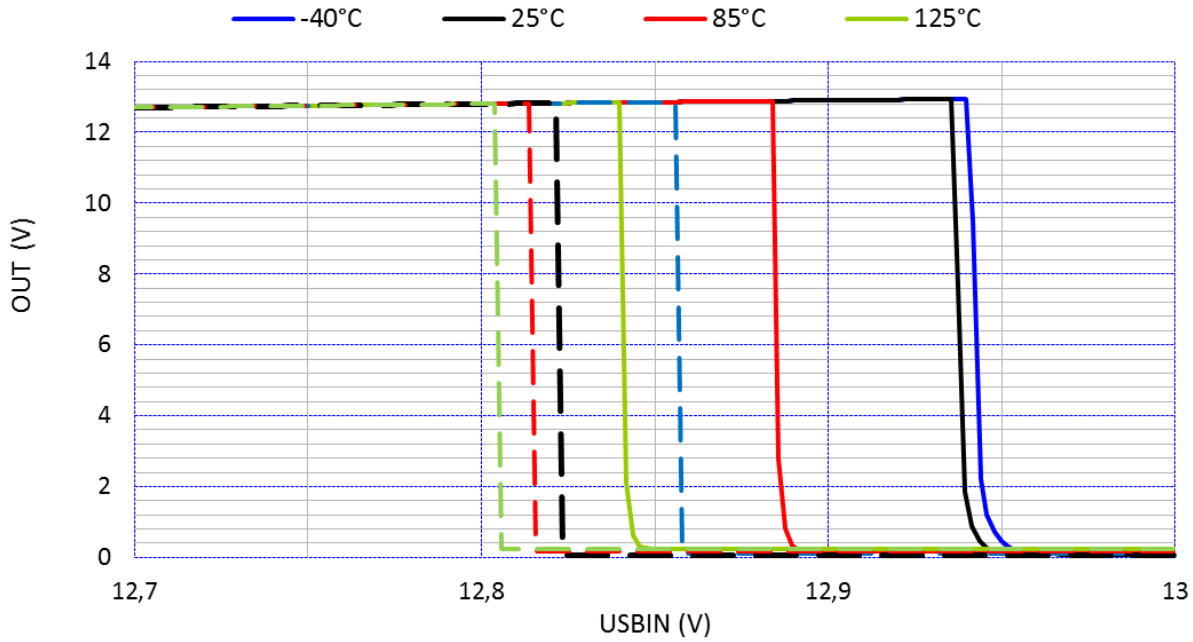


Figure 17. OVLO Threshold and Hysteresis vs. Temperature, VP High

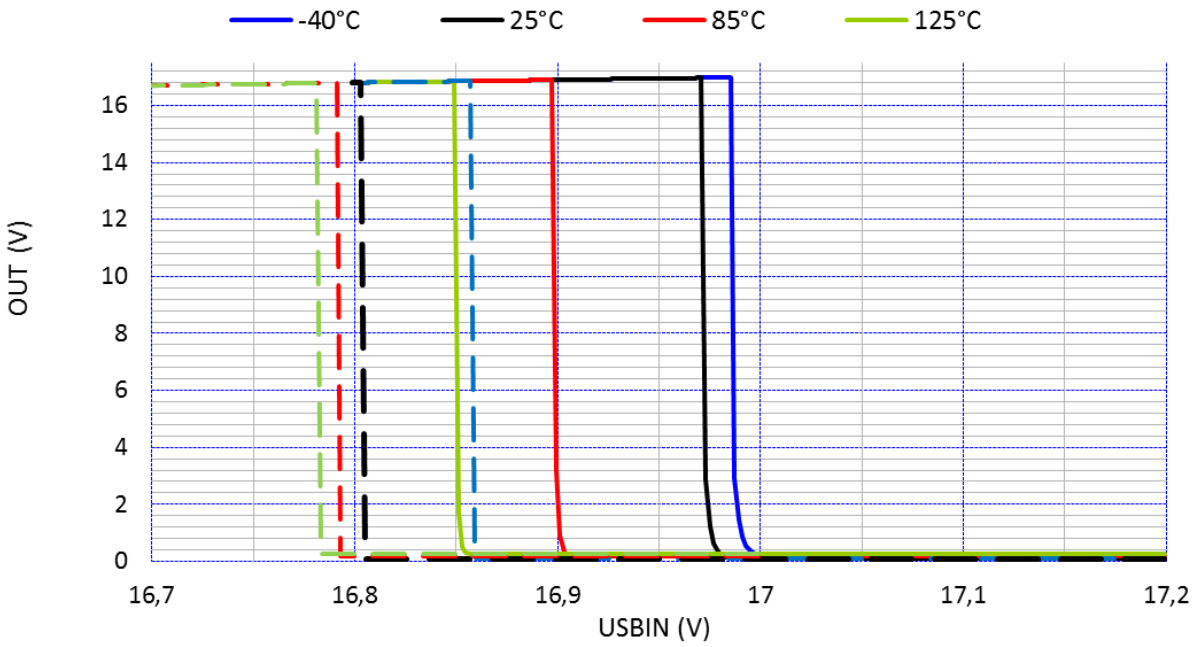


Figure 18. OVLO Threshold and Hysteresis vs. Temperature, VP Low

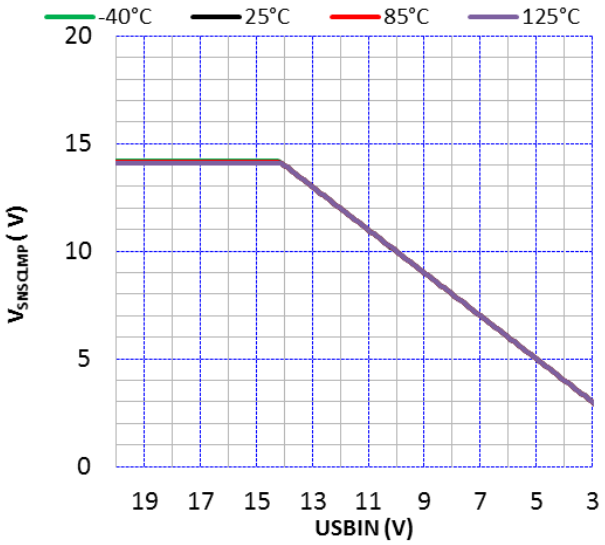


Figure 19. USBSNS Voltage vs. USBIN and Temperature, VP High

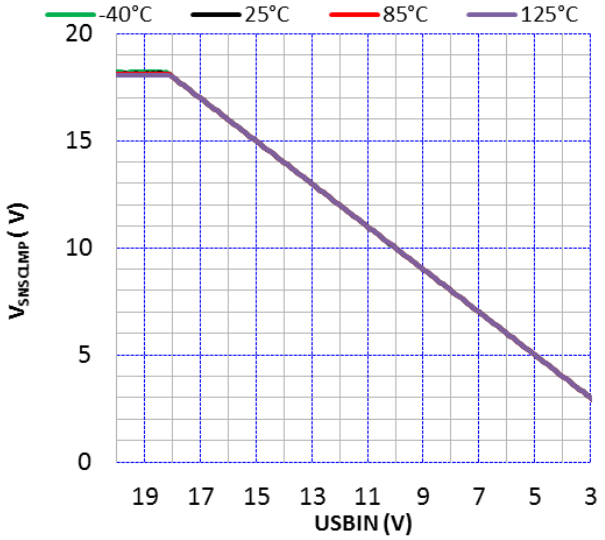


Figure 20. USBSNS Voltage vs. USBIN and Temperature, VP Low

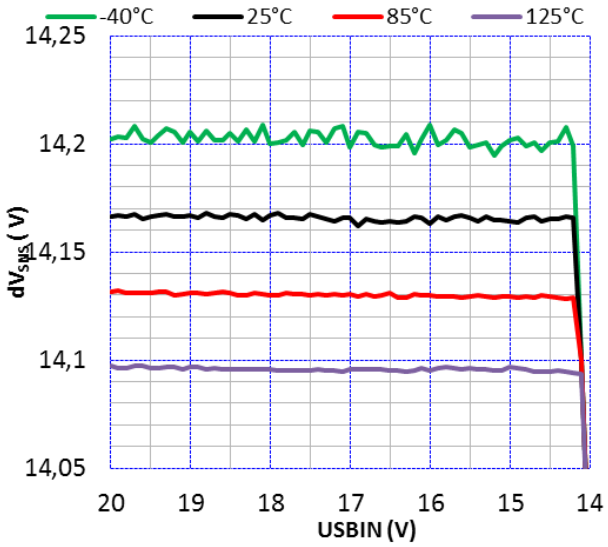


Figure 21. USBSNS Regulation vs. Temperature, VP High

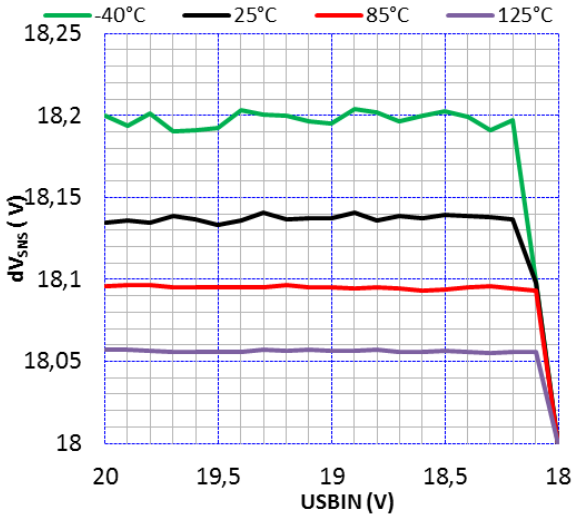


Figure 22. USBSNS Regulation vs. Temperature, VP Low

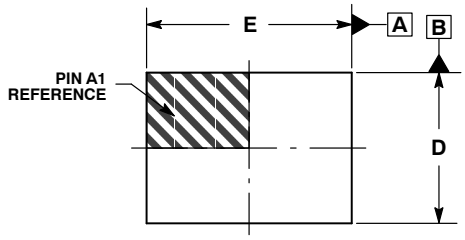
ORDERING INFORMATION

Device	Marking	Package	Shipping
NCP3902FCCTBG	3902	WLCSP20 1.66 x 2.26 mm	3000 Tape/Reel

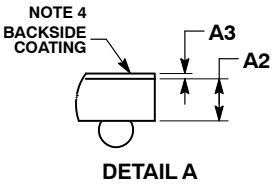
WLCSP20, 1.66x2.26x0.6
CASE 567PM
ISSUE O

DATE 09 AUG 2016

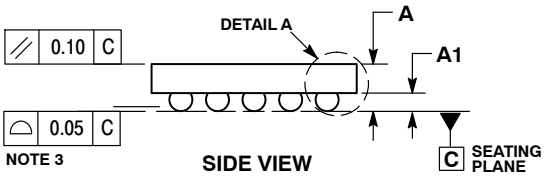
SCALE 4:1



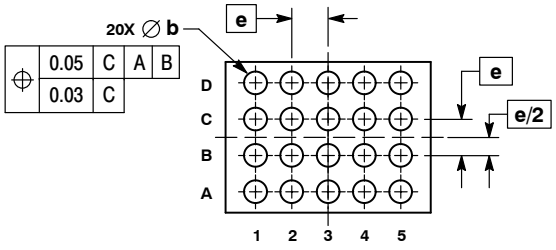
TOP VIEW



DETAIL A



SIDE VIEW

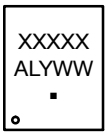


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.
4. BACKSIDE COATING IS OPTIONAL.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	–––	–––	0.60
A1	0.179	0.199	0.219
A2	0.323	0.338	0.353
A3	0.017	0.022	0.027
b	0.241	0.271	0.301
D	1.61	1.66	1.71
E	2.21	2.26	2.31
e	0.40 BSC		

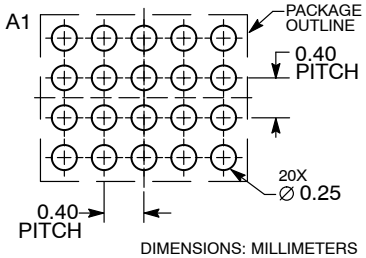
GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WLCSP20, 1.66X2.26X0.6**	**PAGE 1 OF 1**

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