

# MOSFET - Power, Single N-Channel

## 40 V, 1.1 mΩ, 240 A



ON Semiconductor®

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### FDBL9406L-F085

#### Features

- Small Footprint (TOLL) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	40	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$ 240 A
		$T_C = 100^\circ\text{C}$	$P_D$ 300 W
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	300 W
		$T_C = 100^\circ\text{C}$	150 W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ 43 A
		$T_A = 100^\circ\text{C}$	31 A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$ 3.5 W
		$T_A = 100^\circ\text{C}$	1.7 W
Pulsed Drain Current	$T_C = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$ 2755	A
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	100	A
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 85 \text{ A}; L = 60 \mu\text{H}$ )	$E_{AS}$	217	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

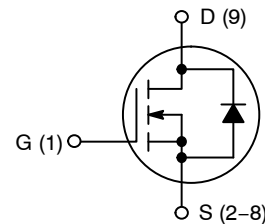
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS

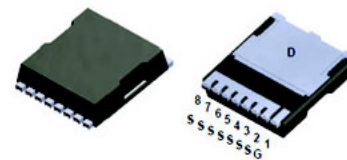
Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	0.5	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	43	$^\circ\text{C}/\text{W}$

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Current is limited by bondwire configuration.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
40 V	1.1 mΩ @ 10 V	80 A
	1.78 mΩ @ 4.5 V	

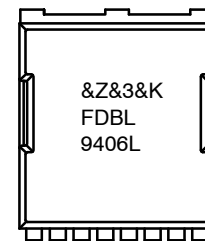


N-CHANNEL MOSFET



MO-299A  
CASE 100CU

#### MARKING DIAGRAM



&Z = Assembly Plant Code  
 &3 = Numeric Date Code  
 &K = Lot Code  
 FDBL9406L = Specific Device Code

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

# FDBL9406L–F085

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	40	-	-	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$		-	19.3	-	mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, T_J = 25^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, T_J = 175^\circ\text{C}$	-	-	1	$\text{mA}$
Zero Gate Voltage Drain Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1	1.9	3	V
Threshold Temperature Coefficient	$V_{GS(th)}/T_J$		-	-6.5	-	mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 80\text{ A}$	-	0.9	1.1	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 40\text{ A}$	-	1.25	1.78	

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 20\text{ V}$	-	8600	-	pF
Output Capacitance	$C_{oss}$		-	2380	-	pF
Reverse Transfer Capacitance	$C_{rss}$		-	106	-	pF
Gate Resistance	$R_g$	$V_{GS} = 0.5\text{ V}, f = 1\text{ MHz}$	-	2	-	$\Omega$
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 32\text{ V}, I_D = 80\text{ A}$	-	58	-	nC
		$V_{GS} = 10\text{ V}, V_{DS} = 32\text{ V}, I_D = 80\text{ A}$	-	121	-	
Threshold Gate Charge	$Q_{g(th)}$	$V_{GS} = 0\text{ to }1\text{ V}$	-	7	-	
Gate-to-Source Gate Charge	$Q_{gs}$	$V_{DD} = 32\text{ V}, I_D = 80\text{ A}$	-	26	-	
Gate-to-Drain "Miller" Charge	$Q_{gd}$		-	19	-	
Plateau Voltage	$V_{GP}$		-	3.2	-	V

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, I_D = 80\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$	-	22	-	ns
Turn-On Rise Time	$t_r$		-	22	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	134	-	ns
Turn-Off Fall Time	$t_f$		-	44	-	ns

### DRAIN-SOURCE DIODE CHARACTERISTICS

Source-to-Drain Diode Voltage	$V_{SD}$	$I_{SD} = 80\text{ A}, V_{GS} = 0\text{ V}$	-	0.81	1.25	V
		$I_{SD} = 40\text{ A}, V_{GS} = 0\text{ V}$	-	0.77	1.2	V
Reverse Recovery Time	$T_{RR}$	$V_{GS} = 0\text{ V}, dI_{SD}/dt = 100\text{ A}/\mu\text{s}$ $I_S = 80\text{ A}$	-	77	-	ns
Charge Time	$t_a$		-	38	-	
Discharge Time	$t_b$		-	39	-	
Reverse Recovery Charge	$Q_{RR}$		-	95	-	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

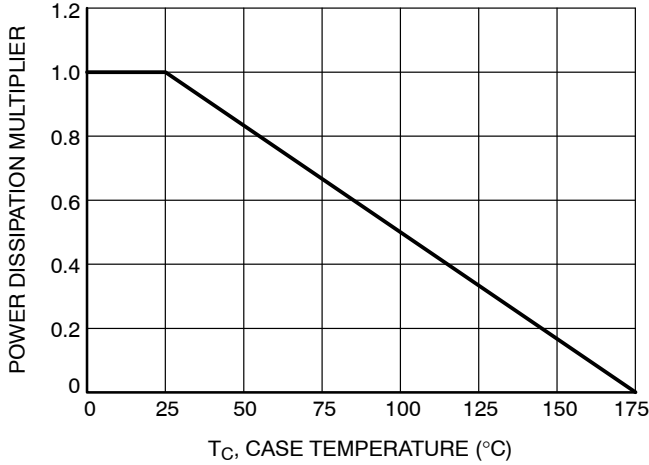


Figure 1. Normalized Power Dissipation vs. Case Temperature

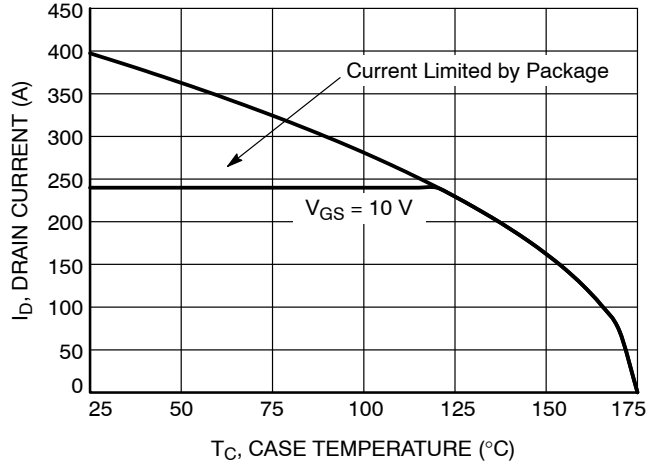


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

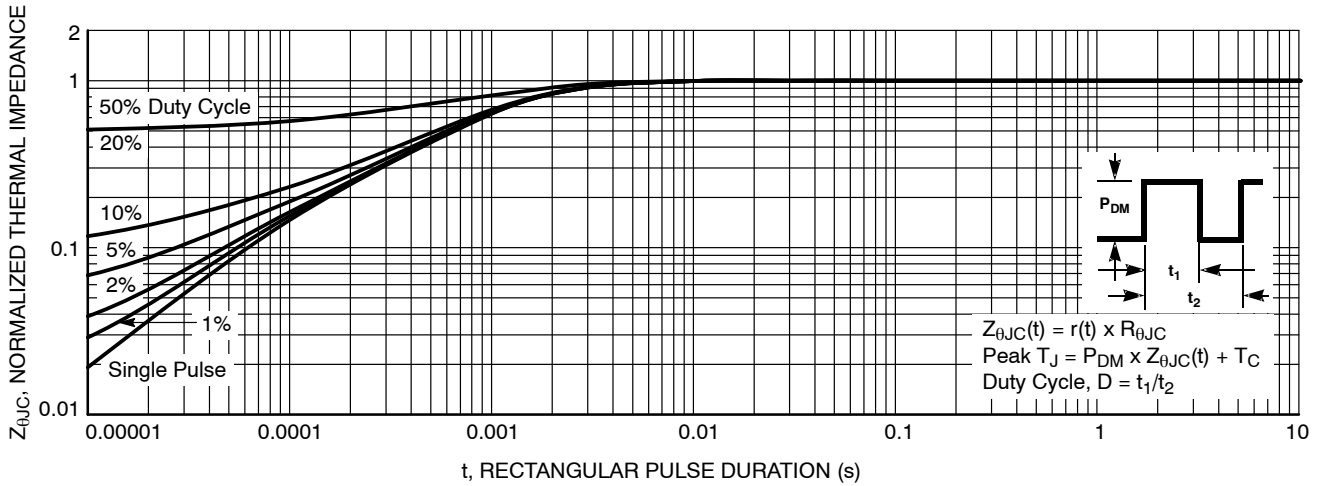


Figure 3. Normalized Maximum Transient Thermal Impedance

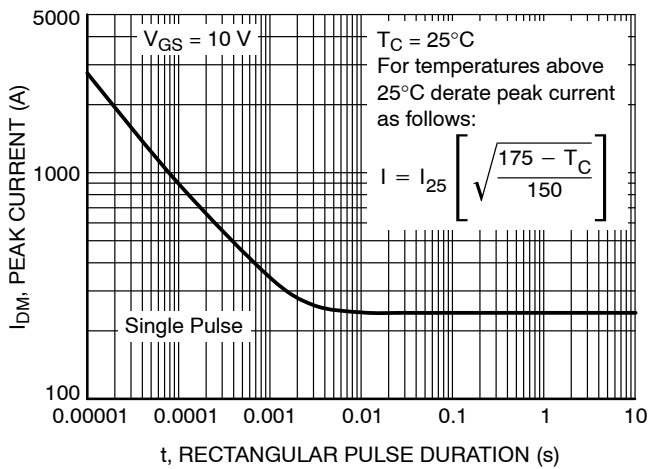


Figure 4. Peak Current Capability

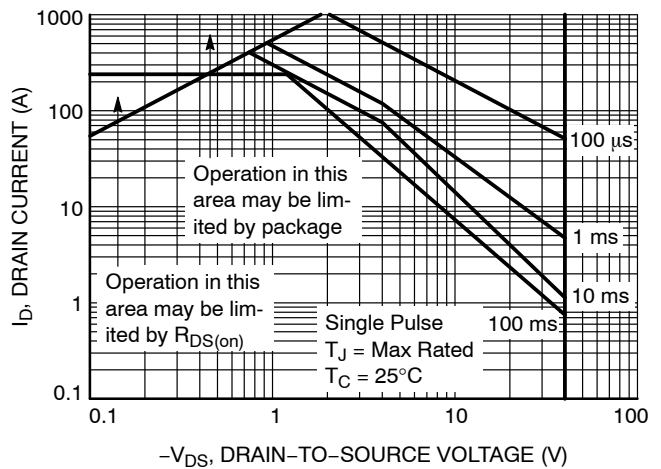


Figure 5. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS

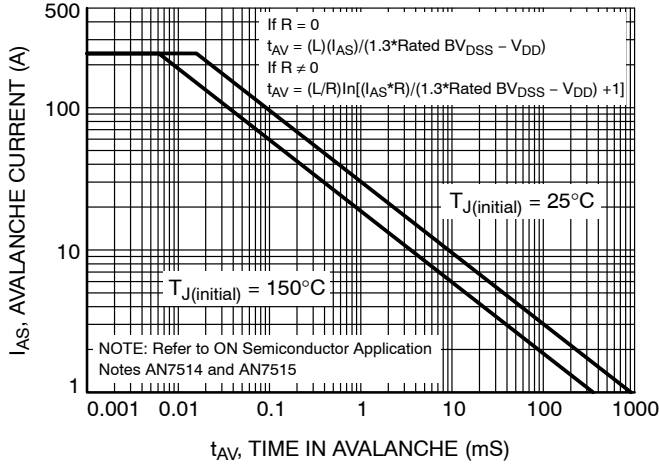


Figure 6. Unclamped Inductive Switching Capability

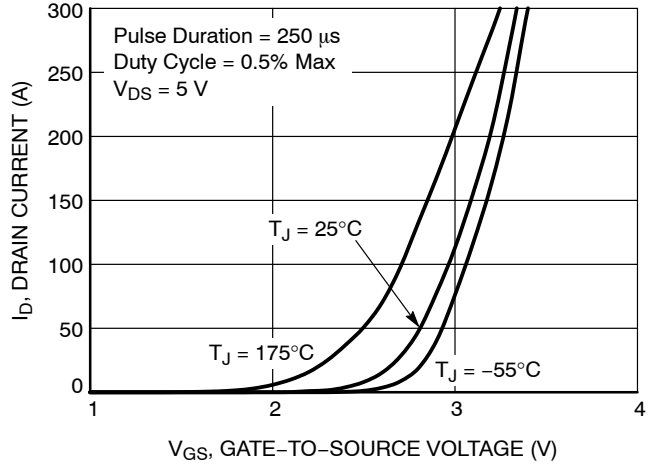


Figure 7. Transfer Characteristics

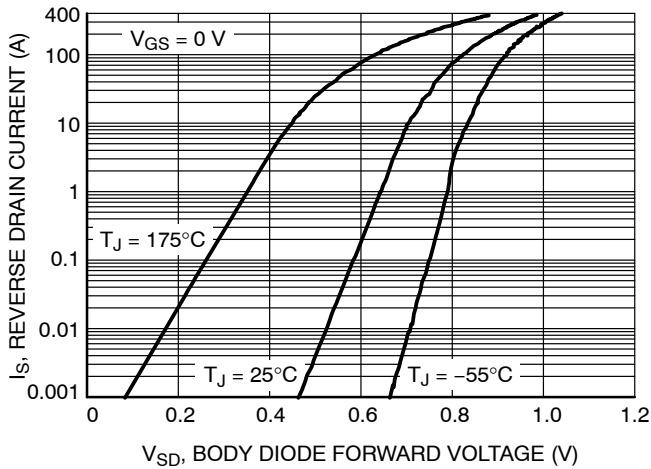


Figure 8. Forward Diode Characteristics

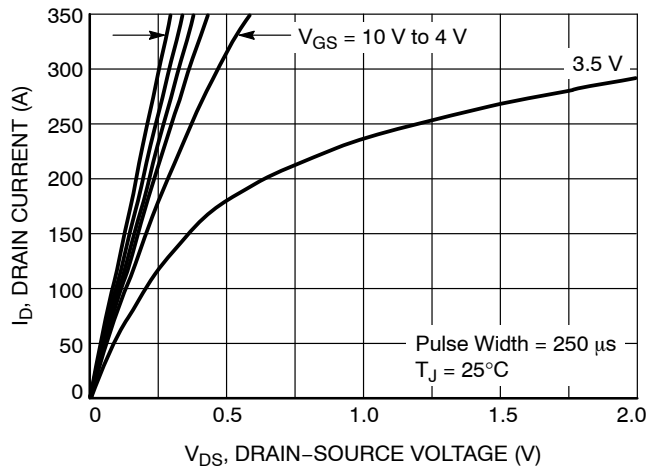


Figure 9. Saturation Characteristics

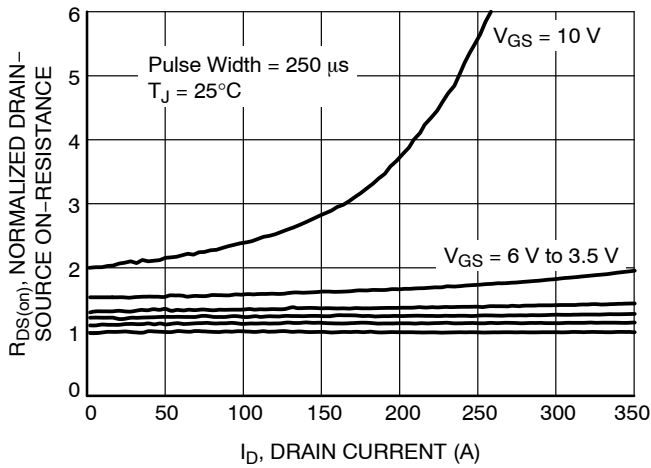


Figure 10. Normalized  $R_{DS(on)}$  vs. Drain Current

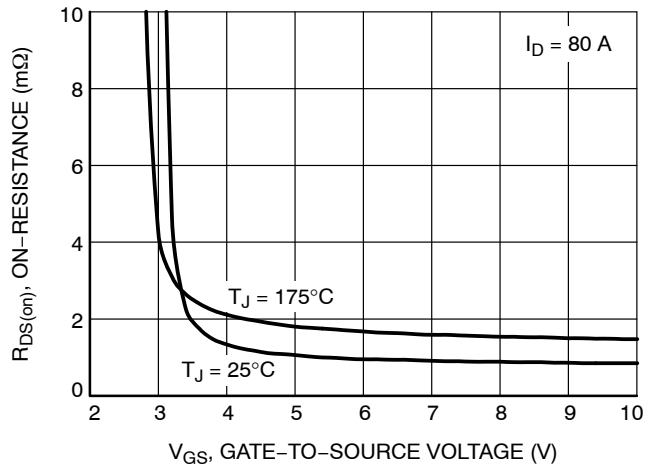


Figure 11.  $R_{DS(on)}$  vs. Gate Voltage

TYPICAL CHARACTERISTICS

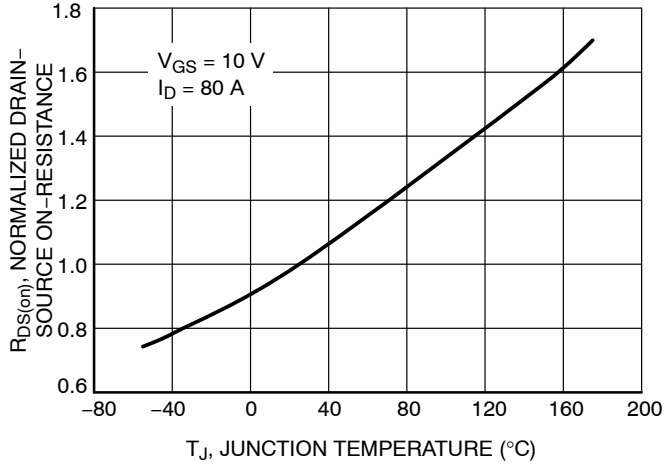


Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature

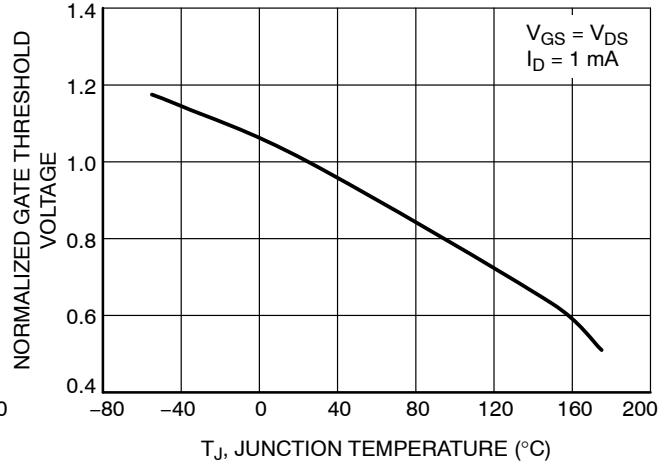


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

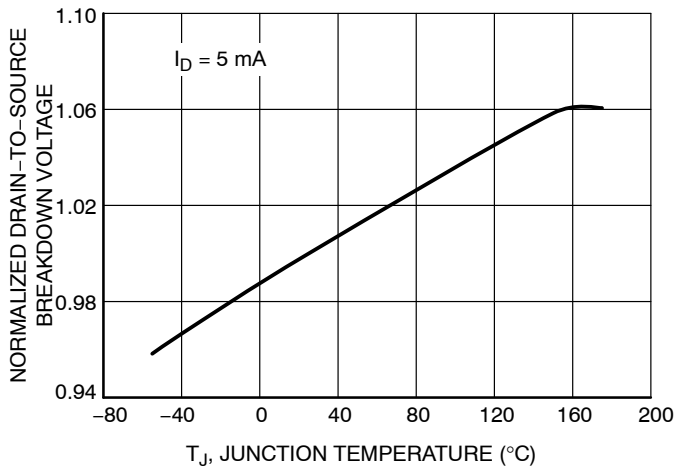


Figure 14. Normalized Drain-to-Source Breakdown Voltage vs. Junction Temperature

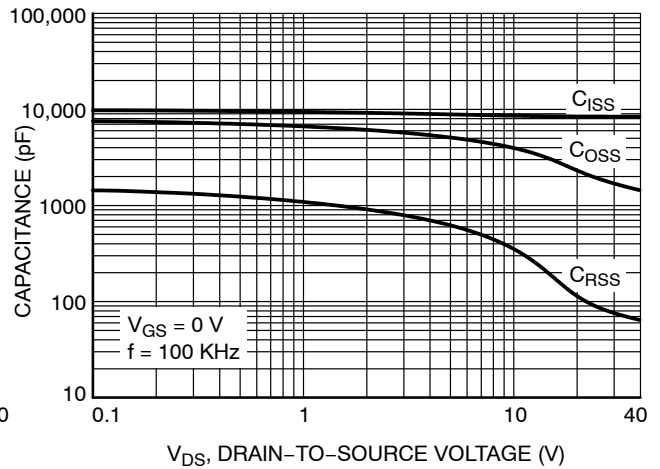


Figure 15. Capacitance vs. Drain-to-Source Voltage

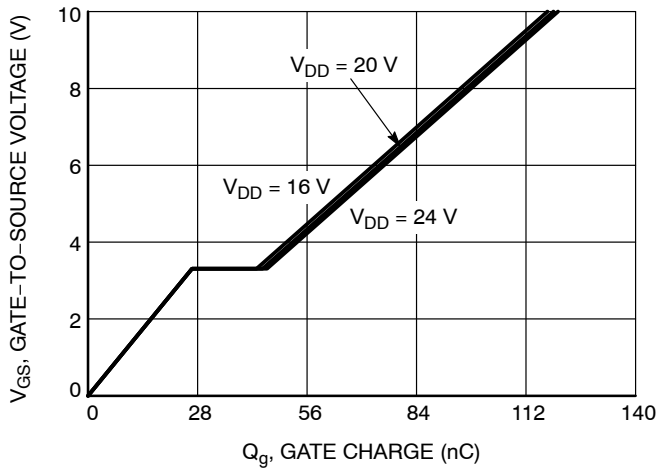


Figure 16. Gate Charge vs. Gate-to-Source Voltage

# FDBL9406L-F085

## PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Reel Size	Tape Width	Quantity
FDBL9406L-F085	FDBL9406L	H-PSOF8L (Pb-Free / Halogen Free)	13"	24 mm	2000 Units

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

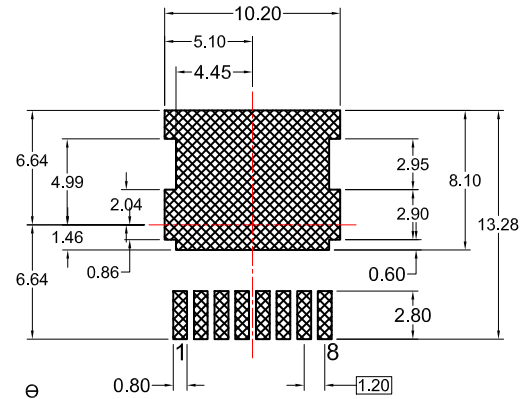
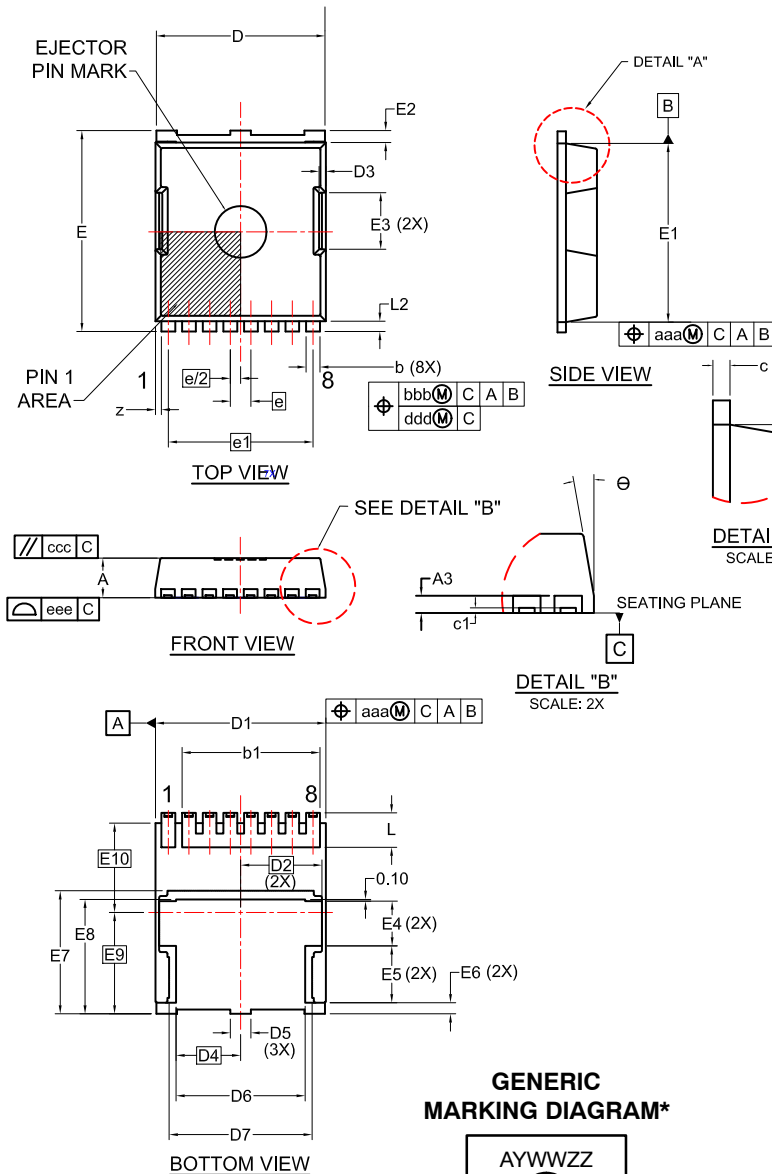
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



## H-PSOF8L 11.68x9.80 CASE 100CU ISSUE A

DATE 06 JAN 2020



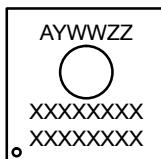
**LAND PATTERN RECOMMENDATION**  
\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

- NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
  2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
  3. CONTROLLING DIMENSION: MILLIMETERS.
  4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
  5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
  6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A3	0.40	0.50	0.60
b	0.70	0.80	0.90
b1	8.00 REF		
c	0.40	0.50	0.60
c1	0.10	--	--
D	9.70	9.80	9.90
D1	9.80	9.90	10.00
D2	4.73 BSC		
D3	0.40 REF		
D4	3.75 BSC		
D5	--	1.20	--
D6	7.40	7.50	7.60
D7	(8.30)		
E	11.58	11.68	11.78
E1	10.28	10.38	10.48
E2	0.60	0.70	0.80
E3	3.30 REF		
E4	--	2.60	--

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
K	1.50	1.57	1.70
L	1.90	2.00	2.10
L2	0.50	0.60	0.70
z	0.35 REF		
θ	0°	--	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		
E5	--	3.30	--
E6	--	0.65	--
E7	7.15 REF		
E8	6.55	6.65	6.75
E9	5.89 BSC		
E10	5.19 BSC		

### GENERIC MARKING DIAGRAM\*



- A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code  
XXXX = Specific Device Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>H-PSOF8L 11.68x9.80</b>	<b>PAGE 1 OF 1</b>

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