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FDA24N50F

May 2014

N-Channel UniFETTM FRFET[®] MOSFET 500 V, 24 A, 200 m Ω

Features

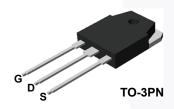
- $R_{DS(on)}$ = 166 m Ω (Typ.) @ V_{GS} = 10 V, I_D = 12 A
- Low Gate Charge (Typ. 65 nC)
- Low C_{rss} (Typ. 32 pF)
- 100% Avalanche Tested
- · Improved dv/dt Capability
- · RoHS Compliant

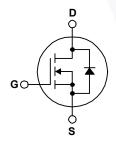
Applications

- PDP TV
- Uninterruptible Power Supply
- · AC-DC Power Supply

Description

UniFETTM MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its trr is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FDA24N50F	Unit
V _{DSS}	Drain to Source Voltage			500	V
V _{GSS}	Gate to Source Voltage		9	±30	V
	Drain Current	- Continuous (T _C = 25°C)		24	Α
ID	Drain Current	- Continuous (T _C = 100°C)		14	A
I _{DM}	Drain Current	- Pulsed	- Pulsed (Note 1)		Α
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		(Note 2)	1872	mJ
I _{AR}	Avalanche Current		(Note 1)	24	Α
E _{AR}	Repetitive Avalanche Ener	gy	(Note 1)	27	mJ
dv/dt	Peak Diode Recovery dv/d	t	(Note 3)	20	V/ns
D	Dawer Dissination	(T _C = 25°C)		270	W
P_{D}	Power Dissipation	- Derate Above 25°C		2.2	W/°C
T _J , T _{STG}	Operating and Storage Ter	nperature Range		-55 to +150	οС
T _L	Maximum Lead Temperatu	re for Soldering, 1/8" from Case for 5	Seconds	300	°С

Thermal Characteristics

Symbol	Parameter FDA24N50F			
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.46	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	0/00	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDA24N50F	FDA24N50F	TO-3PN	Tube	N/A	N/A	30 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_J = 25^{\circ} C$	500	-	-	V
ΔBV _{DSS} / ΔΤ _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C	-	0.6	-	V/°C
1	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	-	-	1	μА
IDSS	Zero Gate voltage Drain Current	$V_{DS} = 400 \text{ V}, T_C = 125^{\circ}\text{C}$	-	-	10	μΑ
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	-	-	±100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	3.0	-	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 12 A	-	0.166	0.2	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 12 A	-	30	1	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V - 25 V V - 0 V		-	3240	4310	pF
C _{oss}	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		-	450	600	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12		-\	32	48	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 400 V, I _D = 24 A,		-	65	85	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V		- \	18	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	1)	Note 4,)	-	26	-	nC

Switching Characteristics

t _{d(on)}	Turn-On Delay Time			-	49	108	ns
t _r	Turn-On Rise Time	$V_{DD} = 250 \text{ V}, I_D = 24 \text{ A},$		-	105	220	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V, R}_{G} = 25 \Omega$		-	165	340	ns
t _f	Turn-Off Fall Time		(Note 4)	-	87	185	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current			-	24	Α
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	96	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 24 A	-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 24 A,	-	264	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	1.4	/ -	μС

Notes

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. L = 6.5 mH, I_{AS} = 24 A, V_{DD} = 50 V, R_G = 25 Ω , starting T_J = 25°C.
- 3. $I_{SD} \le 24$ A, di/dt ≤ 200 A/ μs , $V_{DD} \le BV_{DSS}$, starting T $_J$ = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

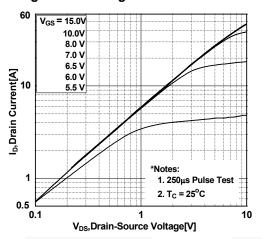


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

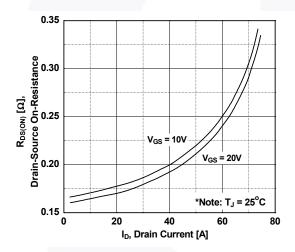


Figure 5. Capacitance Characteristics

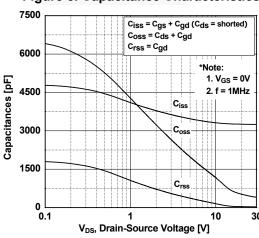


Figure 2. Transfer Characteristics

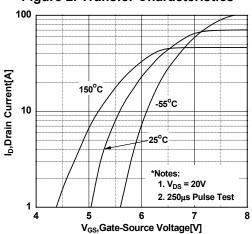


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

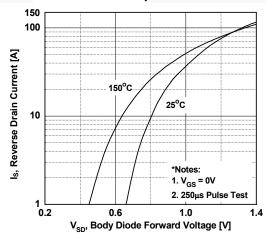
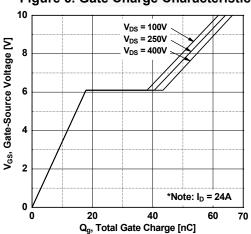


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

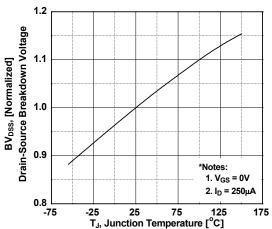


Figure 8. On-Resistance Variation vs. Temperature

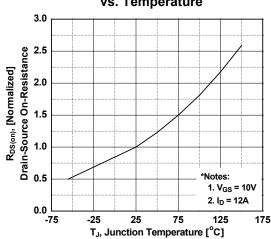


Figure 9. Maximum Safe Operating Area

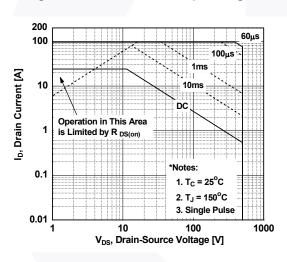


Figure 10. Maximum Drain Current vs. Case Temperature

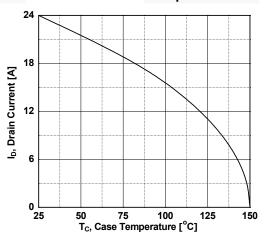
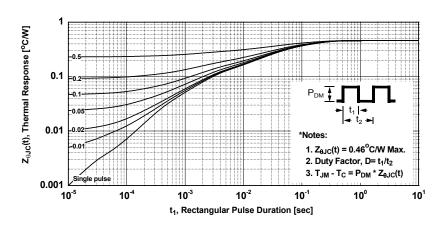


Figure 11. Transient Thermal Response Curve



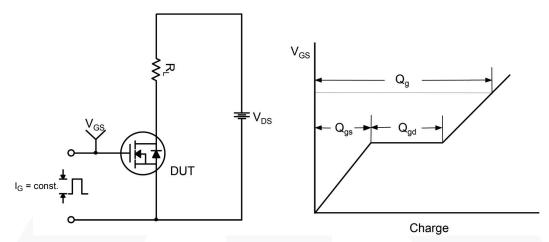


Figure 12. Gate Charge Test Circuit & Waveform

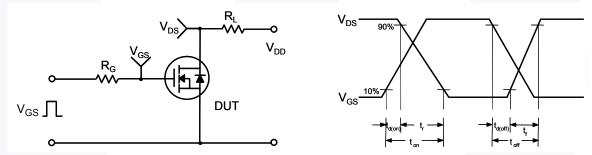


Figure 13. Resistive Switching Test Circuit & Waveforms

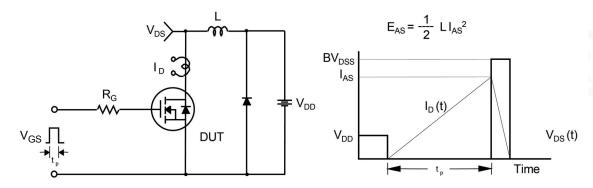


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

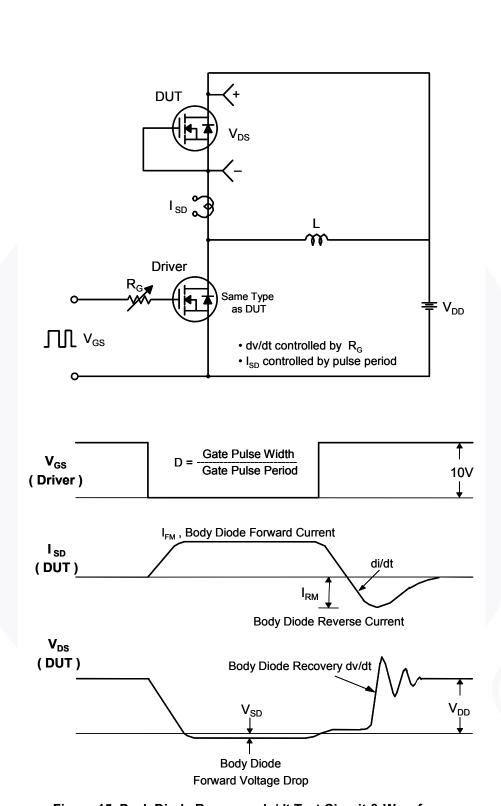
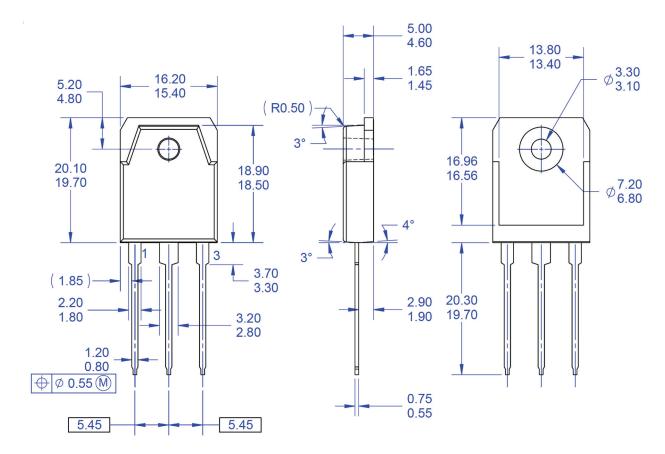
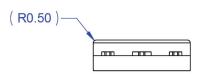


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions





NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSION AND TOLERANCING PER ASME14.5-2009.
- D) DIMENSIONS ARE EXCLUSSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSSIONS.
 E) DRAWING FILE NAME: TO3PN03AREV1.
- FAIRCHILD SEMICONDUCTOR.

Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65

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