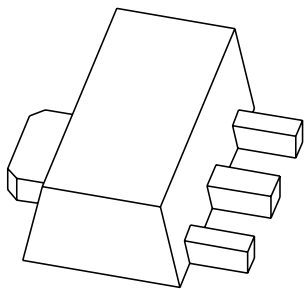


# DATA SHEET



## **BST50; BST51; BST52** NPN Darlington transistors

Product specification  
Supersedes data of 2001 Feb 20

2004 Dec 09

# NPN Darlington transistors

# BST50; BST51; BST52

### FEATURES

- High current (max. 0.5 A)
- Low voltage (max. 80 V)
- Integrated diode and resistor.

### APPLICATIONS

- Industrial switching applications such as:
  - Print hammer
  - Solenoid
  - Relay and lamp driving.

### DESCRIPTION

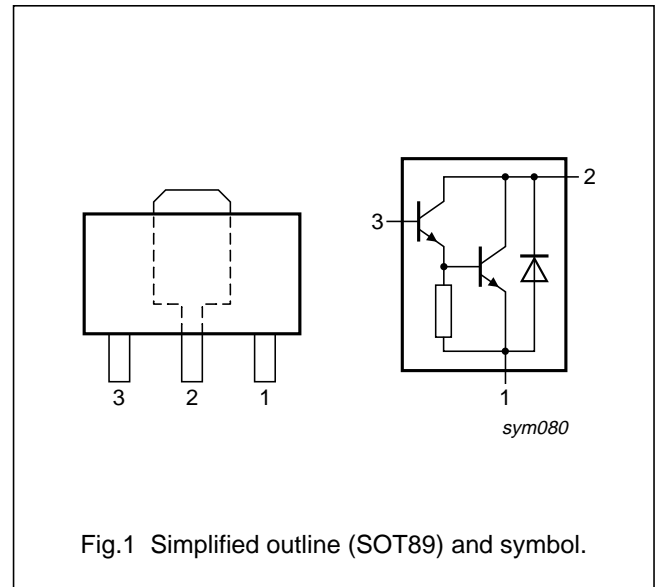
NPN Darlington transistor in a SOT89 plastic package.  
PNP complements: BST60, BST61 and BST62.

### MARKING

TYPE NUMBER	MARKING CODE
BST50	AS1
BST51	AS2
BST52	AS3

### PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base



### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
BST50	SC-62	plastic surface mounted package; collector pad for good heat transfer; 3 leads	SOT89
BST51			
BST52			

## NPN Darlington transistors

## BST50; BST51; BST52

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CBO</sub>	collector-base voltage	open emitter			
	BST50		–	60	V
	BST51		–	80	V
	BST52		–	90	V
V <sub>CES</sub>	collector-emitter voltage	V <sub>BE</sub> = 0 V			
	BST50		–	45	V
	BST51		–	60	V
	BST52		–	80	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	5	V
I <sub>C</sub>	collector current (DC)		–	1	A
I <sub>CM</sub>	peak collector current		–	2	A
I <sub>B</sub>	base current (DC)		–	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	1.3	W
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	ambient temperature		–65	+150	°C
T <sub>stg</sub>	storage temperature		–65	+150	°C

**Note**

- Device mounted on a printed-circuit board, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.  
For other mounting conditions, see *“Thermal considerations for SOT89 in the General Part of associated Handbook”*.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	note 1	96	K/W
R <sub>th(j-s)</sub>	thermal resistance from junction to soldering point		16	K/W

**Note**

- Device mounted on a printed-circuit board, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.  
For other mounting conditions, see *“Thermal considerations for SOT89 in the General Part of associated Handbook”*.

## NPN Darlington transistors

## BST50; BST51; BST52

**CHARACTERISTICS**

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

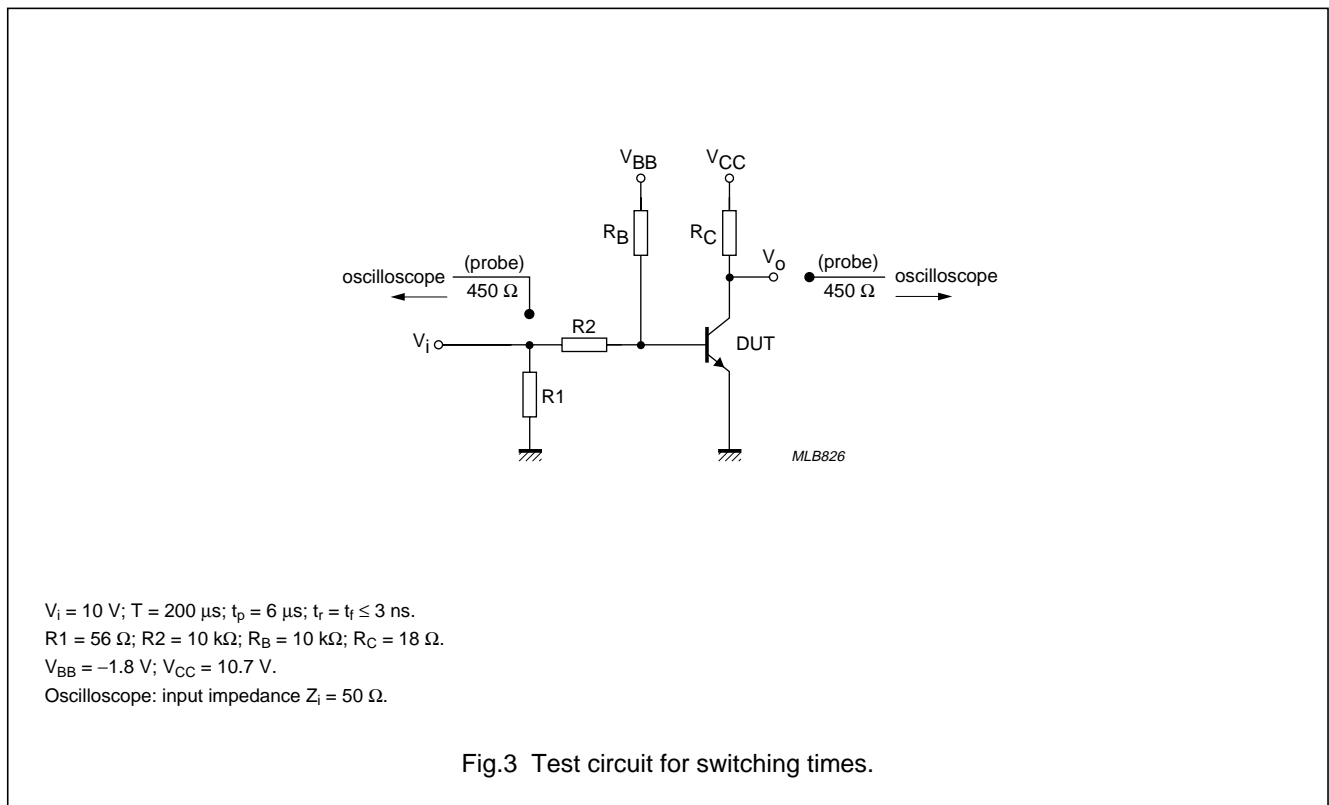
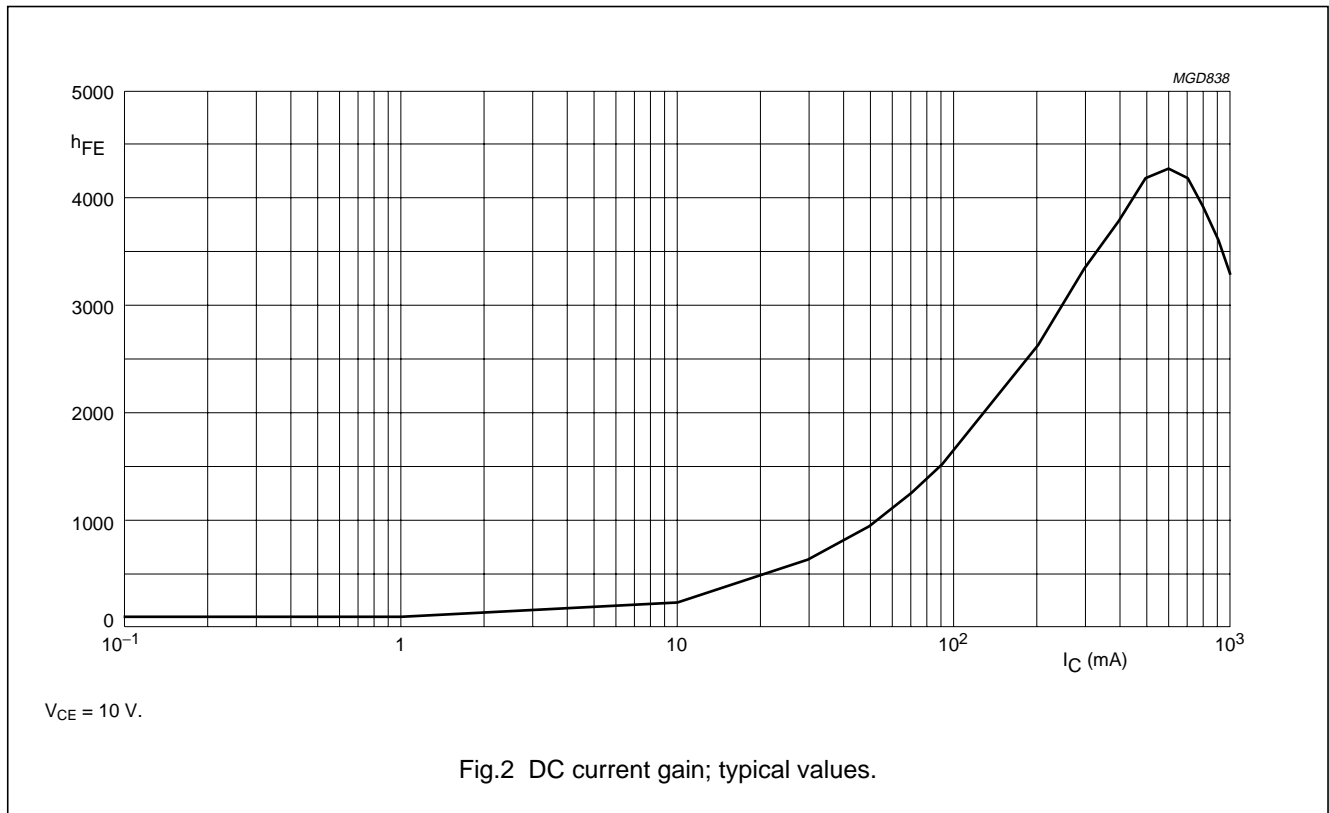
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CES}$	collector-emitter cut-off current					
	BST50	$V_{BE} = 0\text{ V}; V_{CE} = 45\text{ V}$	–	–	50	nA
	BST51	$V_{BE} = 0\text{ V}; V_{CE} = 60\text{ V}$	–	–	50	nA
	BST52	$V_{BE} = 0\text{ V}; V_{CE} = 80\text{ V}$	–	–	50	nA
$I_{EBO}$	emitter-base cut-off current	$I_C = 0\text{ A}; V_{EB} = 4\text{ V}$	–	–	50	nA
$h_{FE}$	DC current gain	$V_{CE} = 10\text{ V}$ ; note 1; (see Fig.2)				
		$I_C = 150\text{ mA}$	1000	–	–	
		$I_C = 500\text{ mA}$	2000	–	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 500\text{ mA}; I_B = 0.5\text{ mA}$	–	–	1.3	V
		$I_C = 500\text{ mA}; I_B = 0.5\text{ mA}; T_j = 150\text{ °C}$	–	–	1.3	V
$V_{BEsat}$	base-emitter saturation voltage	$I_C = 500\text{ mA}; I_B = 0.5\text{ mA}$	–	–	1.9	V
$f_T$	transition frequency	$I_C = 500\text{ mA}; V_{CE} = 5\text{ V}; f = 100\text{ MHz}$	–	200	–	MHz
<b>Switching times (between 10% and 90% levels); (see Fig.3)</b>						
$t_{on}$	turn-on time	$I_{Con} = 500\text{ mA}; I_{Bon} = 0.5\text{ mA}; I_{Boff} = -0.5\text{ mA}$	–	400	–	ns
$t_{off}$	turn-off time		–	1500	–	ns

**Note**

1. Pulse test:  $t_p \leq 300\text{ }\mu\text{s}$ ;  $\delta \leq 0.02$ .

NPN Darlington transistors

BST50; BST51; BST52



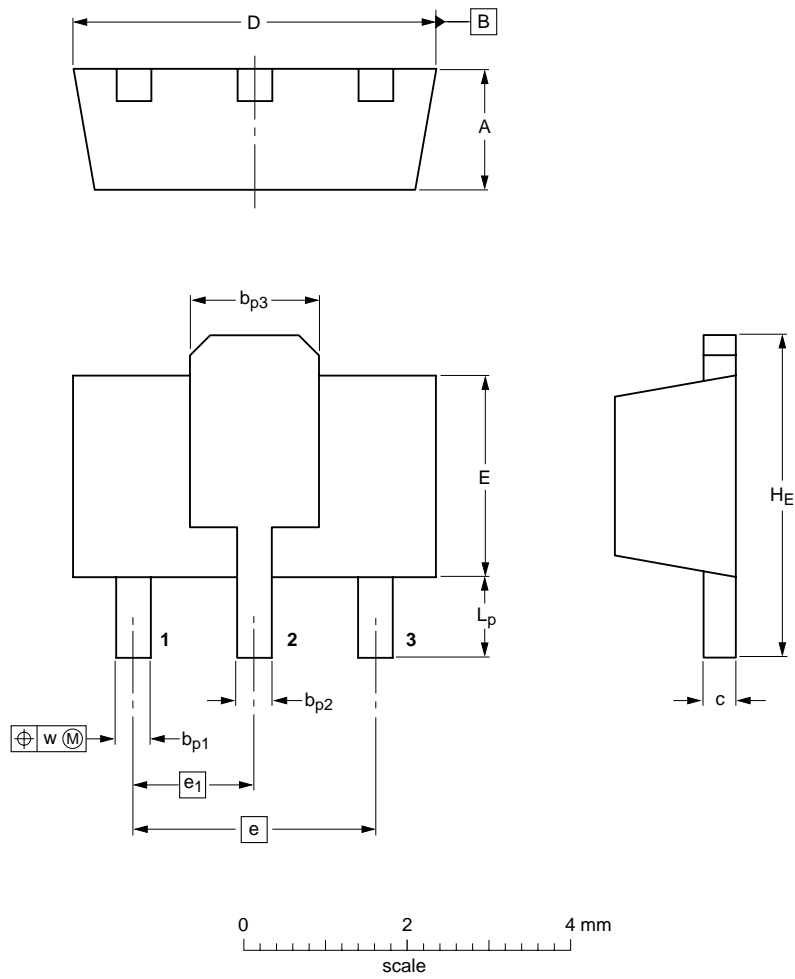
NPN Darlington transistors

BST50; BST51; BST52

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>p1</sub>	b <sub>p2</sub>	b <sub>p3</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.23	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	1.2 0.8	0.13

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT89		TO-243	SC-62		99-09-13 04-08-03

## NPN Darlington transistors

## BST50; BST51; BST52

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