MC32XSG

Multi-purpose high-side switches

Rev. 4 — 3 September 2020 Data sheet: technical data

1 General description

The 32XSG family is designed to control, protect and diagnose various type of low-voltage loads with enhanced precision. It combines flexibility, extended digital and analog feedbacks, safety, and robustness. This family offers the possibility to configure outputs to improve EMC, manage frequency and duty cycle, adapt the dynamic overcurrent profiles to the load, program the current sense ratio of each output, and many more. Devices can be driven either by the embedded SPI module or by direct inputs in Fail-safe operation mode and remains operational, controllable and protected in this case. This product is driven by SMARTMOS technology.

2 Features and benefits

- Penta high-side switches with high transient capability
- 16-bit 5.0 MHz SPI control of overcurrent profiles, channel control including PWM duty cycles, output On and Off openload detections, thermal shutdown and prewarning, and fault reporting
- Output current monitoring with programmable synchronization signal and supply voltage feedback
- Fail-safe mode
- External smart power switch control
- Operating voltage is 7.0 V to 30 V with sleep current < 5.0 µA, extended mode from 6.0 V to 32 V
- -16 V reverse polarity and ground disconnect protections
- Compatible PCB foot print and SPI software driver among the family

3 Simplified application diagram

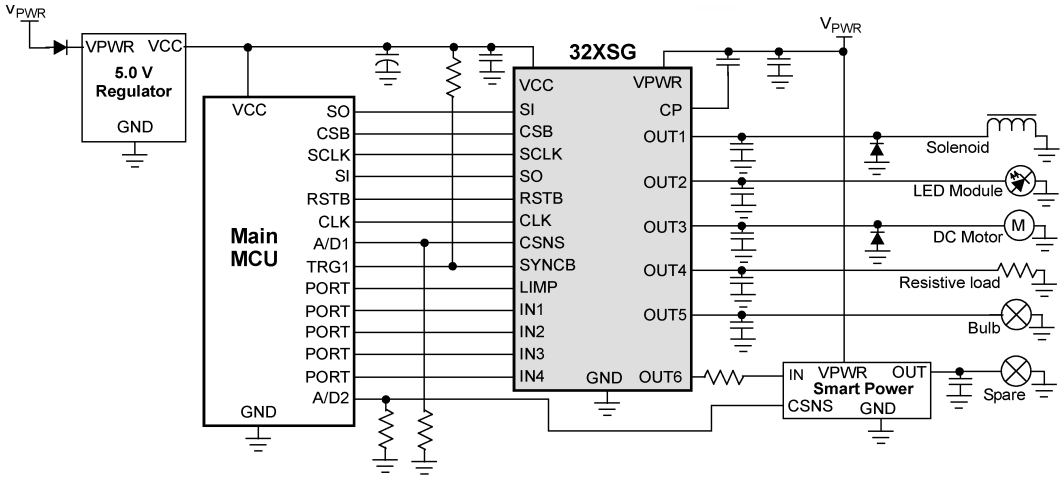


Figure 1. Simplified application diagram

4 Applications

- Low-voltage exterior lighting
- Low-voltage industrial lighting
- Low-voltage automation systems
- Halogen lamps
- Incandescent bulbs
- Light-emitting diodes (LEDs)
- HID Xenon ballasts
- DC Motors

5 Ordering information

This section describes the part numbers available to be purchased along with their differences.

Table 1. Orderable parts

Part number	Notes	Temperature (T_A)	Package	OUT1 $R_{DS(on)}$	OUT2 $R_{DS(on)}$	OUT3 $R_{DS(on)}$	OUT4 $R_{DS(on)}$	OUT5 $R_{DS(on)}$	OUT6
MC07XSG517EK	[1]	–40 °C to 125 °C	SOIC54 pins exposed pad	17 mΩ	17 mΩ	7.0 mΩ	7.0 mΩ	7.0 mΩ	Yes
MC17XSG500EK			SOIC32 pins exposed pad	17 mΩ	17 mΩ	17 mΩ	17 mΩ	17 mΩ	Yes
MC17XSG500BEK			SOIC32 pins exposed pad	17 mΩ	17 mΩ	17 mΩ	17 mΩ	17 mΩ	Yes

[1] To order parts in tape and reel, add the R2 suffix to the part number.

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search.

6 Internal block diagram

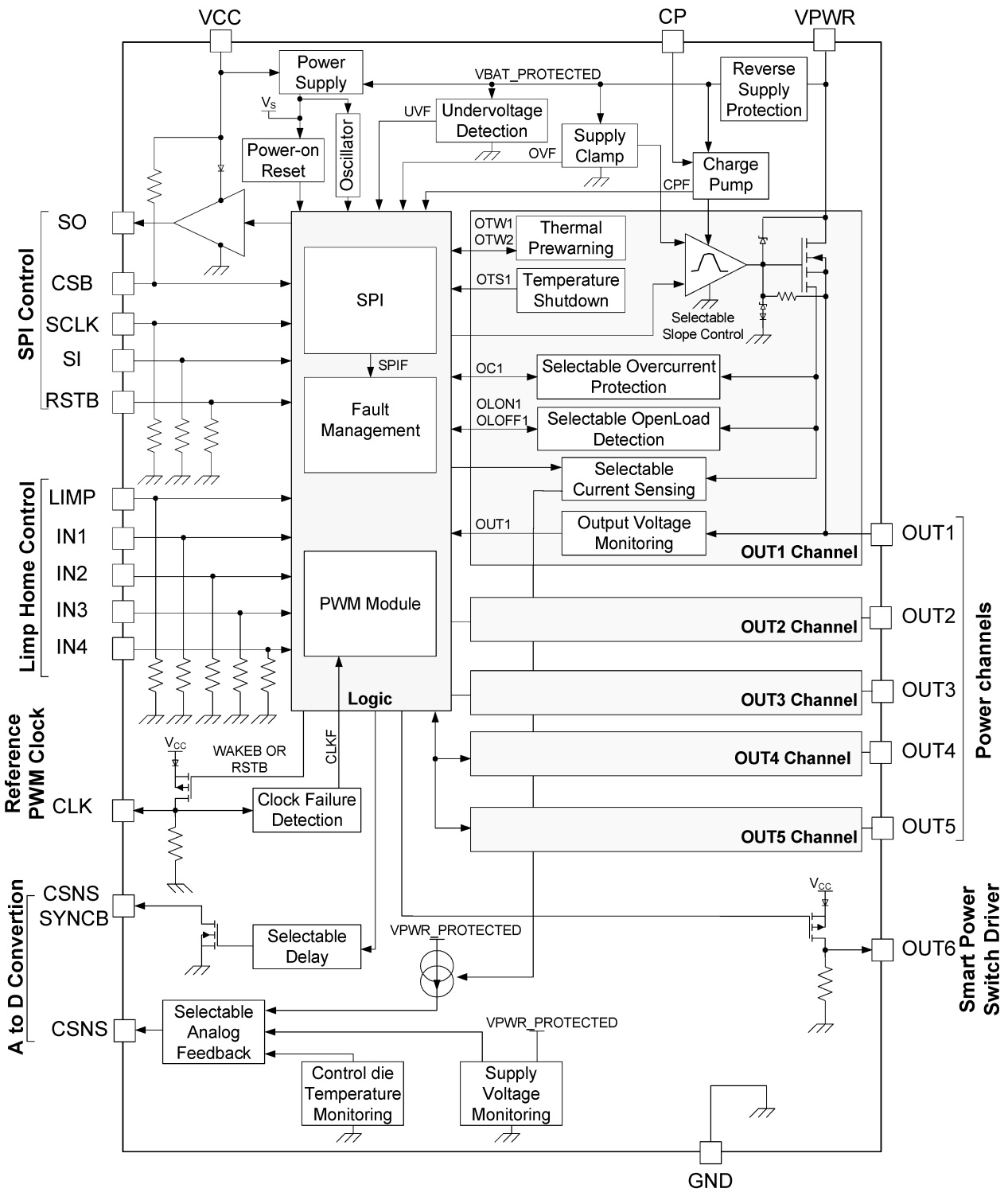


Figure 2. 32XSG simplified internal block diagram

7 Pinning information

7.1 Pinning

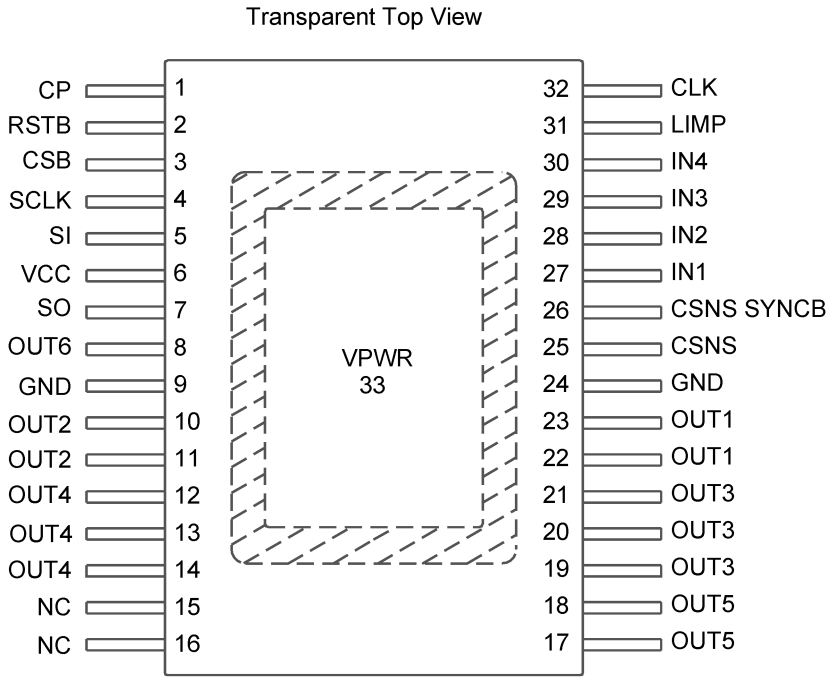


Figure 3. Pin configuration for 32-pin SOIC-EP package

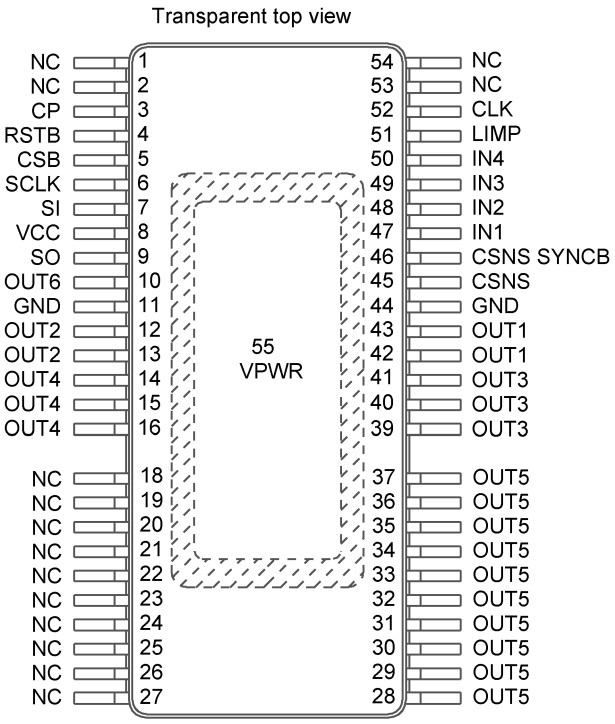


Figure 4. Pin configuration for 54-pin SOIC-EP package

7.2 Pin description

Table 2. Pin description

Symbol	Pin 32 SOIC-EP	Pin 54 SOIC-EP [1]	Pin function	Formal name	Definition
CP	1	3	Internal supply	Charge pump	This pin is the connection for an external capacitor for charge pump use only.
RSTB	2	4	SPI	Reset	This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low-current Sleep mode. This pin has a passive internal pull-down.
CSB	3	5	SPI	Chip select	This input pin is connected to a chip select output of a master microcontroller (MCU). When this digital signal is high, SPI signals are ignored. Asserting this pin low starts an SPI transaction. The transaction is indicated as completed when this signal returns to high level. This pin has a passive internal pull-up to VCC through a diode
SCLK	4	6	SPI	Serial clock	This input pin is connected to the MCU providing the required bit shift clock for SPI communication. This pin has a passive internal pull-down.

Symbol	Pin 32 SOIC-EP	Pin 54 SOIC-EP [1]	Pin function	Formal name	Definition
SI	5	7	SPI	Serial input	This pin is the data input of the SPI communication interface. The data at the input are sampled on the positive edge of the SCLK. This pin has a passive internal pull-down.
VCC	6	8	Power supply	MCU power supply	This pin is a power supply pin for internal logic, the SPI I/Os and the OUT6 driver.
SO	7	9	SPI	Serial Output	This output pin is connected to the SPI Serial Data Input pin of the MCU or to the SI pin of the next device of a daisy chain of devices. The SPI changes on the negative edge of SCLK. When CSB is high, this pin is high- impedance.
OUT6	8	10	Output	External Solid State	This output pin controls an external Smart Power Switch by logic level. This pin has a passive internal pull-down.
GND	9 and 24	11 and 44	Ground	Ground	These pins are the ground for the logic and analog circuitries of the device. For ESD and electrical parameter accuracy purpose, the ground pins must be shorted on the board.
OUT2	10 to 11	12 to 13	Output	Channel #2	Protected high-side power output pins to the load.
OUT4	12 to 14	14 to 16	Output	Channel #4	Protected high-side power output pins to the load.
NC	15, 16	1, 2, 18 to 27, 53, 54	N/A	Not connected	These pins are not connected. It is recommended to connect these pint to ground
OUT5	17 to 18	28 to 37	Output	Channel #5	Protected high-side power output pins to the load
OUT3	19 to 21	39 to 41	Output	Channel #3	Protected high-side power output pins to the load
OUT1	22 to 23	42 to 43	Output	Channel #1	Protected high-side power output pins to the load
CSNS	25	45	Feedback	Current sense	This pin reports an analog value proportional to the designated OUT[1:5] output current or the temperature of the exposed pad or the supply voltage. It is used externally to generate a ground-referenced voltage for the microcontroller (MCU). Current recopy and analog voltage feedbacks are SPI programmable.

Symbol	Pin 32 SOIC-EP	Pin 54 SOIC-EP [1]	Pin function	Formal name	Definition
CSNS SYNCB	26	46	Feedback	Current sense synchronization	This open drain output pin allows synchronizing the MCU A/D conversion. This pin requires an external pull-up resistor to VCC.
IN1	27	47	Input	Direct input #1	This input wakes up the device. This input pin is used to directly control corresponding channel in Fail mode. During Normal mode the control of the outputs by the control inputs is SPI programmable. This pin has a passive internal pull-down.
IN2	28	48	Input	Direct input #2	This input wakes up the device. This input pin is used to directly control corresponding channel in Fail mode. During Normal mode the control of the outputs by the control inputs is SPI programmable. This pin has a passive internal pull-down.
IN3	29	49	Input	Direct input #3	This input wakes up the device. This input pin is used to directly control corresponding channel in Fail mode. During Normal mode the control of the outputs by the control inputs is SPI programmable. This pin has a passive internal pull-down.
IN4	30	50	Input	Direct input #4	This input wakes up the device. This input pin is used to directly control corresponding channel in Fail mode. During Normal mode the control of the outputs by the control inputs is SPI programmable. This pin has a passive internal pull-down.
LIMP	31	51	Input	Limp Home	The Fail mode can be activated by this digital input. This pin has a passive internal pull-down.
CLK	32	52	Input/Output	Device mode feedback Reference PWM clock	This pin is an input/output pin. It is used to report the device sleep-state information. It is also used to apply reference PWM clock which is divided by 2^8 in Normal operating mode. This pin has a passive internal pull-down.
VPWR	33	55	Power supply	Power supply	This exposed pad connects to the positive power supply and is the source of operational power for the device.

[1] Pins 17 and 38 are omitted.

8 General product characteristics

8.1 Relationship between ratings and operating requirements

The analog portion of device is supplied by the voltage applied to the VPWR exposed pad. Thereby the supply of internal circuitry (logic in case of a V_{CC} disconnect, charge pump, gate drive,…) is derived from the VPWR pin.

In case of a reverse supply:

- The internal supply rail is protected (max. –16 V)
- The output drivers (OUT1… OUT5) are switched on, to reduce the power consumption in the drivers when using incandescent bulbs.

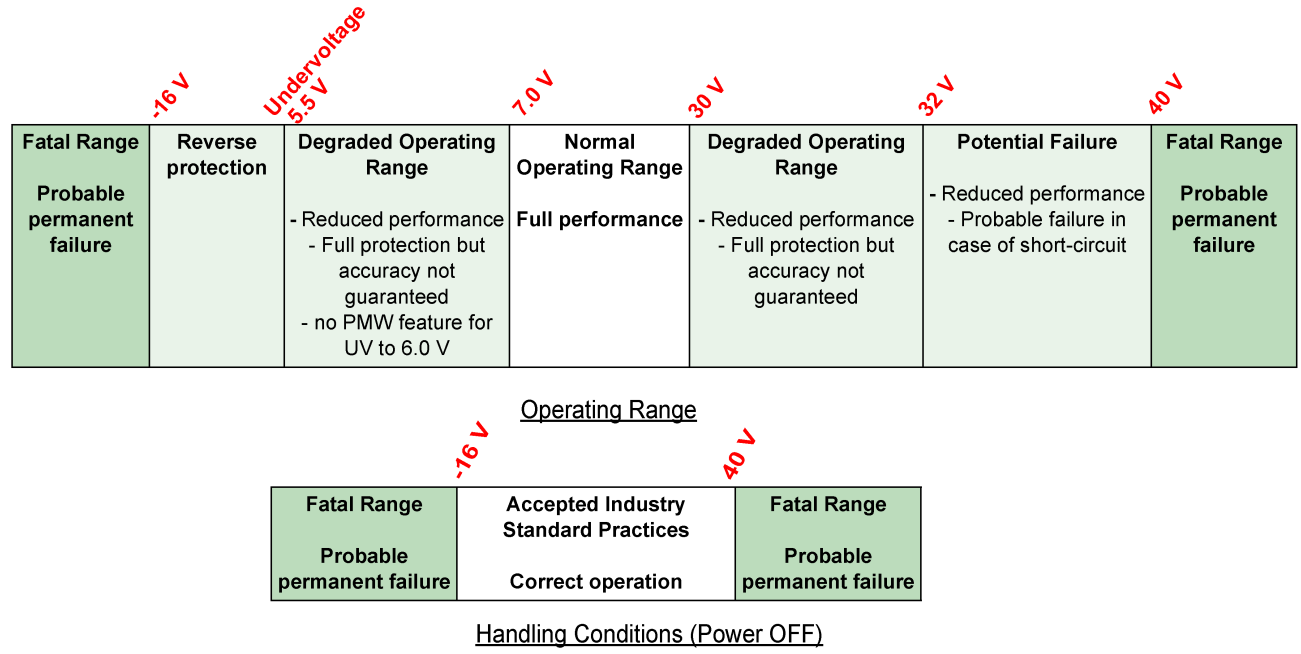


Figure 5. Ratings vs. operating requirements (VPWR pin)

The device's digital circuitry is powered by the voltage applied to the VCC pin. If VCC is disconnected, the logic part is supplied by the VPWR pin.

The output driver for SPI signals, CLK pin (wake feedback), and OUT6 are supplied by the VCC pin only. This pin must be protected externally in case of a reverse polarity, and in case of a high-voltage disturbance.

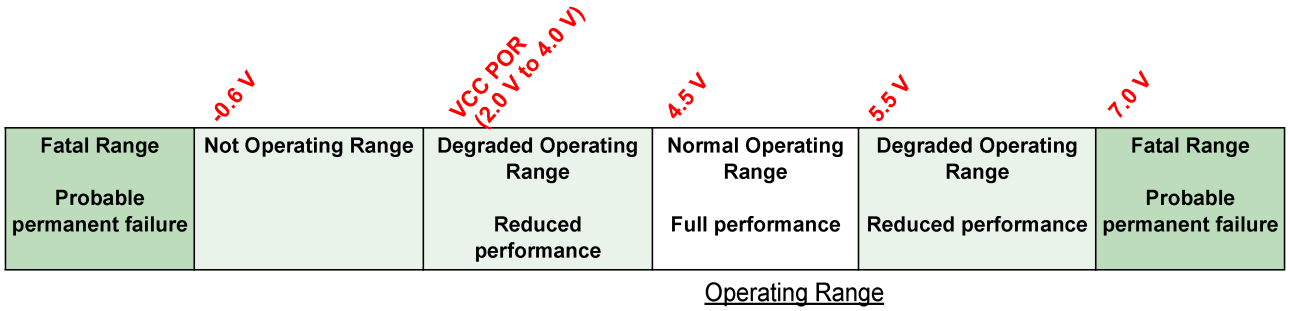


Figure 6. Ratings vs. operating requirements (VCC pin)

8.2 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
ELECTRICAL RATINGS				
V_{PWR}	VPWR voltage range	–16	40	V
V_{CC}	VCC logic supply voltage	–0.3	7.0	V
V_{IN}	Digital input voltage [1] IN1:IN4 and LIMP CLK, SI, SCLK, CSB, and RSTB	 –0.3 –0.3	 40 20	V
V_{OUT}	Digital output voltage [1] SO, CSNS, CSNS SYNCB, OUT6, CLK	 –0.3	 20	V
I_{CL}	Negative digital input clamp current [2]	—	5.0	mA
I_{OUT}	Power channel current [3] 7.0 mΩ channel 17 mΩ channel	 — —	 11 5.5	A
E_{CL}	Power channel clamp energy capability [4] 7.0 mΩ channel - Initial T_J = 150 °C 17 mΩ channel - Initial T_J = 150 °C	 — —	 100 50	mJ

[1] Exceeding voltage limits on those pins may cause a malfunction or permanent damage to the device.
[2] Maximum current in negative clamping for IN1:IN4, LIMP, RSTB, CLK, SI, SO, SCLK, and CSB pins.
[3] Continuous high-side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
[4] Active clamp energy using single-pulse method (L = 2.0 mH, R_L = 0 Ω, V_{PWR} = 14 V). Refer to Section 10.1.4 "Digital diagnostics"

8.3 Thermal characteristics

Table 4. Thermal ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
THERMAL RATINGS				
	Operating temperature [1]			
T_A	Ambient	–40	+125	°C
T_J	Junction	–40	+150	
T_{STG}	Storage temperature	–55	+150	°C
T_{PPRT}	Peak package reflow temperature during reflow [2] [3]	—	260	°C
THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS				
$R_{\Theta JB}$	Junction-to-Board [4]	—	2.5	°C/W
$R_{\Theta JA}$	Junction-to-Ambient, Natural Convection, Four-Layer Board (2s2p) [5] [6]	—	17.4	°C/W
$R_{\Theta JC}$	Junction-to-Case (Case top surface) [7]	—	10.6	°C/W

[1] To achieve high reliability over 10 years of continuous operation, the device's continuous operating junction temperature should not exceed 125 °C.
[2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
[3] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.
[4] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[5] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[6] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
[7] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

8.4 Operating conditions

This section describes the operating conditions of the device. Conditions apply to the following data, unless otherwise noted.

Table 5. Operating conditions

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Min	Max	Unit
V_{PWR}	Functional operating supply voltage - Device is fully functional. All features are operating.	7.0	30	V
	Reverse supply	–16	—	V
V_{CC}	Functional operating supply voltage - Device is fully functional. All features are operating.	4.5	5.5	V

8.5 Supply currents

This section describes the current consumption characteristics of the device.

Table 6. Supply currents

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, –40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A= 25 °C under nominal conditions, unless otherwise noted.

Symbol	Ratings	Min	Typ	Max	Unit
VPWR CURRENT CONSUMPTIONS					
I_{QVPWR}	Sleep mode measured at V_{PWR} = 24 V [1] [2] T_A = 25 °C T_A = 125 °C	 — —	 25 35	 35 45	 µA
I_{VPWR}	Operating mode measured at V_{PWR} = 24 V [2]	—	7.0	10	mA
VCC CURRENT CONSUMPTIONS					
I_{QVCC}	Sleep mode measured at V_{CC} = 5.5 V and V_{PWR} = 24 V	—	15	50	µA
I_{VCC}	Operating mode measured at V_{CC} = 5.5 V and V_{PWR} = 30 V (SPI frequency 5.0 MHz)	—	2.8	4.0	mA

[1] With the OUT1… OUT5 power channels grounded.
[2] With the OUT1… OUT5 power channels opened.

9 General IC functional description and application information

9.1 Introduction

The 32XSG family provides advanced features. It consists of two similar devices compatible in terms of software drivers and package footprints. It diagnoses the low-current using an enhanced current sense precision with a synchronization pin, as well as driving high power motors with a perfect control of its current consumption. It combines flexibility through daisy chainable SPI 5.0 MHz, extended digital and analog feedback, safety, and robustness. It integrates an enhanced PWM module with 8-bit duty cycle capability and a PWM frequency prescaler per power channel.

9.2 Features

The main attributes of the 32XSG are:

- Penta high-side switches with overload, overtemperature, and undervoltage protection
- Control output for one external smart power switch
- 16-bit SPI communication interface with daisy chain capability
- Dedicated control inputs for use in fail mode
- Analog feedback pin with SPI programmable multiplexer and sync signal
- Channel diagnosis by SPI communication
- Advanced current sense mode for low current use
- Synchronous PWM module with external clock, prescaler, and multiphase feature
- Excellent EMC behavior
- Power net and reverse polarity protection
- Ultra low-power mode
- Scalable and flexible family concept
- Board layout compatible SOIC54 and SOIC32 package with exposed pad

9.3 Block diagram

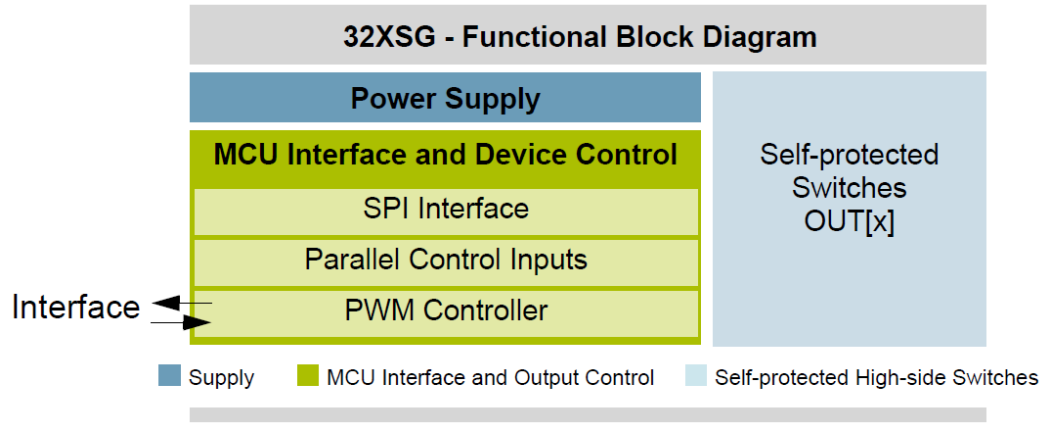


Figure 7. Functional block diagram

9.3.1 Self-protected high-side switches

OUT1… OUT5 are the output pins of the power switches. The power channels are protected against various kinds of short-circuits, and have active clamp circuitry which may be activated when switching off inductive loads. Many protective and diagnostic functions are available.

9.3.2 Power supply

The device operates with supply voltages from 5.5 V to 40 V (V_{PWR}), but is full spec. compliant only between 7.0 V and 30 V. The VPWR pin supplies power to the internal regulator, analog, and logic circuit blocks. The VCC pin (5.0 V typ.) supplies the output register of the serial peripheral interface (SPI). Consequently, the SPI registers cannot be read without presence of V_{CC}. The employed IC architecture guarantees a low quiescent current in sleep mode.

9.3.3 MCU interface and device control

In normal mode the power output channels are controlled by the embedded PWM module, which is configured by the SPI register settings. For bidirectional SPI communication, V_{CC} has to be in the authorized range. Failure diagnostics and configuration are also performed through the SPI port. The reported failure types are: openload, short-circuit to supply, severe short-circuit to ground, overcurrent, overtemperature, clock-fail, under and overvoltage. The device allows driving loads at different frequencies to 400 Hz.

9.4 Functional description

The device has four fundamental operating modes: Sleep, Normal, Fail and Power off. It possesses multiple high-side switches (power channels) each of which can be controlled independently:

- In Normal mode by SPI interface. A second supply voltage (V_{CC}) is required for bidirectional SPI communication.

- In Fail mode by the corresponding direct inputs IN1… IN4. The OUT5 and OUT6 are off in this mode.

9.5 Modes of operation

The operating modes are based on the signals:

- wake = (IN1_ON) or (IN2_ON) or (IN3_ON) or (IN4_ON) or (RSTB). For more details, see Section 10.3.3.2 "Logic I/O plausibility check".
- fail = (SPI_fail) or (LIMP). For more details, see Section 10.3.3.1 "Loss of communication interface".

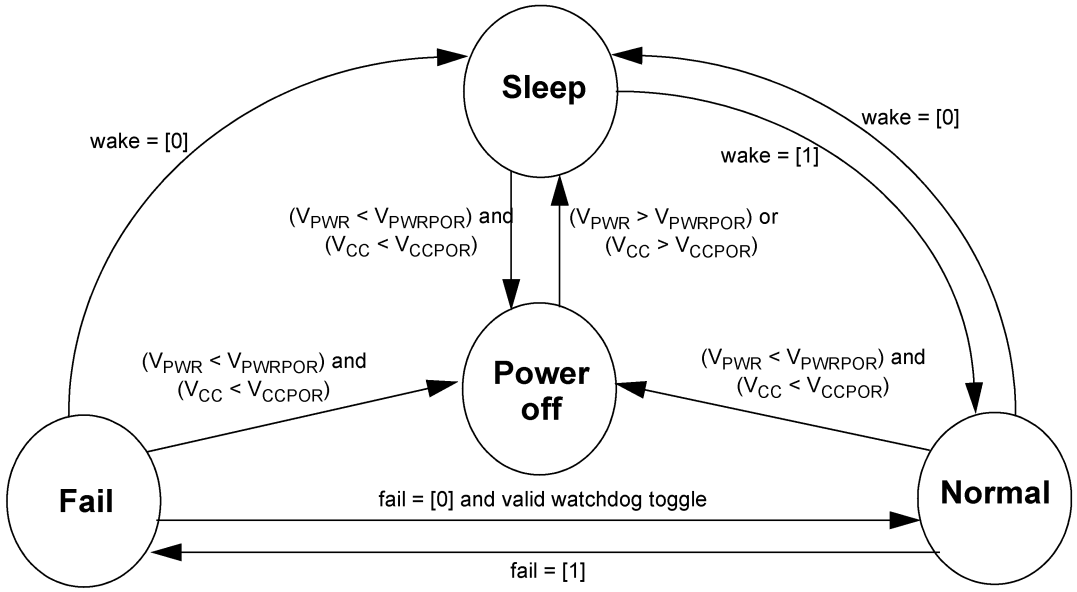


Figure 8. General IC operating modes

9.5.1 Power Off mode

The power off mode is applied when V_{PWR} and V_{CC} are below the power on reset threshold ($V_{PWR\ POR}$, $V_{CC\ POR}$). No functionality is available, but the device is protected by the clamping circuits in power off. See Section 10.2.3 "Supply voltage disconnection".

9.5.2 Sleep mode

The sleep mode is used to provide ultra low-current consumption. During sleep mode:

- the component is inactive and all outputs are disabled
- the outputs are protected by the clamping circuits
- the pull-up/pull-down resistors are present

Sleep mode is the default mode of the device after applying the supply voltages (V_{PWR} or V_{CC}) prior to any wake-up condition (wake = [0]). Wake-up from sleep mode is provided by the wake signal.

9.5.3 Normal mode

The Normal mode is the regular operating mode of the device. The device is in Normal mode, when the device is in the wake state (wake = [1]) and no fail condition (fail = [0]) is detected. During Normal mode:

- the power outputs are under control of the SPI and its programmable PWM mode
- the power outputs are protected by the overload protection circuits
- the digital diagnostic feature transfers status of the smart switch via the SPI
- the analog feedback output (CSNS and CSNS SYNCB) can be controlled by the SPI

9.5.4 Fail mode

The device enters the Fail mode, when:

- the LIMP input pin is high (logic [1])
- or a SPI failure is detected

During Fail mode (wake = [1] & fail = [1]):

- the OUT1… OUT4 outputs are directly controlled by the corresponding control inputs (IN1… IN4)
- the OUT5… OUT6 are turned off and not controllable
- the PWM module is not available
- while no SPI control is feasible, the SPI diagnosis is functional (depending on the fail mode condition):
  - SO reports the content of SO register defined by SOA0 to 3 bits
- the outputs are fully protected in case of an overload, overtemperature, and undervoltage
- no analog feedback is available
- the max. output overcurrent profile is activated (OCLO and window times)
- in case of an overload condition or undervoltage, the autorestart feature controls the OUT1… OUT4 outputs
- in case of an overtemperature condition, OCHI1 detection, or severe short-circuit detection, the corresponding output is latched OFF until a new wake-up event

9.5.5 Mode transitions

After a wake-up:

- a power on reset is applied and all SPI SI and SO registers are cleared (logic[0])
- the faults are blanked during $t_{BLANKING}$

The device enters in Normal mode after start-up if following sequence is provided:

- V_{PWR} and V_{CC} power supplies must be above their undervoltage thresholds (sleep mode)
- generate wake-up event (wake = 1) setting RSTB from 0 to 1

The device initialization is completed after 50 µsec (typ). During this time, the device is robust in case of VPWR interrupts higher than 150 nsec. The transition from “Normal mode” to “Fail mode” is executed immediately when a fail condition is detected. During the transition, the SPI SI settings are cleared and the SPI SO registers are not cleared.

When the Fail mode condition is a:

- LIMP input, WD toggle timeout, WD toggle sequence, or a SPI modulo 16 error, the SPI diagnosis is available during Fail mode
- SI/SO stuck to static level, the SPI diagnosis is not available during Fail mode

The transition from “Fail mode” to “Normal mode” is enabled when:

- the fail condition is removed and
- two SPI commands are sent within a valid watchdog cycle (first WD=[0] and then WD=[1])

During this transition:

- all SPI SI and SO registers are cleared (logic[0])
- the DSF (device status flag) in the registers #1… #7 and the RCF (Register Clearer flag) in the device status register #1 are set (logic[1])

To delatch the RCF diagnosis, a read command of the quick status register #1 must be performed.

9.6 SPI interface and configurations

9.6.1 Introduction

The SPI is used to:

- control the device in case of Normal mode
- provide diagnostics in case of Normal and Fail mode

The SPI is a 16-bit full-duplex synchronous data transfer interface with daisy chain capability. The interface consists of four I/O lines with 5.0 V CMOS logic levels and termination resistors:

- The SCLK pin clocks the internal shift registers of the device
- The SI pin accepts data into the input shift register on the rising edge of the SCLK signal
- The SO pin changes its state on the rising edge of SCLK and reads out on the falling edge
- The CSB enables the SPI interface:
  - with the leading edge of CSB, the registers load
  - while CSB is logic [0], SI/SO data shifts
  - with the trailing edge of the CSB signal, SPI data latches into the internal registers
  - when CSB is logic [1], the signals at the SCLK and SI pins are ignored and SO is high-impedance

When the RSTB input is:

- low (logic [0]), the SPI and the fault registers are reset. The wake state then depends on the status of the input pins (IN_ON1… IN_ON4)
- high (logic[1]), the device is in wake status and the SPI is enabled

The functionality of the SPI is checked by a plausibility check. During a SPI failure, the device enters Fail mode.

9.6.2 SPI input register and bit descriptions

The first nibble of the 16-bit data word (D15… D12) serves as address bits.

Table 7. SPI input register and bit descriptions

Register	SI address						SI data									
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
name	x	4 bit address				WD	11 bit address										

11 bits (D10… D0) are used as data bits.

The D11 bit is the WD toggle bit. This bit has to be toggled with each write command.

When the toggling of the bit is not executed within the WD timeout, a SPI fail is detected.

All register values are logic [0] after a reset. The predefined value is off/inactive unless otherwise noted.

Register	SI address					SI data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Initialization 1	0	0	0	0	0	WD	WD SEL	SYNC EN1	SYNC EN0	MUX2	MUX1	MUX0	0	SOA3	SOA2	SOA1	SOA0
Initialization 2	1	0	0	0	1	WD	OCHI THERMAL	x	X	X	OCHI OD5	OCHI OD4	OCHI OD3	OCHI OD2	OCHI OD1	PWM sync	OTW SEL
CH1 control	2	0	0	1	0	WD	PH11	PH01	ON1	PWM71	PWM61	PWM51	PWM41	PWM31	PWM21	PWM11	PWM01
CH2 control	3	0	0	1	1	WD	PH12	PH02	ON2	PWM72	PWM62	PWM52	PWM42	PWM32	PWM22	PWM12	PWM02
CH3 control	4	0	1	0	0	WD	PH13	PH03	ON3	PWM73	PWM63	PWM53	PWM43	PWM33	PWM23	PWM13	PWM03
CH4 control	5	0	1	0	1	WD	PH14	PH04	ON4	PWM74	PWM64	PWM54	PWM44	PWM34	PWM24	PWM14	PWM04
CH5 control	6	0	1	1	0	WD	PH15	PH05	ON5	PWM75	PWM65	PWM55	PWM45	PWM35	PWM25	PWM15	PWM05
CH6 control	7	0	1	1	1	WD	PH16	PH06	ON6	PWM76	PWM66	PWM56	PWM46	PWM36	PWM26	PWM16	PWM06
output control	8	1	0	0	0	WD	X	X	X	X	X	ON6	ON5	ON4	ON3	ON2	ON1
Global PWM control	9-1	1	0	0	1	WD	0	X	X	X	X	GPWM EN6	GPWM EN5	GPWM EN4	GPWM EN3	GPWM EN2	GPWM EN1
	9-2	1	0	0	1	WD	1	X	X	GPWM7	GPWM6	GPWM5	GPWM4	GPWM3	GPWM2	GPWM1	GPWM0
overcurrent control	10-1	1	0	1	0	WD	0	OCLO5	OCLO4	OCLO3	OCLO2	OCLO1	ACM EN5	ACM EN4	ACM EN3	ACM EN2	ACM EN1
	10-2	1	0	1	0	WD	1	NO OCHI5	NO OCHI4	NO OCHI3	NO OCHI2	NO OCHI1	SHORT OCHI5	SHORT OCHI4	SHORT OCHI3	SHORT OCHI2	SHORT OCHI1
Input enable	11	1	0	1	1	WD	0	X	X	INEN14	INEN04	INEN13	INEN03	INEN12	INEN02	INEN11	INEN01
prescaler settings	12-1	1	1	0	0	WD	0	PRS15	PRS05	PRS14	PRS04	PRS13	PRS03	PRS12	PRS02	PRS11	PRS01
	12-2	1	1	0	0	WD	1	X	X	X	X	X	X	X	X	PRS16	PRS06
OL control	13-1	1	1	0	1	WD	0	X	X	X	X	X	OLOFF EN5	OLOFF EN4	OLOFF EN3	OLOFF EN2	OLOFF EN1
OLLED control	13-2	1	1	0	1	WD	1	X	X	X	X	OLLED TRIG	OLLED EN5	OLLED EN4	OLLED EN3	OLLED EN2	OLLED EN1
increment / decrement	14	1	1	1	0	WD	INCR SGN	INCR15	INCR05	INCR14	INCR04	INCR13	INCR03	INCR12	INCR02	INCR11	INCR01
testmode	15	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X

WD	#0~#14	= watchdog toggle bit
SOA0 ~ SOA3	#0	= address of next SO data word
SOA MODE	#0	= single read address of next SO data word
MUX0 ~ MUX2	#0	= CSNS multiplexer setting
SYNC EN0~ SYNC EN1	#0	= SYNC delay setting
WD SEL	#0	= watchdog timeout select
OTW SEL	#1	= over temperature warning threshold selection
PWM SYNC	#1	= reset clock module
OCHI ODx	#1	= OCHI window on load demand
OCHI THERMAL	#1	= OCHI1 level depending on control die temperature
PWM0x ~ PWM7x	#2~#7	= PWM value (8-bit)
PH0x ~ PH1x	#2~#7	= phase control
ONx	#2~#8	= channel on/off ind. OCHI control
GPWM ENx	#9-1	= global PWM enable
GPWM1 ~ GPWM7	#9-2	= global PWM value (8Bit)
ACM ENx	#10-1	= advanced current sense mode enable
OCLOx	#10-1	= OCLO level control
SHORT OCHIx	#10-2	= use short OCHI window time
NO OCHIx	#10-2	= start with OCLO threshold
INEN0x ~ INEN1x	#11	= input enable control
PRS0x ~ PRS1x	#12	= pre scaler setting
OLOFF ENx	#13-1	= OL load in off state enable
OLLED ENx	#13-2	= OL LED mode enable
OLLED TRIG	#13-2	= trigger for OLLED detection in 100% d.c.
INCR SGN	#14	= PWM increment / decrement sign
INCR0x ~ INCR1x	#14	= PWM increment / decrement setting

#0

MUX2	MUX1	MUX0	CSNS
0	0	0	off
0	0	1	OUT1 current
0	1	0	OUT2 current
0	1	1	OUT3 current
1	0	0	OUT4 current
1	0	1	OUT5 current
1	1	0	VBAT monitor
1	1	1	control die temp.monitor

#0

SYNC EN1	SYNC EN0	Sync status
0	0	sync off
0	1	valid
1	0	trig0
1	1	trig1/2

#2~#7

PH 1x	PH 0x	Phase
0	0	0°
0	1	90°
1	0	180°
1	1	270°

#11

ONx	INEN1x	INEN0x	GPWM ENx	INx=0 OUTx	INx=0 PWMx	INx=1 OUTx	INx=1 PWMx
0	x	x	x	OFF	x	OFF	x
1	0	0	0	ON	individual	ON	individual
			1	ON	global	ON	global
	0	1	0	OFF	individual	ON	individual
			1	OFF	global	ON	global
	1	0	0	OFF	individual	ON	individual
			1	OFF	global	ON	global
	1	1	0	ON	individual	ON	global
			1	ON	global	ON	individual

#12

PRS 1x	PRS 0x	PRS divider	
0	0	/4	25Hz 100Hz
0	1	/2	50Hz 200Hz
1	x	/1	100Hz 400Hz

#14

INCR SGN	increment/decrement
0	decrement
1	increment

#14

INCR 1x	INCR 0x	increment/decrement
0	0	no increment/decrement
0	1	4 LSB
1	0	8 LSB
1	1	16 LSB

Figure 9. SPI input register

9.6.3 SPI output register and bit descriptions

The first nibble of the 16-bit data word (D12… D15) serves as address bits. All register values are logic [0] after a reset, except DSF and RCF bits. The predefined value is off/inactive unless otherwise noted.

Register	SO address					SO data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
not used*	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
quick status	1	0	0	0	1	FM	DSF	OVLF	OLF	CPF	RCF	CLKF	QSF5	QSF4	QSF3	QSF2	QSF1
CH1 status	2	0	0	1	0	FM	DSF	OVLF	OLF	X	OTS1	OTW1	OC21	OC11	OC01	OLON1	OLOFF1
CH2 status	3	0	0	1	1	FM	DSF	OVLF	OLF	X	OTS2	OTW2	OC22	OC12	OC02	OLON2	OLOFF2
CH3 status	4	0	1	0	0	FM	DSF	OVLF	OLF	X	OTS3	OTW3	OC23	OC13	OC03	OLON3	OLOFF3
CH4 status	5	0	1	0	1	FM	DSF	OVLF	OLF	X	OTS4	OTW4	OC24	OC14	OC04	OLON4	OLOFF4
CH5 status	6	0	1	1	0	FM	DSF	OVLF	OLF	X	OTS5	OTW5	OC25	OC15	OC05	OLON5	OLOFF5
device status	7	0	1	1	1	FM	DSF	OVLF	OLF	X	X	X	X	OVF	UVF	SPIF	ILIMP
I/O status	8	1	0	0	0	FM	DSF	TOGGLE	IIN4	IIN3	IIN2	IIN1	OUT5	OUT4	OUT3	OUT2	OUT1

* SOA address #0 shall be mapped to register #1, referred to R23442

QSFx	#1	= quick status (OC or OTW or OTS or OLON or OLOFF)
CLKF	#1	= PWM clock fail flag
RCF	#1	= registers clear flag
CPF	#1	= charge pump flag
OLF	#1~#7	= open load flag (wired or of all OL signals)
OVLF	#1~#7	= over load flag (wired or of all OC and OTS signals)
DSF	#1~#7	= device status flag (RCF or UVF or OVF or CPF or CLKF or TMF)
FM	#1~#8	= fail mode flag
OLOFFx	#2~#6	= open load in off state status bit
OLONx	#2~#6	= open load in on state status bit
OTWx	#2~#6	= overtemperature warning bit
OTSx	#2~#6	= overtemperature shutdown bit
ILIMP	#7	= limp input pin status
SPIF	#7	= SPI fail flag
UVF	#7	= undervoltage flag
OVF	#7	= overvoltage flag
TMF	#7	= testmode activation flag
OUTx	#8	= status of VBAT/2 comparator (reported in real time)
IINx	#8	= status of IINx signal (reported in real time)
TOGGLE	#8	= status of INx_ON signals (IN1_ON or IN2_ON or IN3_ON or IN4_ON)
DEVID0 ~ DEVID2	#9	= device type
DEVID3 ~ DEVID4	#9	= device family
DEVID5 ~ DEVID7	#9	= design status (incremented number)

#2~#6	OC2x	OC1x	OC0x	overcurrent status
	0	0	0	no overcurrent
	0	0	1	OCHI1
	0	1	0	OCHI2
	0	1	1	OCHI3
	1	0	0	OCLO
	1	0	1	OCHIOD
	1	1	0	SSC
	1	1	1	not used

Figure 10. SPI output register

9.6.4 Timing diagrams

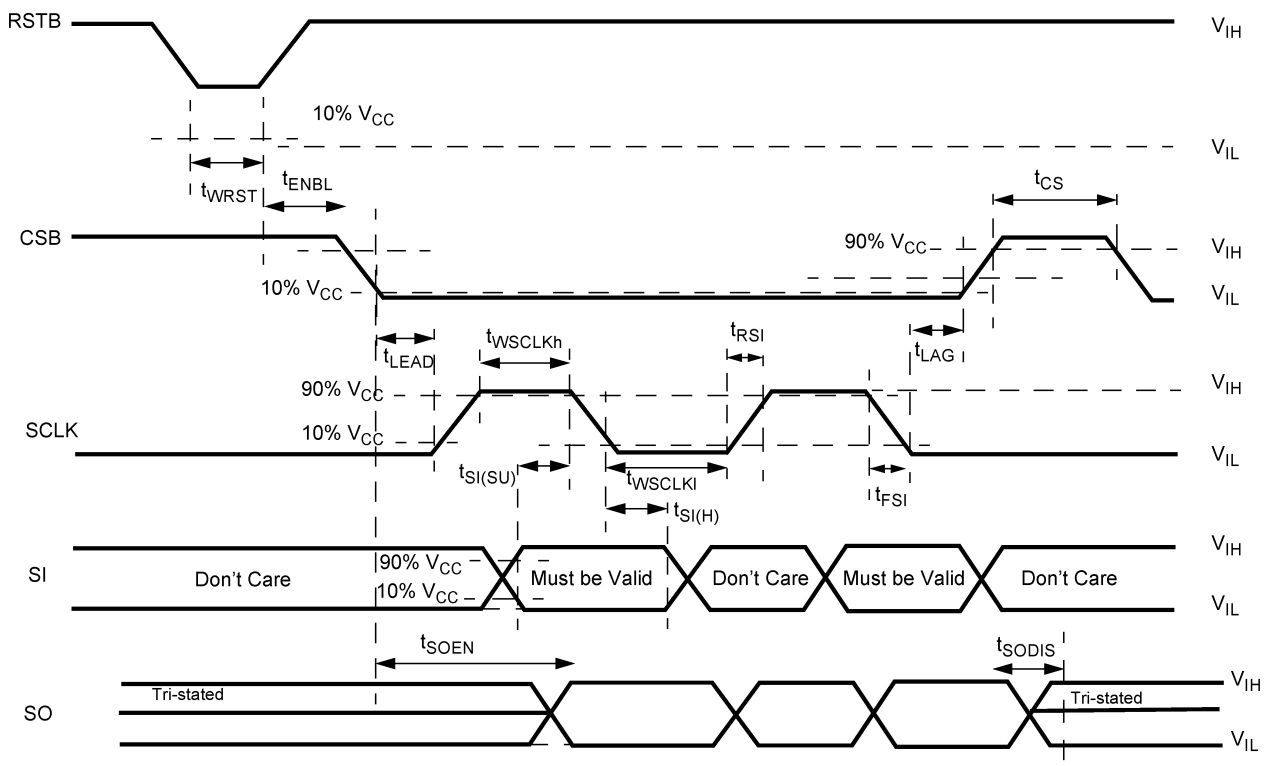


Figure 11. Timing requirements during SPI communication

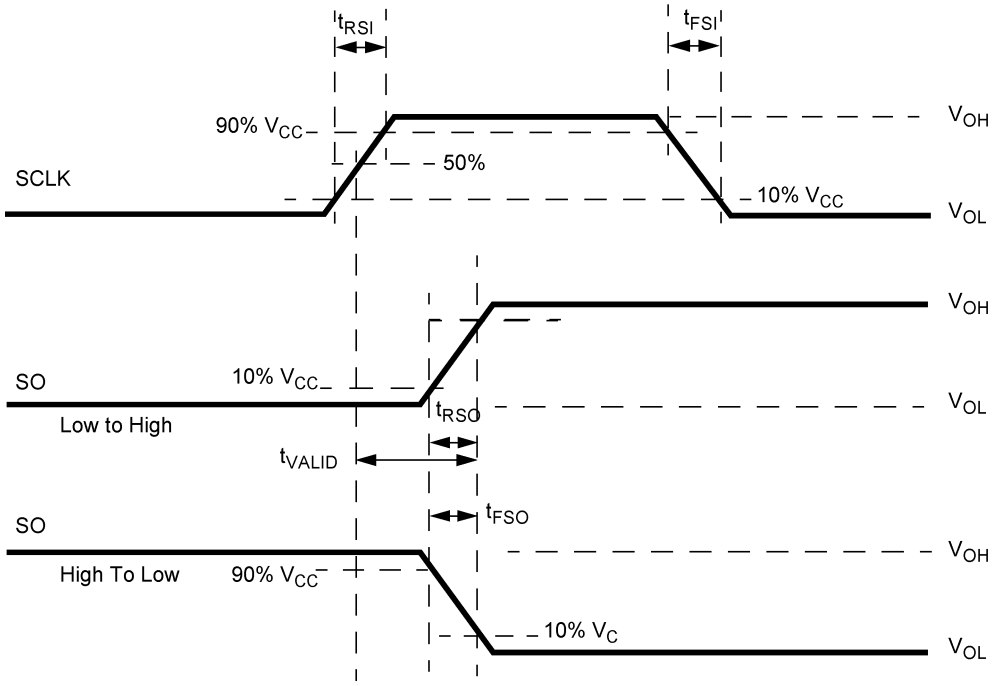


Figure 12. Timing diagram for serial output (SO) data communication

9.6.5 Electrical characterization

Table 8. Electrical characteristics

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, –40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
SPI SIGNALS CSB, SI, SO, SCLK, SO					
f_{SPI}	SPI clock frequency	0.5	—	5.0	MHz
V_{IH}	Logic input high state level (SI, SCLK, CSB, RSTB)	3.5	—	—	V
$V_{IH(WAKE)}$	Logic input high state level for wake-up (RSTB)	3.75	—	—	V
V_{IL}	Logic input low state level (SI, SCLK, CSB, RSTB)	—	—	0.85	V
V_{OH}	Logic output high state level (SO)	VCC – 0.4	—	—	V
V_{OL}	Logic output low state level (SO)	—	—	0.4	V
I_{IN}	Logic input leakage current in inactive state (SI = SCLK = RSTB = [0] and CSB = [1])	-0.5	—	+0.5	µA
I_{OUT}	Logic output tri-state leakage current (SO from 0 V to V_{CC})	-10	—	+1.0	µA
R_{PULL}	Logic input pull-up/pull-down resistor	25	—	100	kΩ
$R_{PULL-CSB}$	Logic pull-up resistor for CSB	25	—	130	kΩ
C_{IN}	Logic input capacitance [1]	—	—	20	pF
t_{RST_DGL}	RSTB deglitch time	7.5	10	12.5	µs

Symbol	Characteristic	Min	Typ	Max	Unit
t_{SO}	SO rising and falling edges with 80 pF	—	—	20	ns
t_{WCLKh}	Required high state duration of SCLK (required setup time)	80	—	—	ns
t_{WCLKl}	Required low state duration of SCLK (required setup time)	80	—	—	ns
t_{CS}	Required duration from the rising to the falling edge of CSB (required setup time)	1.0	—	—	µs
t_{RST}	Required low state duration for reset RST	1.0	—	—	µs
t_{LEAD}	Falling edge of CSB to rising edge of SCLK (required setup time)	320	—	—	ns
t_{LAG}	Falling edge of SCLK to rising edge of CSB (required setup lag time)	100	—	—	ns
$t_{SI(SU)}$	SI to falling edge of SCLK (required setup time)	20	—	—	ns
$t_{SI(H)}$	Falling edge of SCLK to SI (required hold time of the SI signal)	20	—	—	ns
t_{RSI}	SI, CSB, SCLK, max. rise time allowing operation at maximum f_{SPI}	—	20	50	ns
t_{FSI}	SI, CSB, SCLK, max. fall time allowing operation at maximum f_{SPI}	—	20	50	ns
$t_{SO(EN)}$	Time from falling edge of CSB to reach low-impedance on SO (access time)	—	—	—	ns
$t_{SO(DIS)}$	Time from rising edge of CSB to reach tri-state on SO	—	—	—	ns

[1] Parameter is derived from simulations.

10 Functional block requirements and behaviors

10.1 Self-protected high-side switches description and application information

10.1.1 Features

Up to five power outputs are foreseen to drive light as well as DC motor applications. The outputs are optimized for driving bulbs, HID ballasts, LEDs, and other resistive, capacitive, or low inductive loads. The smart switches are controlled by use of high sophisticated gate drivers. The gate drivers provide:

- output pulse shaping
- output protections
- active clamps
- output diagnostics

10.1.2 Output pulse shaping

The outputs are controlled with a closed loop active pulse shaping to provide the best compromise between:

- low switching losses
- low EMC emission performance
- minimum propagation delay time

Depending on the programming of the prescaler setting register #12-1, #12-2, the switching speeds of the outputs are adjusted to the output frequency range of each channel. The edge shaping must be designed according to the following table.

Divider factor	PWM freq. (Hz)		PWM period (ms)		D.C. range (hex)		D.C. range (LSB)		Min. on/ off duty cycle time (µs)
	min.	max.	min.	max.	min.	max.	min.	max.	
4	25	100	10	40	03	FB	4	252	156
2	50	200	5	20	07	F7	8	248	156
1	100	400	2.5	10	07	F7	8	248	78

The edge shaping provides full symmetry for rising and falling transition.

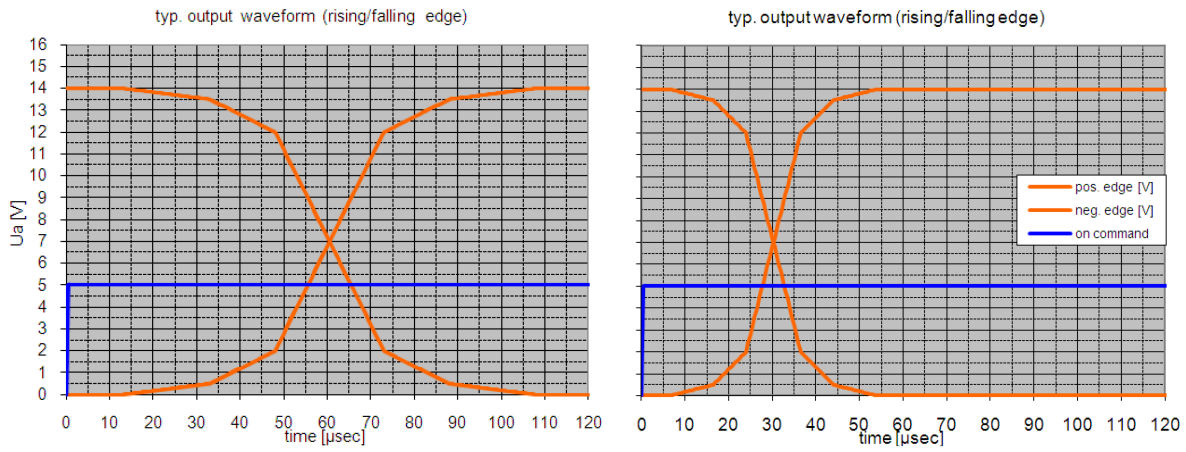


Figure 13. Typical power output switching (slow and fast slew rate)

10.1.2.1 SPI control and configuration

For optimized control of the outputs, a synchronous clock module is integrated. The PWM frequency and output timing during normal mode are generated from the clock input (CLK) by the integrated PWM module. In case of a clock fail (very low frequency, very high frequency), the output duty cycle is 100 %.

Each output (OUT1:OUT6) can be controlled by an individual channel control register.

Register	SI address					SI data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CHx control	2-7	channel address				WD	PH1x	PH0x	Onx	PWM7x	PWM6x	PWM5x	PWM4x	PWM3x	PWM2x	PWM1x	PWM0x

Where:

- PH0x… PH1x: phase assignment of the output channel x
- ONx: on/off control including overcurrent window control of the output channel x
- PWM0x… PWM7x: 8-bit PWM value individually for each output channel x

The ONx bits are duplicated in the output control register #8 to control the outputs with either the CHx control register or the output control register. The PRS1x… PRS0x prescaler settings can be set in the prescaler settings register #12-1 and #12-2.

The synchronization of the switching phases between different devices is provided by the PWM SYNC bit in the initialization 2 register #1.

On a SPI write into initialization 2 register (#1):

- initialization when the bit D1 (PWM SYNC) is logic[1], all counters of the PWM module are reset with the positive edge of the CSB, the phase synchronization is performed immediately within one SPI frame. It could help to synchronize different 32XSG devices in the board
- when the bit D1 is logic[0], no action is executed

The switching frequency can be adjusted for the corresponding channel as described in the following table:

CLK freq. (kHz)		prescaler setting		divider factor	PWN freq. (Hz)		slew rate	PWM resolution	
min.	max.	PRS1x	PRS0x		min.	max.		(Bit)	(steps)
25.6	102.4	0	0	4	25	100	slow	8	256
		0	1	2	50	200	slow		
		1	X	1	100	400	fast		

No PWM feature is provided in case of:

- fail mode
- clock input signal failure

10.1.2.2 Global PWM control

In addition to the individual PWM register, each channel can be assigned independently to a global PWM register. The setting is controlled by the GPWM EN bits inside the global PWM control register #9-1. When no control by direct input pin is enabled and the GPWM EN bit is:

- low (logic[0]), the output is assigned to individual PWM (default status)
- high (logic[1]), the output is assigned to global PWM

The PWM value of the global PWM channel is controlled by the global PWM control register #9-2.

When a channel is assigned to global PWM, the switching phase the prescaler and the pulse skipping are according the corresponding output channel setting.

Table 9. Global PWM Register

Register	SI address	SI data															
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Global PWM control	9-1	1	0	0	1	WD	0	X	X	X	X	GPWM EN6	GPWM EN5	GPWM EN4	GPWM EN3	GPWM EN2	GPWM EN1
	9-2	1	0	0	1	WD	1	X	X	GPWM 7	GPWM6	GPWM5	GPWM4	GPWM3	GPWM2	GPWM1	GPWM0

10.1.2.3 Incremental PWM control

To reduce the control overhead during soft start/stop of bulbs or DC motors (theatre dimming), an incremental PWM control feature is implemented. With the incremental

PWM control feature the PWM values of all internal channels OUT1:OUT5 can be incremented or decremented with one SPI frame.

The incremental PWM feature is not available for:

- the global PWM channel
- the external channel OUT6

The control is according the increment/decrement register #14:

- INCR SGN: sign of incremental dimming (valid for all channels)
- INCR 1x, INCR 0x increment/decrement

INCR SGN	Increment/decrement
0	decrement
1	increment

INCR 1x	INCR 0x	Increment/decrement
0	0	no increment/decrement
0	1	4
1	0	8
1	1	16

This feature limits the duty cycle to the rails (00 resp. FF) to avoid any overflow.

10.1.2.4 Input control

Up to four dedicated control inputs (IN1:IN4) are foreseen to:

- wake-up the device
- fully control the corresponding output in case of Fail mode
- control the corresponding output in case of Normal mode

The control during Normal mode is according the INEN0x and INEN1x bits in the input enable register #11 and according to the logic in Table 9. An input deglitcher is provided at each control input to avoid high frequency control of the outputs. The internal signal is called iINx.

As the input thresholds are logic level compatible, the input structure of the pin is able to withstand supply voltage levels (max. 40 V) without damage. External current limit resistors (1.0 kΩ, 10 kΩ) can be used to handle reverse current conditions. The inputs have an integrated pull-down resistor.

10.1.2.5 Electrical characterization

Table 10. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 30 V, –40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A= 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
POWER OUTPUTS OUT1:OUT5					

Symbol	Characteristic	Min	Typ	Max	Unit
$R_{DS(on)}$	ON-Resistance, Drain-to-Source for 7.0 mΩ power channel				
	T_J = 25 °C, V_{PWR} ≥ 24 V	—	7.0	—	mΩ
	T_J = 150 °C, V_{PWR} ≥ 24 V	—	—	12.9	
	T_J = 25 °C, V_{PWR} = –12 V	—	—	13	
	T_J = 150 °C, V_{PWR} = –12 V	—	—	18.2	
$R_{DS(on)}$	ON-Resistance, Drain-to-Source for 17 mΩ power channel				
	T_J = 25 °C, V_{PWR} ≥ 24 V	—	17	—	mΩ
	T_J = 150 °C, V_{PWR} ≥ 24 V	—	—	30.9	
	T_J = 25 °C, V_{PWR} = –12 V	—	—	31	
	T_J = 150 °C, V_{PWR} = –12 V	—	—	43.5	
$I_{LEAK\ SLEEP}$	Sleep mode output leakage current (Output shorted to GND) per channel				
	T_J = 25 °C, V_{PWR} = 24 V	—	—	0.5	µA
	T_J = 125 °C, V_{PWR} = 24 V	—	—	5.0	
	T_J = 25 °C, V_{PWR} = 35 V	—	—	5.0	
	T_J = 125 °C, V_{PWR} = 35 V	—	—	25	
$I_{OUT\ OFF}$	OFF operational output leakage current in OFF-state per channel				
	T_J = 25 °C, V_{PWR} = 30 V	—	—	10	µA
	T_J = 125 °C, V_{PWR} = 30 V	—	—	20	
δ_{PWM}	Output PWM duty cycle range (measured at V_{OUT} = $V_{PWR/2}$)				
	Low Frequency Range (25 to 100 Hz)	4.0	—	252	LSB
	Medium Frequency Range (50 to 200 Hz)	8.0	—	248	
	High Frequency Range (100 to 400 Hz)	8.0	—	248	
SR	Rising and falling edges slew rate at VPWR = 24 V (measured from VOUT = 2.5 V to VPWR – 2.5 V) [1]				
	Low Frequency Range	0.15	0.35	0.5	V/µs
	Medium Frequency Range	0.15	0.35	0.5	
	High Frequency Range	0.35	0.7	1.05	
ΔSR	Rising and falling edges slew rate matching at V_{PWR} = 24 V (SRr/ SRf) [1]	0.9	1.0	1.1	
t_{DLY}	Turn-on and turn-off delay time at V_{PWR} = 24 V [1]				
	Low frequency range	20	70	120	µs
	Medium frequency range	20	70	120	
	High frequency range	10	30	50	
Δt_{DLY}	Turn-on and turn-off delay time matching at V_{PWR} = 24 V [1]				
	Low frequency range	–20	0.0	20	µs
	Medium frequency range	–20	0.0	20	
	High frequency range	–10	0.0	10	
$t_{OUTPUT\ SD}$	Shutdown delay time in case of fault	0.5	2.5	4.5	µs
REFERENCE PWM CLOCK					

Symbol	Characteristic	Min	Typ	Max	Unit
f_{CLK}	Clock input frequency range	25.6	—	102.4	kHz

[1] With nominal resistive load: 2.5 Ω and 5.0 Ω respectively for 7.0 mΩ and 17 mΩ channel.

10.1.3 Output protections

The power outputs are protected against fault conditions in Normal and Fail mode in case of:

- overload conditions
- harness short-circuit
- overcurrent and severe short-circuit
- overtemperature including overtemperature warning
- under and overvoltage
- charge pump failure
- reverse polarity

In case a fault condition is detected, the corresponding output is commanded off immediately after the deglitch time $t_{FAULT\ SD}$. The turn off in case of a fault shutdown (OCHI1, OCHI2, OCHI3, OCLO, OTS, UV, CPF, OLOFF) is provided by the FTO feature (fast turn off). The FTO:

- does not use edge shaping
- is provided with high slew rate to minimize the output turn-off time $t_{OUTPUT\ SD}$, in regards to the detected fault
- uses a latch which keeps the FTO active during an undervoltage condition ($0 \le V_{PWR} \le V_{PWR\ UVF}$)

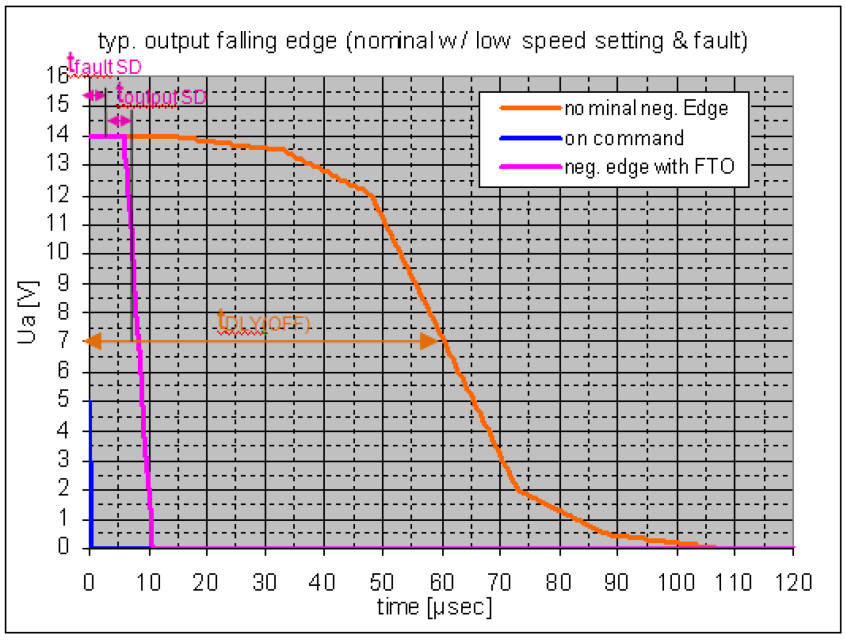


Figure 14. Power output switching in nominal operation and in case of fault

In case of a fault condition during Normal mode:

- the status is reported in the quick status register #1 and the corresponding channel status register #2:#6.

To restart the output:

- the channel must be restarted by writing the corresponding ON bit in the channel control register #2:#6 or output control register #8

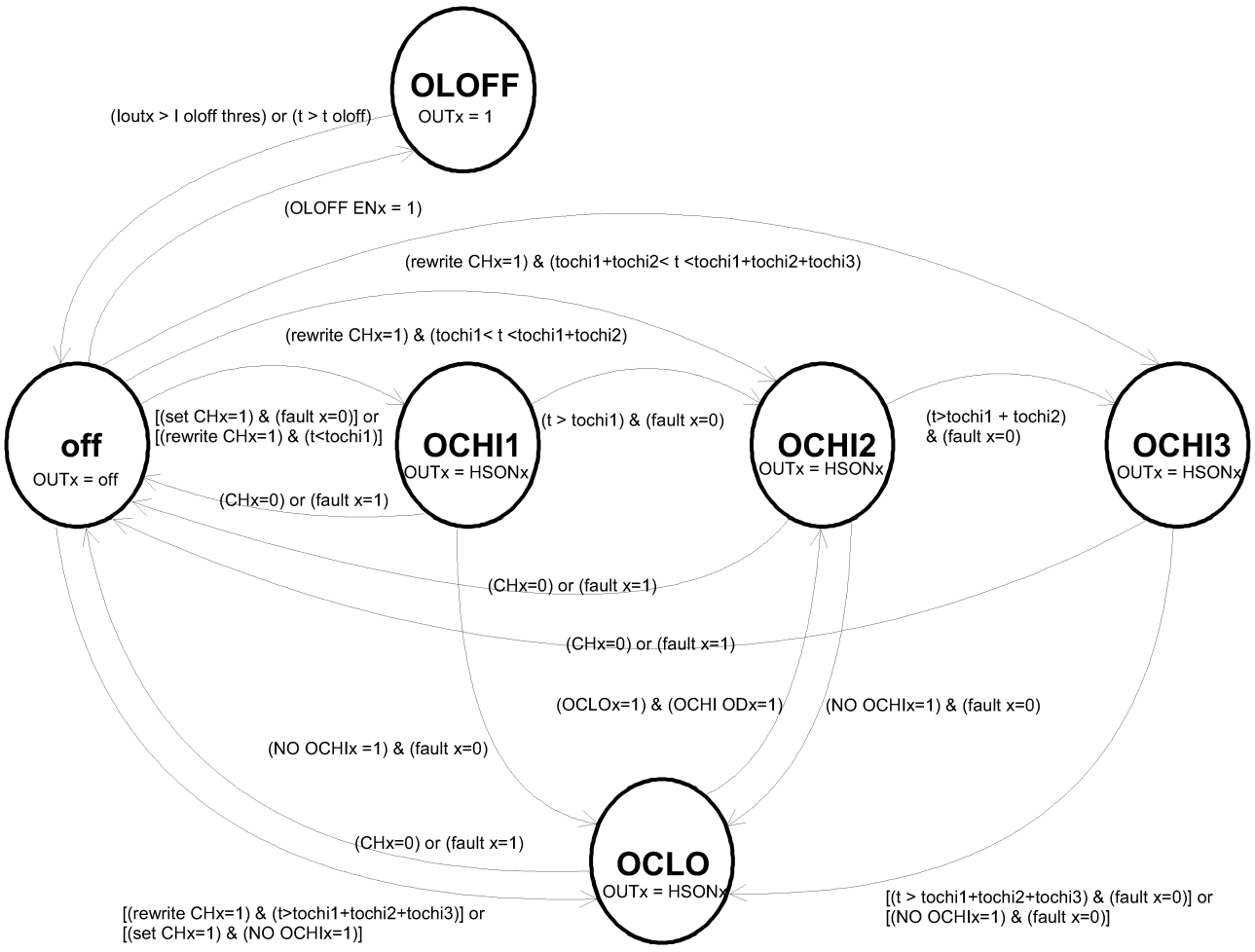


Figure 15. Output control diagram in Normal mode

Fail mode

If an overcurrent (OCHI2, OCHI3, OCLO) or undervoltage is detected, the restart is controlled by the autorestart feature.

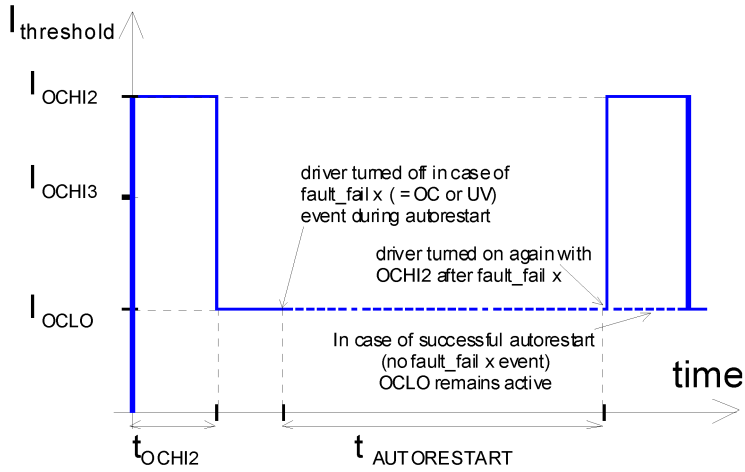


Figure 16. Autorestart in Fail mode

During overtemperature (OTSx), severe short-circuit (SSCx), or OCHI1 overcurrent, the corresponding output enters the latch off state until the next wake-up cycle or mode change.

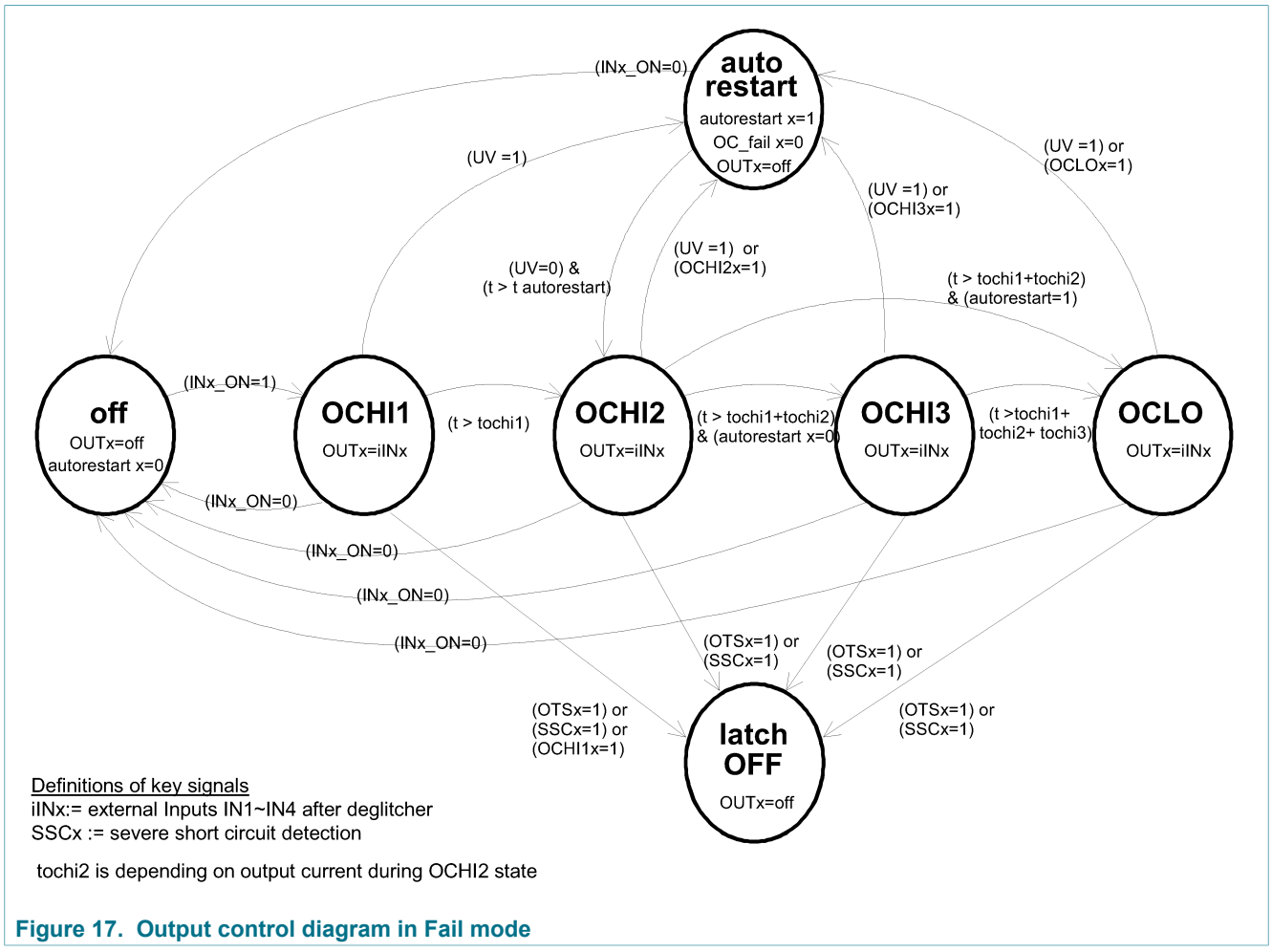


Figure 17. Output control diagram in Fail mode

10.1.3.1 Overcurrent protections

Each output channel is protected against overload conditions by use of a multilevel overcurrent shutdown.

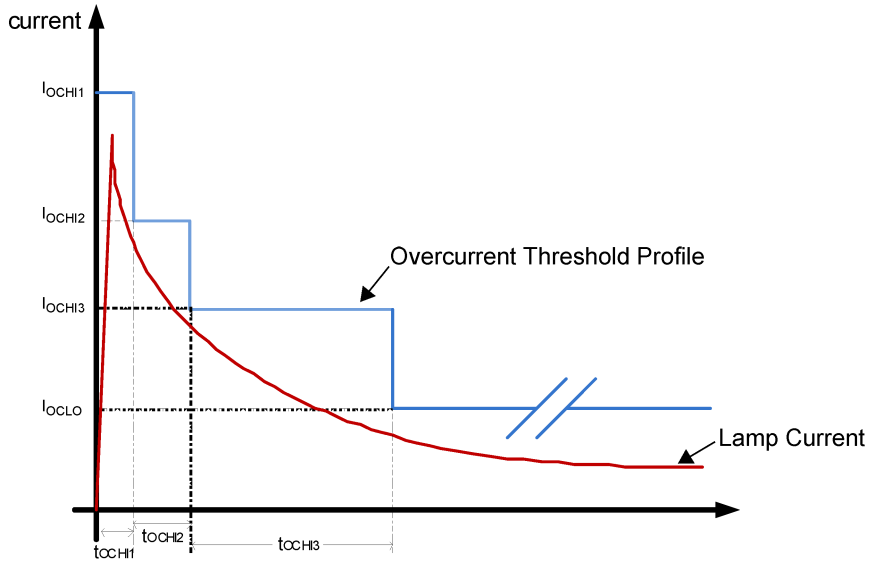


Figure 18. Transient overcurrent profile

The current thresholds and the threshold window times are fixed for each type of power channel. When the output is in PWM mode, these timings (tOCHI1:tOCHI3) are accumulated at each On state period of the output.

In addition, a severe short-circuit protection (SSC) is implemented to limit the power dissipation in Normal and Fail modes, in case of severe short-circuit event. This feature is active only for a very short period of time, during OFF-to-ON transition. The load impedance is monitored during the output turn-on. Each of the previously listed faults are reported in the corresponding channel status register #2…#6, as shown in Table 11.

Table 11. Channel status register #2…#6

OC2x	OC1x	OC0x	Overcurrent status
0	0	0	no overcurrent
0	0	1	OCHI1
0	1	0	OCHI2
0	1	1	OCHI3
1	0	0	OCLO
1	0	1	OCHIOD
1	1	0	SSC
1	1	1	not used

Normal mode

The enabling of the high current window (OCHI1:OCHI3) is dependent on CHx signal. When no control input pin is enabled, the control of the overcurrent window depends on

the ON bits inside channel control registers #2:#7 or the output control register #8. When the corresponding CHx signal is:

- toggled (turn OFF and then ON), the OCHI window counter resets and the full OCHI windows is applied
- rewritten (logic [1]), the OCHI window time is proceeding without reset of the OCHI counter

Fail mode

The enabling of the high current window (OCHI1:OCHI3) is dependent on INx_ON toggle signal. The enabling of output (OUT1:5) is dependent on CHx signal.

10.1.3.2 Overcurrent control programming

OCHI On Demand (OCHI OD)

In some instances, a lamp might be de-powered when its supply is interrupted by the opening of a switch (as in a door), or by disconnecting the load (as for a supply dock). In these cases, the driver should be tolerant of the inrush current occurring when the load is reconnected and the channel is already ON. The OCHI On Demand feature allows such control individually for each channel through the OCHI ODx bits inside the Initialization #2 register. When the OCHI ODx bit is:

- low (logic[0]), the channel operates in its Normal, Default mode. After end of OCHI window timeout the output is protected with an OCLO threshold
- high (logic[1]), the channel operates in the OCHI On Demand mode and uses the OCHI2 and OCHI3 windows and times after an OCLO event (when horizontal current threshold OCLO is crossed, a new window with OCHI2&3 is started)

To reset the OCHI ODx bit (logic[0]) and change the response of the channel, first change the bit in the Initialization #2 register and then turn the channel off. The OCHI ODx bit is also reset after an overcurrent event at the corresponding output. The fault detection status is reported in the quick status register #1 and the corresponding channel status registers #2:#6.

OCLO Threshold Setting

The static overcurrent threshold can be programmed individually for each output in two levels to adapt low duty cycle dimming and a variety of loads. The CSNS recopy factor and OCLO threshold depend on OCLO and ACM settings. The OCLO setting is controlled by the OCLOx bits inside the overcurrent control register #10-1. When the OCLOx bit is:

- low (logic[0]), the output is protected with the higher OCLO threshold (default status and during Fail mode)
- high (logic[1]), the lower OCLO threshold is applied

Short OCHI

The length of the OCHI windows can be shortened by a factor of 2, to accelerate the availability of the CSNS diagnosis and to reduce the potential stress inside the switch during an overload condition. The setting is controlled individually for each output by the SHORT OCHIx bits inside the overload control register #10-2. When the SHORT OCHIx bit is:

- low (logic[0]), the default OCHI window times are applied (default status and during Fail mode)

- high (logic[1]), the short OCHI window times are applied (50 % of the regular OCHI window time)

NO OCHI

Depending on the type of load in the output, the OCHI windows can be suppressed with the NO OCHI feature. In that case, the output is protected with OCLO protection right after the turn On and CSNS reporting is directly available. The switch on process of an output can be done without an OCHI window, to accelerate the availability of the CSNS diagnosis. The setting is controlled individually for each channel by the NO OCHIx bits inside the overcurrent control register #10-2. When the NO OCHIx bit is:

- low (logic[0]), the regular OCHI window is applied (default status and during Fail mode)
- high (logic[1]), the turn on of the output is provided without OCHI windows

Thermal OCHI

To minimize the electro-thermal stress inside the device in case of a short-circuit, the OCHI1 level can be automatically adjusted in regards to the control die temperature. The functionality is controlled for all channels by the OCHI THERMAL bit inside the initialization 2.

When the OCHI THERMAL bit is:

- low (logic[0]), the output is protected with default OCHI1 level
- high (logic[1]), the output is protected with the OCHI1 level reduced by $R_{THERMAL\ OCHI}$ = 15 % (typ) when the control die temperature is above $T_{THERMAL\ OCHI}$ = 63 °C (typ.)

10.1.3.3 Electrical characterization

Table 12. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 30 V, –40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A= 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
POWER OUTPUTS OUT1:OUT5					
I_{OCHI1}	High overcurrent level 1 for 7.0 mΩ power channel	76	84	93	A
I_{OCHI2}	High overcurrent level 2 for 7.0 mΩ power channel	38	46	62	A
I_{OCHI3}	High overcurrent Level 3 for 7.0 mΩ power channel	26	31	35.5	A
I_{OCLO}	Low overcurrent for 7.0 mΩ power channel High level Low level	 17.6 8.8	 21.9 10.8	 26.4 13.2	A
$I_{OCLO\ ACM}$	Low overcurrent for 7.0 mΩ power channel in ACM mode High level Low level	 8.8 4.4	 10.8 5.5	 13.2 6.6	A
I_{OCHI1}	High overcurrent level 1 for 17 mΩ power channel	32	38	44	A
I_{OCHI2}	High overcurrent Level 2 for 17 mΩ power channel	18.5	22.5	26.5	A
I_{OCHI3}	High overcurrent Level 3 for 17 mΩ power channel	11.0	13.5	15.7	A
I_{OCLO}	Low overcurrent for 17 mΩ power channel High level Low level	 8.8 4.4	 10.8 5.5	 13.2 6.6	A

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{OCLO\ ACM}$	Low overcurrent for 17 mΩ power channel in ACM mode High level Low level	 4.4 2.2	 5.5 2.6	 6.6 3.3	 A
$R_{THERMAL\ OCHI}$	High overcurrent ratio 2	0.835	0.85	0.865	
$T_{THERMAL\ OCHI}$	Temperature threshold for IOCHI1 level adjustment	50	63	70	°C
t_{OCHI1}	High overcurrent time 1 Default value Short OCHI option	 1.5 0.75	 2.0 1.0	 2.5 1.25	 ms
t_{OCHI2}	High overcurrent time 2 Default value Short OCHI option	 6.0 3.0	 8.0 4.0	 10 5.0	 ms
t_{OCHI3}	High overcurrent time 3 Default value Short OCHI option	 48 24	 64 32	 80 40	 ms
$t_{FAULT\ SD}$	Fault deglitch time [1] OCLO and OCHI OD OCHI1:3 and SSC	 1.0 1.0	 2.0 2.0	 3.0 3.0	 µs
$t_{AUTO\ RESTART}$	Fault autorestart time in Fail mode	48	64	80	ms
$t_{BLANKING}$	Fault blanking time after wake-up	—	50	100	µs

[1] Guaranteed by test mode.

10.1.3.4 Overtemperature protection

A dedicated temperature sensor is located on each power transistor, to protect the transistors and provide SPI status monitoring. The protection is based on a two stage strategy. When the temperature at the sensor exceeds the:

- selectable overtemperature warning threshold (T_{OTW1}, T_{OTW2}), the output stays on and the event is reported in the SPI
- overtemperature threshold (T_{OTS}), the output is switched off immediately after the deglitch time $t_{FAULT\ SD}$ and the event is reported in the SPI after the deglitch time $t_{FAULT\ SD}$

10.1.3.4.1 Overtemperature warning (OTW)

In case of an overtemperature warning:

- the output remains in current state
- the status is reported in the quick status register #1 and the corresponding channel status register #2:#6

The OTW threshold can be selected by the OTW SEL bit inside the initialization 2 register #1. When the bit is:

- low (logic[0]), the high overtemperature threshold is enabled (default status)
- high (logic[1]), the low overtemperature threshold is enabled

To delatch the OTW bit (OTWx):

- the temperature has to drop below the corresponding overtemperature warning threshold
- a read command of the corresponding channel status register #2:#6 must be performed

10.1.3.4.2 Overtemperature shutdown (OTS)

During an overtemperature shutdown:

- the corresponding output is disabled immediately after the deglitch time $t_{FAULT\ SD}$
- the status is reported after $t_{FAULT\ SD}$ in the quick status register #1 and the corresponding channel status register #2:#6

To restart the output after an overtemperature shutdown event in Normal mode:

- the overtemperature condition must be removed, and the channel must be restarted by a write command of the ON bit in the corresponding channel control register #2:#6, or in the output control register #8

To delatch the diagnosis:

- the overtemperature condition must be removed
- a read command of the corresponding channel status register #2:#6 must be performed

To restart the output after an overtemperature shutdown event in Fail mode:

- a mode transition is needed. Refer to Section 9.5.5 "Mode transitions"

10.1.3.4.3 Electrical characterization

Table 13. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 30 V, –40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
POWER OUTPUTS OUT1:OUT5					
T_{OW}	Overtemperature warning [1]				
	T_{OW1} level	100	115	130	°C
	T_{OW2} level	120	135	150	
T_{OTS}	Overtemperature shutdown [1]	155	170	185	°C
$t_{FAULT\ SD}$	Fault deglitch time				
	OTS	2.0	5.0	10	µs

[1] Guaranteed by test mode.

10.1.3.5 Undervoltage and overvoltage protections

10.1.3.5.1 Undervoltage

During an undervoltage condition ($V_{PWRPOR} \leq V_{PWR} \leq V_{PWR\ UVF}$), all outputs (OUT1:OUT5) are switched off immediately after deglitch time $t_{FAULT\ SD}$. The undervoltage condition is reported after the deglitch time $t_{FAULT\ SD}$:

- in the device status flag (DSF) in the registers #1:#7
- in the undervoltage flag (UVF) inside the device status register #7

Normal mode

The reactivation of the outputs is controlled by the microcontroller. To restart, the output the undervoltage condition must be removed and:

- a write command of the ON Bit must be performed in the corresponding channel control register #2:#6 or in the output control register #8

To delatch the diagnosis:

- the undervoltage condition must be removed
- a read command of the device status register #7 must be performed

Fail mode

When the device is in Fail mode, the restart of the outputs is controlled by the autorestart feature.

10.1.3.5.2 Overvoltage

The overvoltage condition ($V_{PWR} \geq V_{PWR\ OVF}$) is reported in the:

- device status flag (DSF) in the registers #1:#7
- overvoltage flag (OVF) inside the device status register #7

To delatch the diagnosis:

- the overvoltage condition must be removed
- a read command of the device status register #7 must be performed

During an overvoltage ($V_{PWR} \geq V_{PWR\ OVF}$), the output stays in the ON state.

10.1.3.5.3 Electrical characterization

Table 14. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 30 V, –40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
SUPPLY VPWR					
$V_{PWR\ UVF}$	Supply undervoltage	5.0	5.25	5.5	V
$V_{PWR\ UVF\ HYS}$	Supply undervoltage hysteresis	200	350	550	mV
$V_{PWR\ OVF}$	Supply overvoltage	32	33.5	35	V
$V_{PWR\ OVF\ HYS}$	Supply overvoltage hysteresis	0.5	1.0	1.5	V
$V_{PWR\ HIGH}$	Maximum supply voltage for short-circuit protection	32	—	—	V

Symbol	Characteristic	Min	Typ	Max	Unit
$t_{FAULT\ SD}$	Fault deglitch time UV and OV	2.0	3.5	6.0	µs

10.1.3.6 Charge pump protection

The charge pump voltage is monitored in order to protect the smart switches in case of:

- power up
- failure of external capacitor
- failure of charge pump circuitry

When a charge pump failure occurs, output control is no longer possible, and the status reports after $t_{FAULT\ SD}$ in the register Quick status #1 bit D7 (CPF flag) and on all output registers #1…#7 (DSF flag).

To delatch the diagnosis:

- the charge pump failure condition must be removed
- a read command of the quick status register #1 is necessary

10.1.3.6.1 Electrical characterization

Table 15. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 30 V, –40 °C ≤ T_A ≤ 125 °C, GND =0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
CHARGE PUMP CP					
C_{CP}	Charge pump capacitor range (Ceramic type X7R)	47	—	220	nF
$V_{CP\ MAX}$	Maximum charge pump voltage	—	—	16	V
$t_{FAULT\ SD}$	Fault deglitch time CPF	—	4.0	6.0	µs

10.1.3.6.2 Reverse supply protection

The device is protected against reverse polarity of the V_{PWR} line. In reverse polarity condition:

- the output transistors OUT1:5 are turned ON in order to prevent the device from thermal overload
- the OUT6 pin is pulled down to GND. An external current limit resistor must be added in series with OUT6 pin
- no output protection is available in this condition

10.1.4 Digital diagnostics

The device offers several modes for load status detection in on state and off state through the SPI.

10.1.4.1 Openload detections

The device provides smart diagnostics for openload conditions: These diagnostics are provided for each power output (OUT1…5), based on the current monitoring circuit.

Openload detection is reported:

- for the corresponding OUTx on the QSFx bit in the quick status register #1.
- In the global openload flag OLF (register #1…#7)
- In the OLON or OLOFF bit in the corresponding channel status register (#2…#6)
- For LED loads type with the OLLED feature (OLLED control register #13-2)

Openload detection is provided for the following output configuration:

10.1.4.1.1 Output is in the ON state

OLON flag is reported on the bit D1 of the corresponding channel status register if the output current is below the following threshold:

- IOL threshold if the corresponding OLLED EN bit is low (register #13-2)
- IOLLED threshold if the corresponding OLLED EN bit is high

When openload detection in LED mode is enabled (OLLED ENx=1), the output current is checked differently, depending on the output operation:

- When the output is fully On (100 % PWM), the comparison with IOLLED threshold is done by user's demand by setting OLLED TRIG=1 on bit D5 of register OLLED control (#13-2)

When the output is in PWM operation, the comparison with IOLLED threshold is done at each Turn Off phase of each PWM cycle.

- In PWM operation, the OLON diagnosis available within $\delta_{PWM\ OLON}$ duty cycle range.

10.1.4.1.2 Output is in the OFF state

OLOFF flag is reported on the bit D0 of the corresponding channel status register if the output current is below IOLOFF threshold. Openload OFF diagnostic is reported on at the user's demand by setting the bit OLOFF ENx of the corresponding output to high (logic[1]). Once the OLOFF ENx is set high, the corresponding output turns ON during t_{OLOFF} and the output current is compared to I_{OLOFF}:

- If the output current goes above IOLOFF within the t_{OLOFF} period, the output is turned back to the Off state and a logic [0] is reported on the OLOFFx bit of CHx status register #2…#6
- If the output current is below IOLOFF within the t_{OLOFF} period, a logic [1] is reported on the OLOFFx bit of CHx status register #2…#6. The output is turned OFF at the end of the t_{OLOFF} period.

To delatch the diagnosis, the openload condition must be removed and a read command of the corresponding channel status register #2…#6 must be read.

10.1.4.1.3 Electrical characterization

Table 16. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 30 V, –40 °C ≤ T_A ≤ 125 °C, GND =0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
POWER OUTPUTS OUT1…OUT5					
I_{OL}	Openload current threshold in ON state 7.0 mΩ power channel 17 mΩ power channel	 50 30	 200 100	 350 160	mA
$\delta_{PWM\ OLON}$	Output PWM duty cycle range for openload detection in ON state Low frequency range (25 to 100 Hz) Medium frequency range (100 to 200 Hz) High frequency range (200 to 400 Hz)	 18 18 17	 — — —	 — — —	LSB
I_{OLLED}	Openload current threshold in ON state/OLLED mode	2.0	4.0	5.0	mA
t_{OLOFF}	Openload detection time in OFF state	0.9	1.2	1.5	ms
I_{OLOFF}	Openload current threshold in OFF state 7.0 mΩ power channel 17 mΩ power channel	 0.77 0.385	 1.1 0.55	 1.43 0.715	A

10.1.4.2 Output shorted to V_{PWR} in OFF state

A short to VPWR detection during OFF state is provided individually for each power output OUT1…OUT5, based on an output voltage comparator referenced to V_{PWR}/2 (VOUT DETECT) and an external pull-down circuitry. The detection result is reported in the OUTx bits of the I/O status register #8 in real time. In case of UVF, the OUTx bits are undefined.

10.1.4.2.1 Electrical characterization

Table 17. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 30 V, –40 °C ≤ T_A ≤ 125 °C, GND =0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
POWER OUTPUTS OUT1…OUT5					
$V_{OUTDETECT}$	Output voltage comparator threshold	0.42	0.5	0.58	V_{PWR}

10.1.4.3 SPI fault reporting

Protection and monitoring of the outputs during normal mode is provided by digital switch diagnosis via the SPI. The selection of the SO data word is controlled by the SOA0… SOA3 bits inside the initialization 1 register #0. By default the quick status register #1 is returned during write access on the SPI. SOA0…SOA3 selects the output register the user wants to read. The 'quick status register' #1 provides one glance failure overview. As long as no failure flag is set (logic[1]), no action by the microcontroller is needed.

Register	SO address	SO data														
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
quick address	1	0	0	0	1	FM	DSF	OVLF	OLF	CPF	RCF	CLKF	QSF5	QSF4	QSF3	QSF2	QSF1

- FM: Fail mode indication. This bit is also present in all other SO data words, and indicates the fail mode by a logic[1]. When the device is in Normal mode, the bit is logic[0]
- global device status flags (D10:D8): These flags are also present in the channel status registers #2:#6, the device status register #7, and are cleared when all fault bits are cleared by reading the registers #2:#7
- DSF: device status flag (RCF, or UVF, or OVF, or CPF, or CLKF, or TMF). UVF and TMF are also reported in the device status register #7
- OVLF: over load flag (wired OR of all OC and OTS signals)
- OLF: openload flag
- CPF: charge pump flag
- RCF: registers clear flag: this flag is set (logic[1]) when all SI and SO registers are reset
- CLKF: clock fail flag. Refer to Section 10.3.3.2 "Logic I/O plausibility check"
- QSF1:QSF5: channel quick status flags (QSFx = OC0x, or OC1x, or OC2x, or OTWx, or OTSx, or OLONx, or OLOFFx)

The SOA address #0 is also mapped to register #1 (D15…D12 bits report logic [0001]). When a fault condition is indicated by one of the quick status bits (QSF1…QSF5, OVLF, OLF), the detailed status can be evaluated by reading of the corresponding channel status registers #2…#6.

Register	SO address					SO data										
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CH1 status	2	0	0	1	0	FM	DSF	OVLF	OLF	res	OTS1	OTW1	OC21	OC11	OC01	OLON1	OLOFF1
CH2 status	3	0	0	1	1	FM	DSF	OVLF	OLF	res	OTS2	OTW2	OC22	OC12	OC02	OLON2	OLOFF2
CH3 status	4	0	1	0	0	FM	DSF	OVLF	OLF	res	OTS3	OTW3	OC23	OC13	OC03	OLON3	OLOFF3
CH4 status	5	0	1	0	1	FM	DSF	OVLF	OLF	res	OTS4	OTW4	OC24	OC14	OC04	OLON4	OLOFF4
CH5 status	6	0	1	1	0	FM	DSF	OVLF	OLF	res	OTS5	OTW5	OC25	OC15	OC05	OLON5	OLOFF5

- OTSx: overtemperature shutdown flag
- OTWx: overtemperature warning flag
- OC0x…OC2x: overcurrent status flags
- OLONx: openload in ON state flag
- OLOFFx: openload in OFF state flag

The most recent OC fault is reported by the OC0x…OC2x bits, if a new OC occurs before an old OC on the same output read. When a fault condition is indicated by one of the global status bits (FM, DSF), the detailed status can be evaluated by reading of the device status registers #7:

Register	SO address	SO data														
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
device status	7	0	1	1	1	FM	DSF	OVLF	OLF	res	res	res	TMF	OVF	UVF	SPIF	iLMP

- TMF: test mode activation flag. Test mode is used for manufacturing testing only. If this bit is set to logic [1], the MCU must reset the device

- OVF: overvoltage flag
- UVF: undervoltage flag
- SPIF: SPI fail flag
- iLIMP: real time reporting after the t_{IN_DGL}, not latched

The I/O status register #8 can be used for system test, fail mode test and the power down procedure:

Register	SO address	SO data															
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
I/O status	8	1	0	0	0	FM	res	TOGGLE	iIN4	iIN3	iIN2	iIN1	OUT5	OUT4	OUT3	OUT2	OUT1

The register provides the status of the control inputs, the toggle signal, and the power outputs state in real time (not latched).

- TOGGLE: status of the 4 input toggle signals (IN1_ON, or IN2_ON, or IN3_ON, or IN4_ON), reported in real time
- iINx: status of iINx signal (real time reporting after the tIN_DGL, not latched)
- OUTx: status of output pins OUTx (the detection threshold is $V_{PWR/2}$) when undervoltage condition does not occur

10.1.5 Analog diagnostics

The analog feedback circuit (CSNS) is implemented to provide load and device diagnostics during Normal mode. During Fail and Sleep modes, the analog feedback is not available. The routing of the integrated multiplexer is controlled by MUX0:MUX2 bits inside the initialization 1 register #0.

10.1.5.1 Output current monitoring

The current sense monitor provides a current proportional to the current of the selected output (OUT1…OUT5). CSNS output delivers 1.0 mA full scale range current source reporting channel 1…5 current feedback (IFSR).

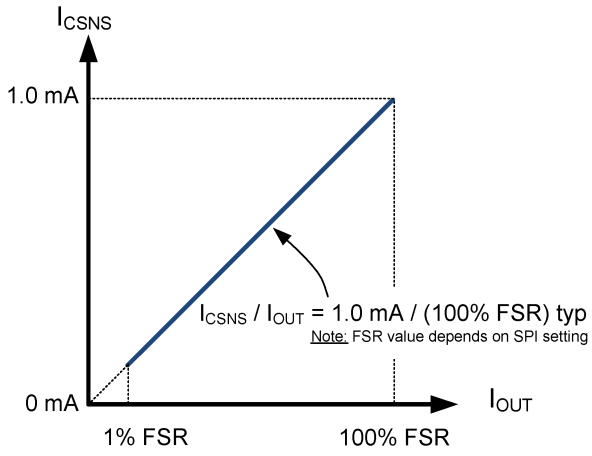


Figure 19. Output current sensing

The feedback is suppressed during OCHI window ($t \leq t_{OCHI1} + t_{OCHI2} + t_{OCHI3}$) and only enabled during low overcurrent shutdown threshold (OCLO). During PWM operation, the current feedback circuit (CSNS) delivers current only during the on time of the output

switch. Current sense settling time, $t_{CSNS(SET)}$, varies with current amplitude. Current sense valid time, $t_{CSNS(VAL)}$, depends on the PWM frequency (see Section 10.1.5.5 "Electrical characterization").

An advanced current sense mode (ACM) is implemented to diagnose LED loads in Normal mode and to improve current sense accuracy for low current loads. In the ACM mode, the offset sign of current sense amplifier is toggled on every CSNS SYNCB rising edge. The error amplifier offset contribution to the CSNS error can be fully eliminated from the measurement result by averaging each two sequential current sense measurements. The ACM mode is enabled with the ACM ENx bits inside the ACM control register #10-1. When the ACM ENx bit is:

- low (logic[0]), ACM disabled (default status and during Fail mode)
- high (logic[1]), ACM enabled

In ACM mode:

- the precision of the current recopy feature (CSNS) is improved, especially at low output currents by averaging CSNS reporting on sequential PWM periods
- the current sense full scale range (FSR) is reduced by a factor of two
- the overcurrent protection threshold OCLO is reduced by a factor of two

Figure 20 describes the timings between the selected channel current and the analog feedback current. Current sense valid time pertains to stabilization time needed after turn on. Current sense settling time pertains to the stabilization time needed after the load current changes while the output is continuously on or when another output signal is selected.

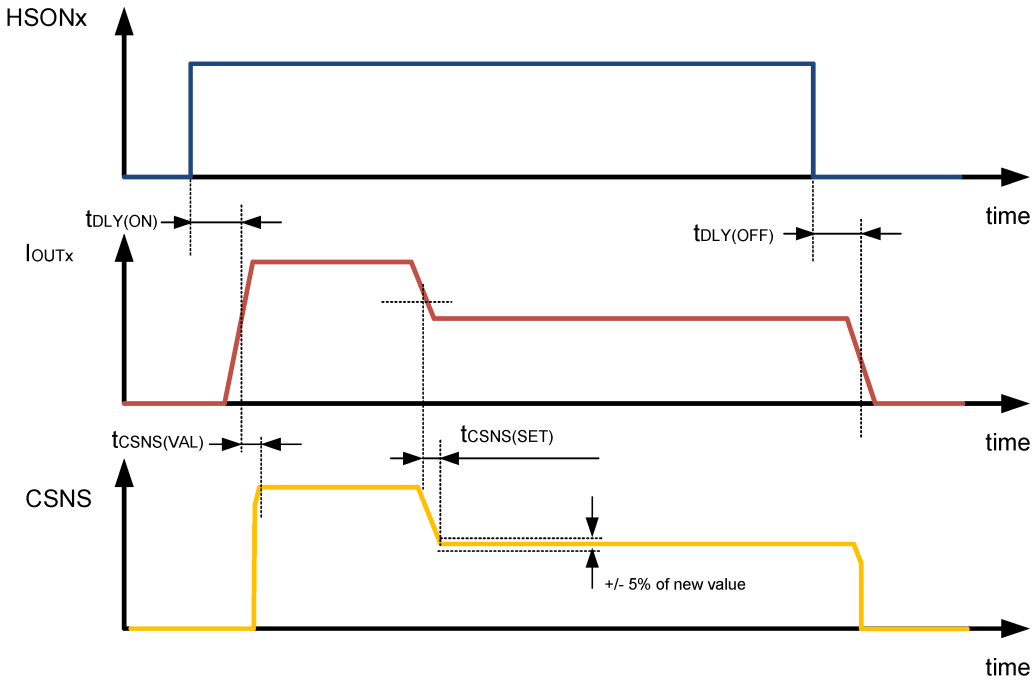


Figure 20. Current sensing response time

Internal circuitry limits the voltage of the CSNS pin when its sense resistor is absent. This feature prevents damage to other circuitry sharing this electrical node, such as a microcontroller pin, for example. Several 32XSG devices may be connected to one shared CSNS resistor.

10.1.5.2 Supply voltage monitoring

The V_{PWR} monitor provides a voltage proportional to the supply tab. The CSNS voltage is proportional to the V_{PWR} voltage as shown in Figure 21.

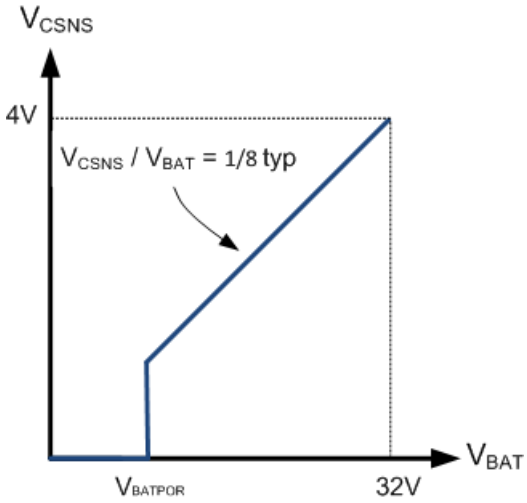


Figure 21. Supply voltage reporting

10.1.5.3 Temperature monitoring

The average temperature of the control die is monitored by an analog temperature sensor. The CSNS pin can report the voltage of this sensor. The chip temperature monitor output voltage is independent of the resistor connected to the CSNS pin, provided the resistor is within the min/max range of 5.0 kΩ to 50 kΩ. Temperature feedback range, T_{FB}, –40 °C to 150 °C.

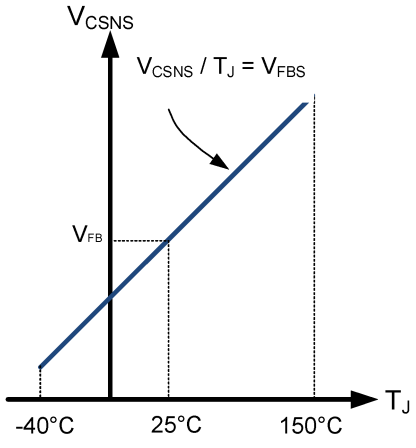


Figure 22. Temperature reporting

10.1.5.4 Analog diagnostic synchronization

A current sense synchronization pin is provided to simplify the synchronous sampling of the CSNS signal. The CSNS SYNCB pin is an open drain requiring an external 5.0 kΩ (min.) pull-up resistor to V_{CC}. The CSNS SYNCB signal is:

- available during Normal mode only

- behavior depends on the type of signal selected by the MUX2…MUX0 bits in the initialization 1 register #0. This signal is either a current proportional to an output current or a voltage proportional to temperature or the supply voltage

Current sense signal

When a current sense signal is selected:

- the pin delivers a recopy of the output control signal during on phase of the PWM defined by the SYNC EN0, SYNC EN1 bits inside the initialization 1 register #0

Table 18. Current sense signal details

SYNC EN1	SYNC EN0	Setting	Behavior
0	0	OFF	CSNS SYNCB is inactive (high)
0	1	VALID	CSNS SYNCB is active (low) when CSNS is valid. During switching the output of MUX, the CSNS SYNCB is inactive (high)
1	0	TRIG0	As in setting VALID, but after a change of the MUX, the CSNS SYNCB is inactive (high) until the next PWM cycle is started
1	1	TRIG1/2	Pulses (active low) from the middle of the CSNS pulse to its end are generated. Switching phases (output and MUX) and the time from the MUX switching to the next middle of the CSNS pulse are blanked (high)

- the CSNS SYNCB pulse is suppressed during OCHI and during OFF phase of the PWM
- the CSNS SYNCB is blanked during settling time of the CSNS multiplexer and ACM switching by a fixed time of $t_{DLY(ON)} + t_{CSNS(SET)}$
- when a PWM clock fail is detected, the CSNS SYNCB delivers a signal with 50 % duty cycle at a fixed period of 6.5 ms
- when the output is programmed with 100 % PWM, the CSNS SYNCB delivers a logic[0] a high pulse with the length of 100 µs (typ.) during the PWM counter overflow for TRIG0 and TRIG1/2 settings
- In case of an output fault, the CSNS SYNCB signal for current sensing does not deliver a trigger signal until the output is enabled again

Temperature signal or V_{PWR} monitor signal

When a voltage signal (average control die temperature or supply voltage) is selected:

- the CSNS SYNCB delivers a signal with 50 % duty cycle and the period of the lowest prescaler setting (f_{CLK}/1024)
- and a PWM clock fail is detected, the CSNS SYNCB delivers a signal with 50 % duty cycle at a fixed period of 6.5 ms ($t_{SYNC\ DEFAULT}$)

10.1.5.5 Electrical characterization

Table 19. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 30 V, –40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
CURRENT SENSE CSNS					
R_{CSNS}	Current sense resistor range	5.0	—	50	kΩ
$I_{CSNS\ LEAK}$	Current sense leakage current when CSNS is disabled	–1.0	—	+ 1.0	µA
V_{CS}	Current sense clamp voltage	6.0	—	8.0	V

Symbol	Characteristic	Min	Typ	Max	Unit
I_{FSR}	Current sense full scale range for 7.0 mΩ power channel				
	High OCLO and ACM = 0	—	22	—	A
	Low OCLO and ACM = 0	—	11	—	
	High OCLO and ACM = 1	—	11	—	
	Low OCLO and ACM = 1	—	5.5	—	
ACC I_{CSNS}	Current sense accuracy for 7.0 V ≤ V_{PWR} ≤ 30 V for 7.0 mΩ power channel				
	I_{OUT} = 80 % FSR	–11	—	11	%
	I_{OUT} = 25 % FSR	–14	—	14	
	I_{OUT} = 10 % FSR	–20	—	20	
	I_{OUT} = 5.0 % FSR	–29	—	29	
$I_{CSNSMIN}$	Minimum current sense reporting for 7.0 mΩ [1] [2]				
	7.0 V < V_{PWR} < 30 V	—	—	1.0	%
I_{FSR}	Current sense full scale range for 7 mΩ power channel				
	High OCLO and ACM = 0	—	11	—	A
	Low OCLO and ACM = 0	—	5.5	—	
	High OCLO and ACM = 1	—	5.5	—	
	Low OCLO and ACM = 1	—	2.75	—	
ACCI_{CSNS}	Current sense accuracy for 7.0 V ≤ V_{PWR} ≤ 30V for 17 mΩ power channel [1]				
	I_{OUT} = 80 % FSR	–11	—	+11	%
	I_{OUT} = 25 % FSR	–14	—	+14	
	I_{OUT} = 10 % FSR	–20	—	+20	
	I_{OUT} = 5.0 % FSR	–29	—	+29	
$I_{CSNSMIN}$	Minimum current sense reporting for 17 mΩ [1] [2]				
	9.0 V ≤ V_{PWR} ≤ 30 V	—	—	1.0	%
V_{PWR}	Supply voltage feedback range	V_{PWRMAX}	—	40	V
ACC V_{PWR}	Supply feedback precision	–7.0	—	+7.0	%
T_{FB}	Temperature feedback range [3]	–40	—	150	°C
V_{FB}	Temperature feedback voltage at 25 °C	—	2.31	—	V
COEF V_{FB}	Temperature feedback thermal coefficient	—	7.72	—	mV/°C
ACC T_{FB}	Temperature feedback voltage precision				
	Default	–15	—	+15	°C
	1 calibration point at 25 °C and V_{PWR} = 7.0 V	–5.0	—	+5.0	
$t_{CSNS(SET)}$	Current sense settling time [3]				
	Current sensing feedback for I_{OUT} from 75 % FSR to 50 % FSR	—	—	40	µs
	Current sensing feedback for I_{OUT} from 10 % FSR to 1.0 %	—	—	260	
	FSR temperature and supply voltage feedbacks	—	—	20	
$t_{CSNS(VAL)}$	Current sense valid time current sensing feedback [4]				
	Low / medium frequency ranges for I_{OUT} > 20 % FSR	10	—	150	µs
	Low / medium frequency ranges for I_{OUT} ≤ 20 % FSR	70	—	300	
	High frequency range for I_{OUT} > 20 % FSR	5.0	—	75	
	High frequency range for I_{OUT} ≤ 20 % FSR	70	—	300	
	Temperature and supply voltage feedback	—	—	12	
	Supply voltage feedback	—	—	15	
$t_{SYNC\ DEFAULT}$	Current sense synchronization period for PWM clock failure	4.8	6.5	8.2	ms
CURRENT SENSE SYNCHRONIZATION CSNS SYNCB					
$R_{CSNS\ SYNC}$	Pull-up current sense synchronization resistor range	5.0	—	—	kΩ
V_{OL}	Current sense synchronization logic output low state level at 1.0 mA	—	—	0.4	V
$I_{OUT\ MAX}$	Current sense synchronization leakage current in tri-state (CSNS SYNC from 0 to 5.5 V)	–1.0	—	+1.0	µA

[1] Precision either OCLO and ACM setting.
[2] Error of ±100 % without calibration for all modes and ±50 % with 1 calibration point done at 25 °C.
[3] Parameter is derived mainly from simulations.
[4] Tested at 5.0 % of final value at VPWR = 14 V, current step from 0 A to 2.8 A (or 5.6 A). Parameter guaranteed by design at 1 % of final value.

10.2 Power supply functional block description and application information

10.2.1 Introduction

The device is functional when wake = [1] with supply voltages from 5.5 V to 40 V (V_{PWR}), but is fully specification compliant only between 7.0 V and 30 V. The VPWR pin supplies power to the internal regulator, analog, and logic circuit blocks. The VCC pin (5.0 V typ.) supplies the output register of the Serial Peripheral Interface (SPI) and the OUT6 driver. Consequently, the SPI registers cannot be read without presence of V_{CC}. The employed IC architecture guarantees a low quiescent current in Sleep mode (wake = [0]).

10.2.2 Wake state reporting

The CLK input/output pin is also used to report the wake state of the device to the microcontroller as long as RSTB is logic [0].

When the device is in:

- "wake state" and RSTB is inactive, the CLK pin reports a high signal (logic[1])
- "sleep mode" or the device is wake by the RSTB pin, the CLK is an input pin

10.2.2.1 Electrical characterization

Table 20. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 30 V, –40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
CLOCK INPUT/OUTPUT CLK					
V_{OH}	Logic output high state level (CLK) at 1.0 mA	V_{CC} – 0.6	—	—	V

10.2.3 Supply voltage disconnection

10.2.3.1 Loss of V_{PWR}

In case of V_{PWR} disconnection (V_{PWR} ≤ $V_{PWR\ POR}$) the device behavior depends on V_{CC} voltage value:

- V_{CC} ≤ $V_{CC\ POR}$: the device enters the power off mode. All outputs are shut off immediately. All registers and faults are cleared
- V_{CC} > $V_{CC\ POR}$: all registers and faults are maintained. OUT1:5 are shut off immediately. The ON/OFF state of OUT6 depends on the current SPI configuration. SPI reporting is available when V_{CC} remains within its operating voltage range (4.5 V to 5.5 V)

The wake-up event is not reported to the CLK pin. The clamping structures (supply clamp, negative output clamp) are available to protect the device. No current is conducted from V_{CC} to V_{PWR}. An external current path must be available to drain the energy from an inductive load, if a supply disconnection occurs when an output is ON.

10.2.3.2 Loss of V_{CC}

In case of a V_{CC} disconnection, the device behavior depends on V_{PWR} voltage:

- $V_{PWR} \leq V_{PWR\ POR}$: the device enters the power off mode. All outputs are shut off immediately. All registers and faults are cleared
- $V_{PWR} > V_{PWR\ POR}$: the SPI is not available. Therefore, the device enters WD timeout

The clamping structures (supply clamp, negative output clamp) are available to protect the device. No current is conducted from V_{PWR} to V_{CC}.

10.2.3.3 Loss of device GND

During loss of ground, the device cannot drive the loads, therefore the OUT1…OUT5 outputs are switched off and the OUT6 voltage is pulled up. The device might be damaged in this failure condition where the load is inductive and V_{PWR} is above 28 V. For protection of the digital inputs series resistors (1.0 kΩ typ.) can be provided externally in order to limit the current to I_{CL}.

10.2.3.4 Electrical characterization

Table 21. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 30 V, –40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
SUPPLY VPWR					
$V_{PWR\ POR}$	Supply power on reset	2.0	3.0	4.0	V
VCC					
$V_{CC\ POR}$	V_{CC} power on reset	2.0	3.0	4.0	V
GROUND GND					
$V_{GND\ SHIFT}$	Maximum ground shift between GND pin and load ground	–1.5	—	+1.5	V

10.3 Communication interface and device control functional block description and application information

10.3.1 Introduction

In Normal mode, the power output channels are controlled by the embedded PWM module, which is configured by the SPI register settings. For bidirectional SPI communication, V_{CC} has to be in the authorized range. Failure diagnostics and configuration are also performed through the SPI port. The reported failure types are: openload, short-circuit to supply, severe short-circuit to ground, overcurrent, overtemperature, clock fail, and under and overvoltage. For direct input control, the device must be in Fail-safe mode. V_{CC} is not required and this mode can be forced by the LIMP input pin.

10.3.2 Fail mode input (LIMP)

The Fail mode of the component can be activated by LIMP direct input. The Fail mode is activated when the input is logic [1]. In Fail mode, the channel power outputs are controlled by the corresponding inputs (INx). Even though the input thresholds are logic level compatible, the input structure of the pins are able to withstand supply voltage level (max. 40 V) without damage. External current limit resistors (1.0 kΩ, 10 kΩ) can be used

to handle reverse current conditions. The direct inputs have an integrated pull-down resistor. The LIMP input has an integrated pull-down resistor. The status of the LIMP input can be monitored by the LIMP IN bit inside the device status register #7.

10.3.2.1 Electrical characterization

Table 22. Electrical characteristics

Characteristics noted under conditions 4.5 V ≤ V_{PWR} ≤ 5.5 V, –40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
FAIL MODE INPUT LIMP					
V_{IH}	Logic input high state level	3.5	—	—	V
V_{IL}	Logic input low state level	—	—	1.5	V
I_{IN}	Logic input leakage current in inactive state (LIMP = [0])	– 0.5	—	+0.5	µA
R_{PULL}	Logic input pull-down resistor	25	—	100	kΩ
C_{IN}	Logic input capacitance [1]	—	—	20	pF
DIRECT INPUTS IN1…IN4					
V_{IH}	Logic input high state level	3.5	—	—	V
$V_{IH(WAKE)}$	Logic input high state level for wake-up	3.75	—	—	V
V_{IL}	Logic input low state level	—	—	1.5	V
I_{IN}	Logic input leakage current in inactive state (forced to [0])	–0.5	—	+0.5	µA
R_{PULL}	Logic input pull-down resistor	25	—	100	kΩ
C_{IN}	Logic input capacitance [1]	—	—	20	pF

[1] Parameter is derived mainly from simulations.

10.3.3 MCU communication interface protections

10.3.3.1 Loss of communication interface

If a SPI communication error occurs, the device is switched into Fail mode. A SPI communication fault is detected if:

- the WD bit is not toggled with each SPI message or
- WD timeout is reached or
- protocol length error (modulo 16 check)

The SI stuck to static levels during CSB period and V_{CC} fail (SPI not functional) are indirectly detected by a WD toggle error. The SPI communication error is reported in:

- SPI failure flag (SPIF) inside the device status register #7 in the next SPI communication

As long as the device is in Fail mode, the SPIF bit retains its state. The SPIF bit is delatched during the transition from fail-to-normal modes.

10.3.3.2 Logic I/O plausibility check

The logic and signal I/O are protected against fatal mistreatment by a signal plausibility check, according following table:

I/O	Signal check strategy
IN1 ~ IN4	frequency above limit (low pass filter)
LIMP	frequency above limit (low pass filter)
RSTB	frequency above limit (low pass filter)
CLK	frequency above limit (low pass filter)

The LIMP and IN1…IN4 have an input deglitch time t_{IN_DGL} = 200 µs (typical). If the LIMP input is set to logic [1] for a delay longer than 200 µs (typ.), the device is switched into Fail mode (internal signal called iLIMP).

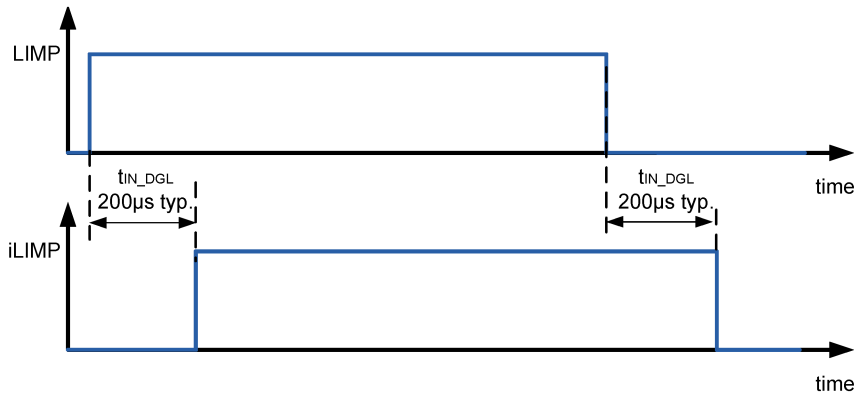


Figure 23. LIMP and iLIMP signal

If the INx input is set to logic [1] for a delay longer than 200µs (typ.), the corresponding channel is controlled by the direct signal (internal signal called iINx).

The RSTB has an input deglitch time t_{RST_DGL} = 10 µs (typ.) for the falling edge only. The CLK has a symmetrical input deglitch time t_{CLK_DGL} = 2.0 µs (typical). Due to the input deglitcher (at the CLK input) a very high input frequency leads to a clock fail detection. The CLK fail detection (clock input frequency detection f_{CLKLOW}) is started immediately with the positive edge of RSTB signal. If the CLK frequency is below $f_{CLK\ LOW}$ limit, the output state depends on the corresponding CHx signal. As soon as the CLK signal is valid, the output duty cycle depends on the corresponding SPI configuration. To delatch the CLK fail diagnosis:

- the clock failure condition must be removed
- a read command of the quick status register #1 must be performed

10.3.3.3 Electrical characterization

Table 23. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 30 V, –40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
LOGIC I/O LIMP IN1:IN4 CLK					

Symbol	Characteristic	Min	Typ	Max	Unit
t_{WD}	SPI watchdog timeout				
	WD SEL = 0	24	32	40	ms
	WD SEL = 1	96	128	160	
t_{DGL}	Input deglitching time				
	LIMP and IN1:IN4	150	200	250	µs
	CLK	1.5	2.0	2.5	
	RSTB	7.5	10	12.5	
$f_{CLOCK\ LOW}$	Clock low frequency detection	50	100	200	Hz

10.3.4 External smart power control (OUT6)

The device provides a control output to drive an external smart power device in Normal mode only. The control is according to the channel 6 settings in the SPI input data register.

- The protection and current feedback of the external SMARTMOS device are under the responsibility of the microcontroller
- The output delivers a 5.0 V CMOS logic signal from V_{CC}

The output is protected against overvoltage. An external current limit resistor (1.0 kΩ, 10 kΩ) must be used to handle negative output voltage conditions. The output has an integrated pull-down resistor to provide a stable OFF condition in Sleep mode and Fail mode. In case of a ground disconnection, the OUT6 voltage is pulled up. External components are mandatory to define the state of external smart power device and to limit possible reverse OUT6 current (resistor in series).

10.3.4.1 Electrical characterization

Table 24. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 30 V, –40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
EXTERNAL SMART POWER OUTPUT OUT6					
$t_{OUT6\ RISE}$	OUT6 rising edge for 100 pF capacitive load	—	—	5.0	µs
$R_{OUT6\ DOWN}$	OUT6 pull-down resistor	5.0	10	30	kΩ
V_{OH}	Logic output high state level (OUT6)	V_{CC} – 0.6	—	—	V
V_{OL}	Logic output low state level (OUT6)	—	—	0.6	V

11 Typical applications

11.1 Introduction

The 32XSG is the latest achievement in DC motors and lighting drivers.

11.1.1 Application diagram

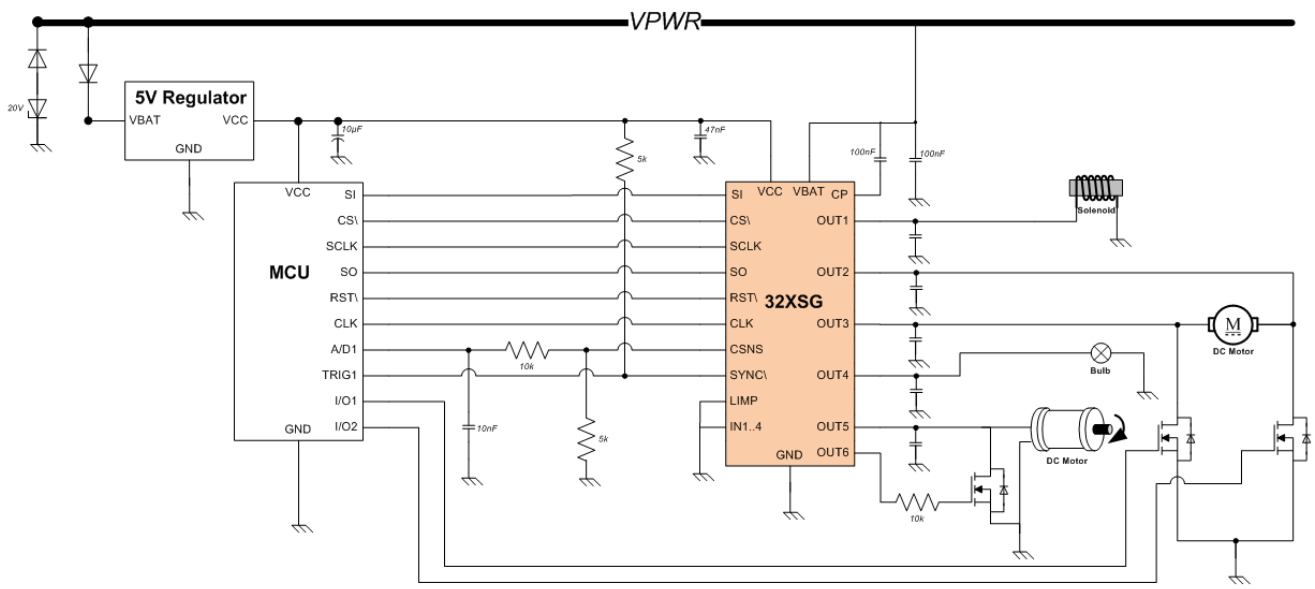


Figure 24. Automation system application

11.1.2 Bill of materials

Table 25. 32XSG Bill of materials

Signal	Location	Mission	Value[1]
V_{PWR}	close to 32XSG eXtreme switch	improve emission and immunity performances	100 nF (X7R 50 V)
CP	close to 32XSG eXtreme switch	charge pump tank capacitor	100 nF (X7R 50 V)
V_{CC}	close to 32XSG eXtreme switch	improve emission and immunity performances	10 nF to 100 nF (X7R 16 V)
OUT1 to OUT5	close to output connector	sustain ESG gun and fast transient pulses improve emission and immunity performances	10 nF to 22 nF (X7R 50 V)
CSNS	close to MCU	output current sensing	5.0 k (±1.0 %)
CSNS	close to MCU	low pass filter removing noise	10 kΩ (±1.0%) and 10 nF (X7R 16 V)
CSNS SYNCB	N/A	pull-up resistor for the synchronization of A/D conversion	5.0 k (±1.0 %)
IN1 to IN4	N/A	sustain high-voltage	1.0 kΩ (±1.0 %)
OUT6	N/A	sustain reverse polarity	1.0 kΩ (±1.0 %)
To sustain 5.0 V voltage regulator Failure mode			
V_{CC}	close to 5.0 V voltage regulator	prevent high-voltage application on the MCU	5.0 V Zener diode and a bipolar transistor

[1] NXP does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While NXP offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

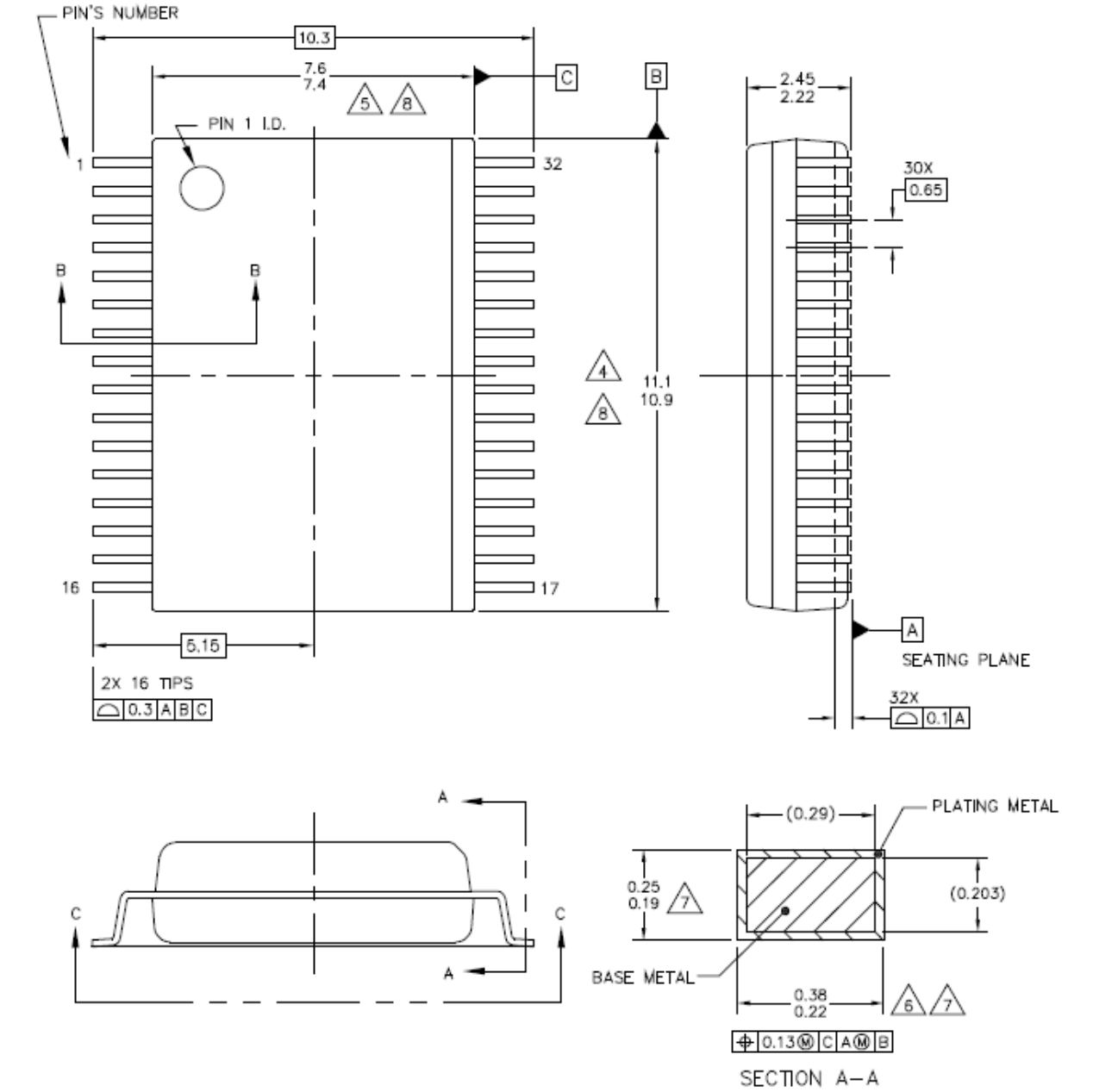
12 Packaging

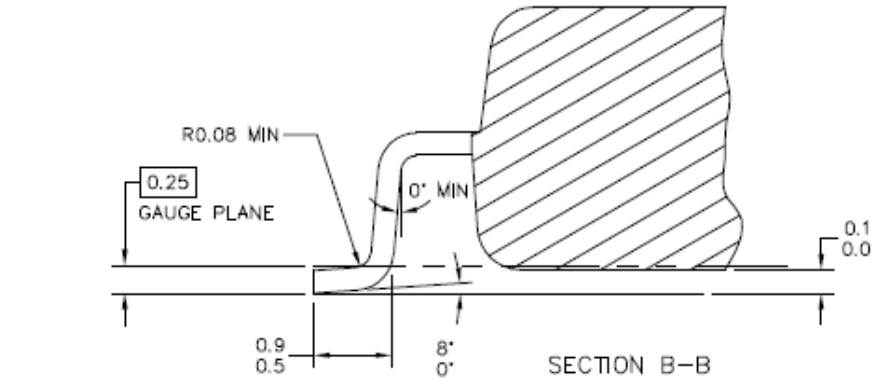
12.1 Package mechanical dimensions

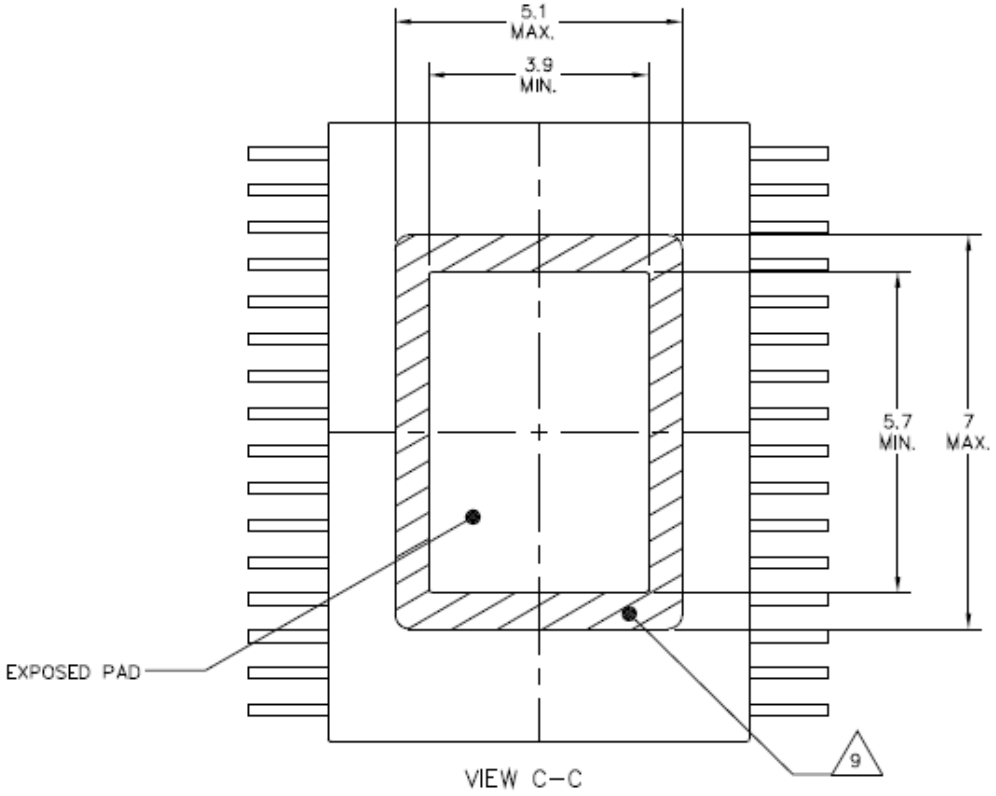
Package dimensions are provided in package drawings. To find the most current package outline drawing, go to nxp.com and perform a keyword search for the drawing's document number.

Table 26. Package outline

Package	Suffix	Package outline drawing number
32-pin SOICEP	EK	98ASA00368D
54-pin SOICEP	EK	98ASA00367D
32-pin SOICEP	BEK	98ASA00894D







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TITLE: SOIC W/B, 32 TERMINAL, 0.65 PITCH, 6.4 X 4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00368D	REV: A
	STANDARD: NON–JEDEC	
	SOT1746–2	07 JAN 2016

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
8. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
9. HATCHED AREA TO BE KEEP–OUT ZONE FOR PCB ROUTING.

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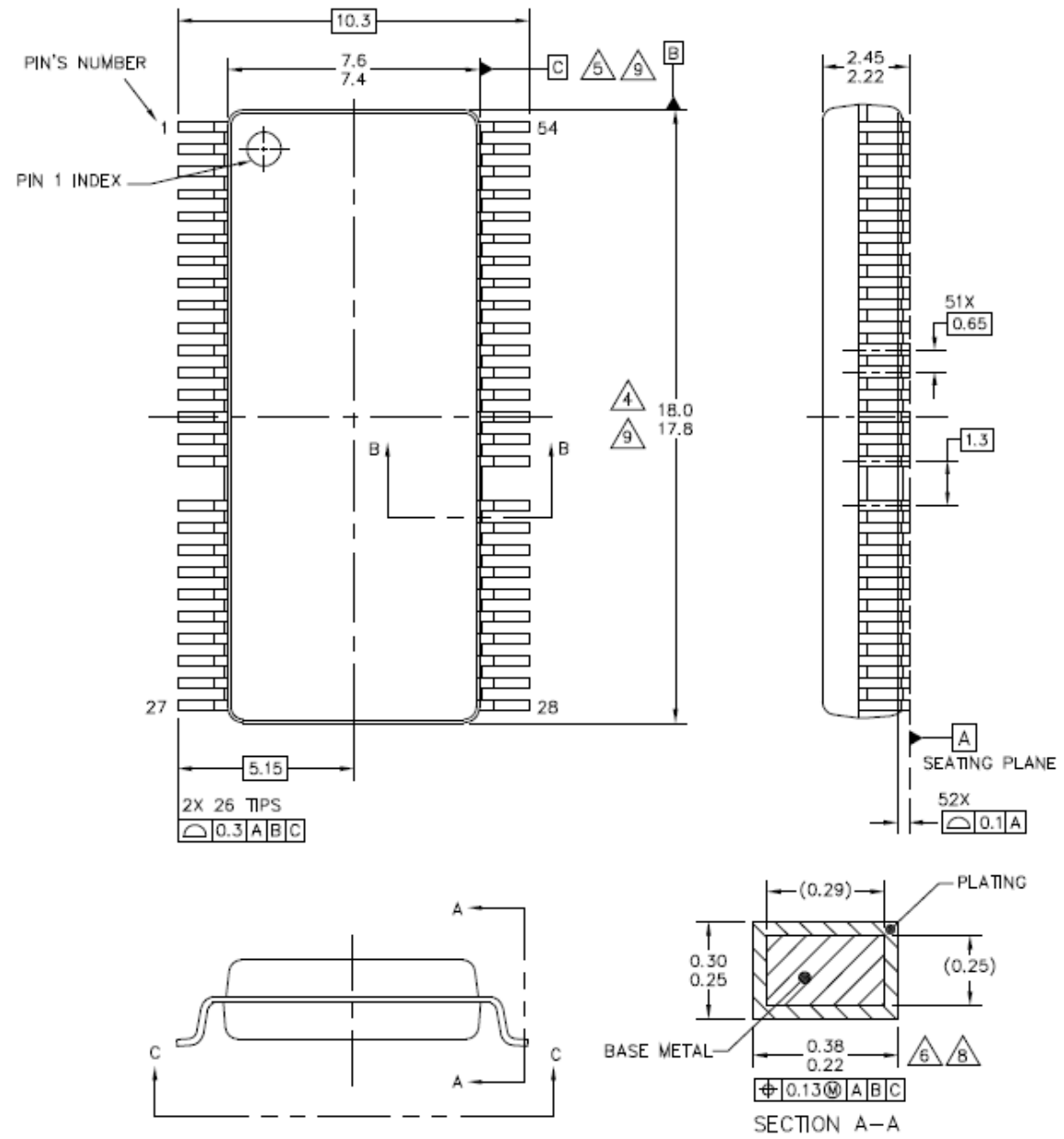
	STANDARD: NON–JEDEC	
	SOT1746–2	07 JAN 2016



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TITLE: SOIC W/B, TOOTH GAP DESIGN, 54 TERMINAL, 0.65 PITCH, 4.5 X 10.3 EXPOSED PAD	DOCUMENT NO: 98ASA00367D	REV: B
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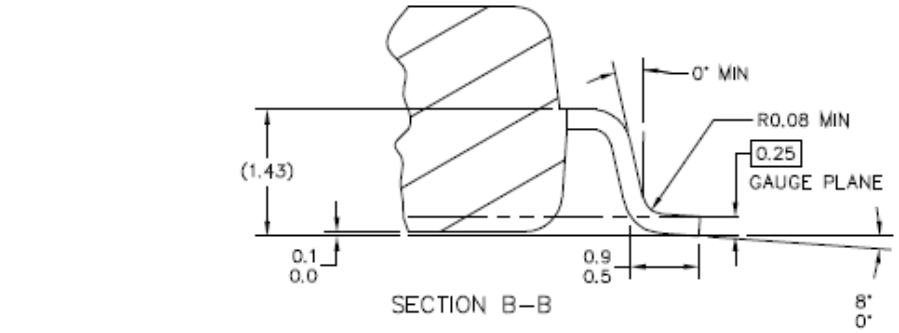
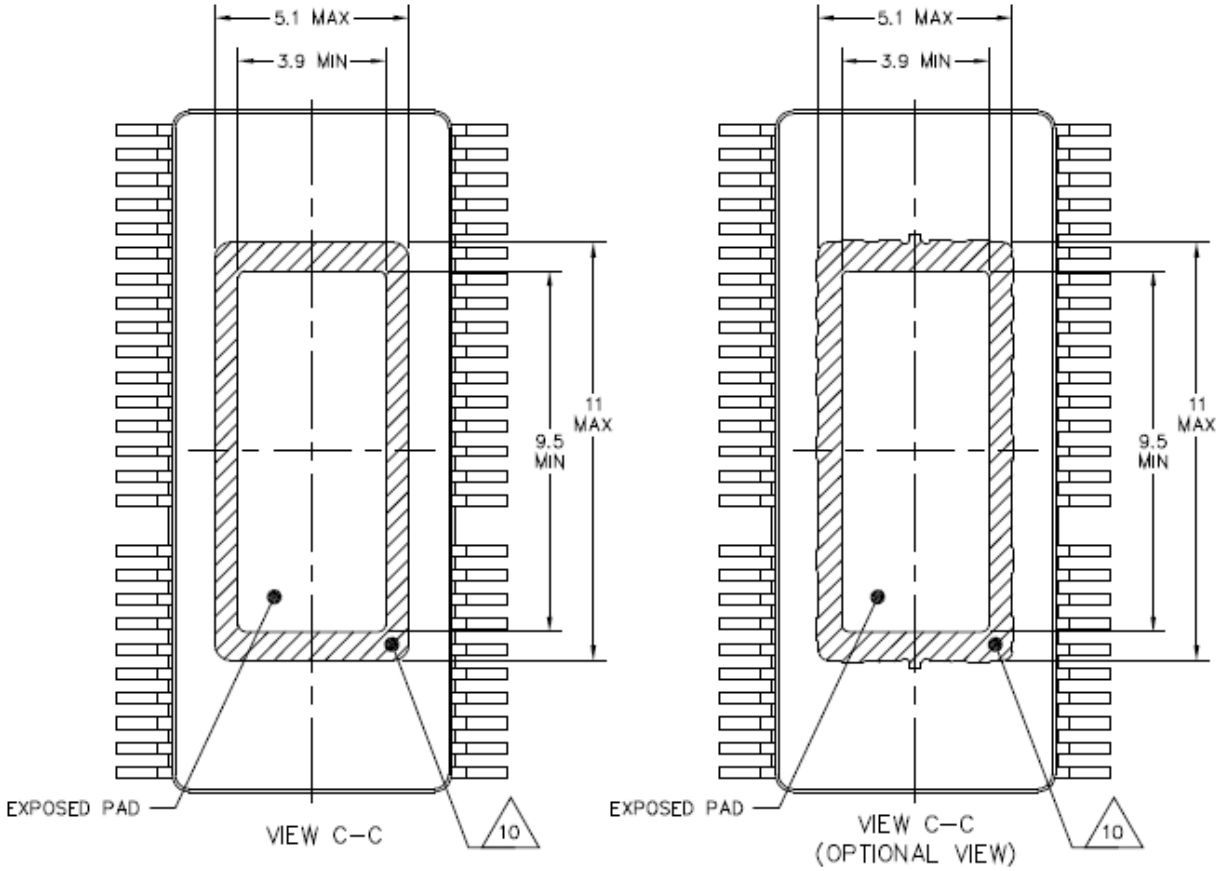
	SOT1747–2	07 JAN 2016





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TITLE: SOIC W/B, TOOTH GAP DESIGN, 54 TERMINAL, 0.65 PITCH, 4.5 X 10.3 EXPOSED PAD	DOCUMENT NO: 98ASA00367D	REV: B
	STANDARD: NON–JEDEC	
	SOT1747–2	07 JAN 2016

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

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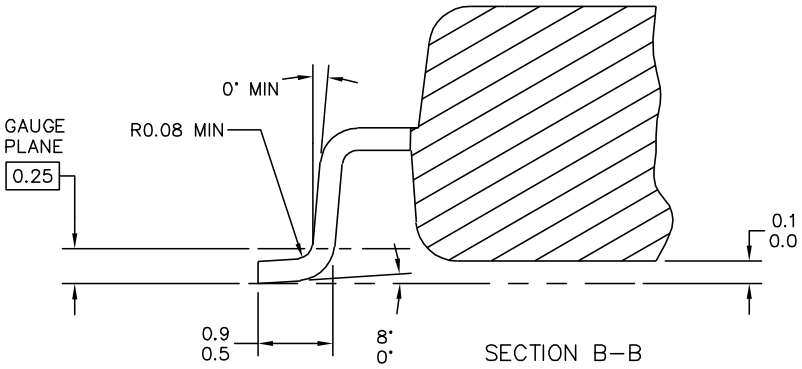
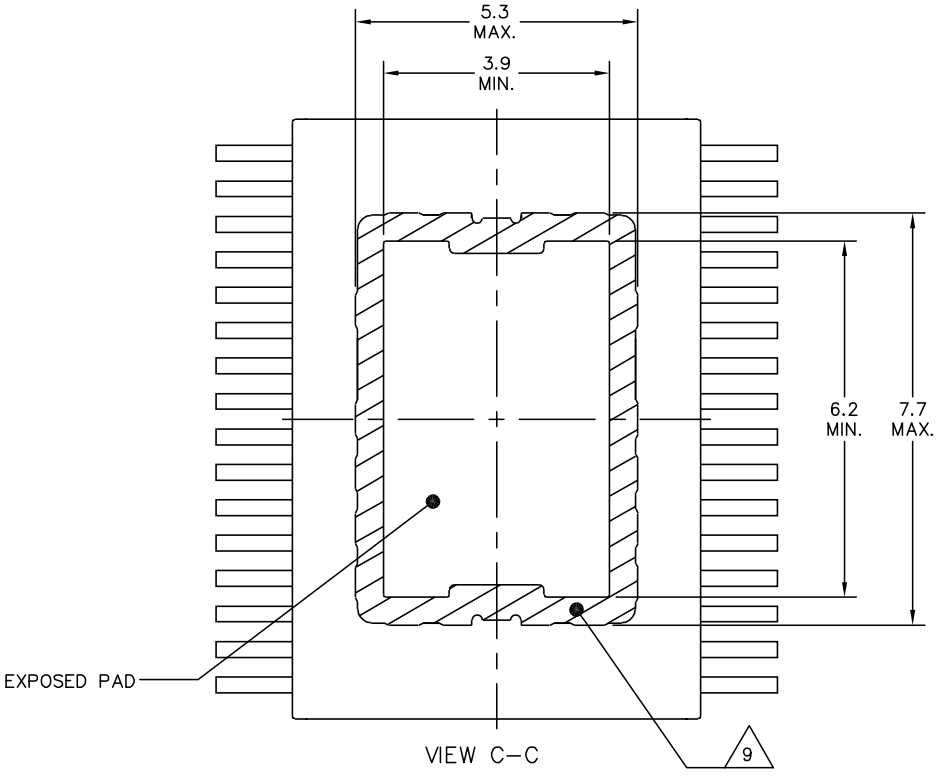
	STANDARD: NON–JEDEC	
	SOT1747–2	07 JAN 2016

MECHANICAL OUTLINE

DO NOT SCALE THIS DRAWING





TITLE: SOIC W/B, 32 TERMINAL, 0.65 PITCH, 4.6 X 7.0 EXPOSED PAD	DOCUMENT NO: 98ASA00894D REV: C
	STANDARD: NON–JEDEC
	SOT1746–4 SHEET: 2

13 Revision history

Revision	Date	Description of changes
1.0	8/2016	• Initial release
2.0	7/2018	• Added MC17XSG500BEK part and associated 98ASA00894D package information
3.0	11/2018	• Updated as per CIN 201811005I • Added footnote [1] to Table 8 • Added footnote [1] to Table 24
4.0	9/2020	• Changed document status from Advance Information to Technical Data • Added values for $R_{PULL\text{-}CSB}$ to Table 8 • Updated the max value for $R_{OUT6\ DOWN}$ in Table 24 (replaced 20 by 30)

14 Legal information

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[2] The term 'short data sheet' is explained in section "Definitions".
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