JD6606S

USB-PD 3.0 and HVDCP Controller

Description

The JD6606S is an integrated USB Power Delivery 3.0 protocol controller. It complies with for HUAWEI Fast Charging Protocol (FCP), Super Charging Protocol (SCP), ACF Protocol and Qualcomm Quick Charge 2.0/3.0/3+ technologies designed for USB Type-C source side charging applications as power adapter, wall chargers, power strip and etc.

The JD6606S monitors the CC pin to detect a USB Type-C attach/detach. It is capable providing output voltage of 5V to 20V. The JD6606S implements VBUS detection and VBUSC discharge for the implementation of compliant connection port. The protection features include over-voltage (VBUS, D+/D-, CC1/CC2).

Additionally, the JD6606S also monitors USB D+/D- data line and automatically adjust the output voltage depending on different device requirement. It is capable providing output voltage of 3.6V to 20V.

The JD6606S integrates dual amplifiers with respectively reference voltages are included for voltage-loop and current-loop regulation to provide constant-voltage (CV) and constant-current (CC) regulation in applications of high precision control.

Features

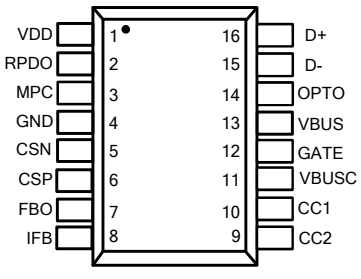
- USB PD 3.0 Certification, TID:3768
- Supports USB Type-C and USB PD 3.0
  - -- 5V to 20V VBUS Source Only
  - -- CC1/CC2 Source Terminator 3A
  - -- Supports PDO Selectable Function
- Supports HUAWEI FCP and SCP
- Supports Qualcomm® Quick Charge™ 2.0/3.0/3+
- Supports USB DCP Shorting D+ Line to D− Line per USB Battery Charging Specification, Revision 1.2
- Supports USB DCP Applying 2.7V on D+ Line and 2.7V on D− Line
- Constant-Voltage and Constant-Current Control
- Multi-Ports Control (MPC) Application
- Power Reduction Function for Multi-Ports
- Over-Voltage Protection
- VBUS Discharge Function
- Over-Current Protection
- CPC-16L and SOP-8 EP Packages

Applications

- Wall-Adapter
- Power Strip
- USB Power Output Ports

Pin Assignments

P5 Package: CPC-16L



SP Package(SOP-8 EP)

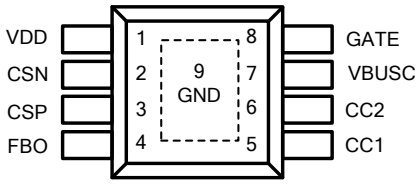


Figure 1. Pin Assignment of JD6606S

Ordering Information

JD6606S□

Package Type
P5: CPC-16L
SP: SOP-8 EP

Typical Application Circuit

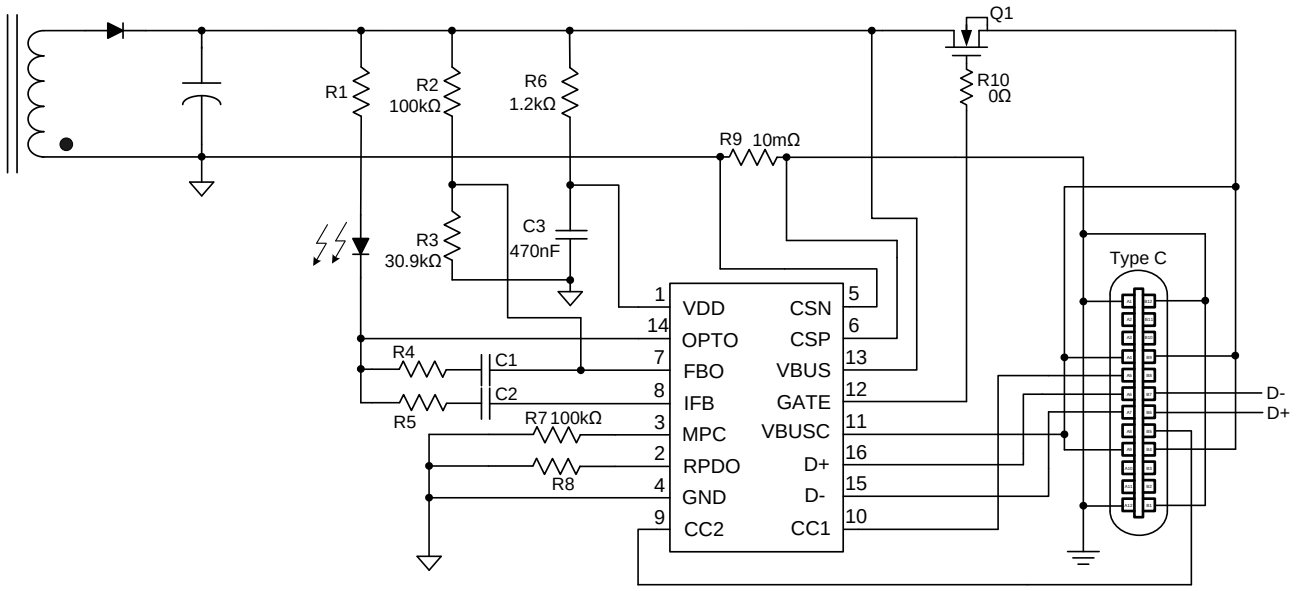


Figure 2. Typical Application Schematic for CPC-16L Package

Table 1. R_{PDO} and Power Configuration Selection:

R_8 (Ω)	QC mode	Rated Power	5V	9V	12V	15V	20V	Power Reduction	QC mode	5V	9V	12V	15V	20V
open	Class A	25W	3A	2.77A				15W	5V	3A				
680k	Class A	20W	3A	2.22A				15W	5V	3A				
470k	Class B	30W	3A	3A	2.5A	2A	1.5A	20W	Class A	3A	2.22A	1.67A		
220k	Class A	18W	3A	2A	1.5A			15W	5V	3A				
100k	Class B	30W	3A	3A	2.5A	2A	1.5A	15W	5V	3A				
68k	Class B	45W	3A	3A	3A	3A	2.25A	20W	Class A	3A	2.22A	1.67A		
47k	Class B	45W	3A	3A	3A	3A	2.25A	30W	Class B	3A	3A	2.5A	2A	1.5A
22k	Class B	60W	3A	3A	3A	3A	3A	45W	Class B	3A	3A	3A	3A	2.25A
10k	Class B	60W	3A	3A	3A	3A	3A	30W	Class B	3A	3A	2.5A	2A	1.5A
0	Class A	20W	3A	2.22A	1.67A			15W	5V	3A				

Note 1: If R_{PDO} setting the 680kΩ or open, the power stage is recommended to use the max voltage design of QC mode.
Note 2: For multiple USB ports application, the voltage of MPC pin will be higher than 0.2V, and then redistributes the rated power.

Typical Application Circuit (Continued)

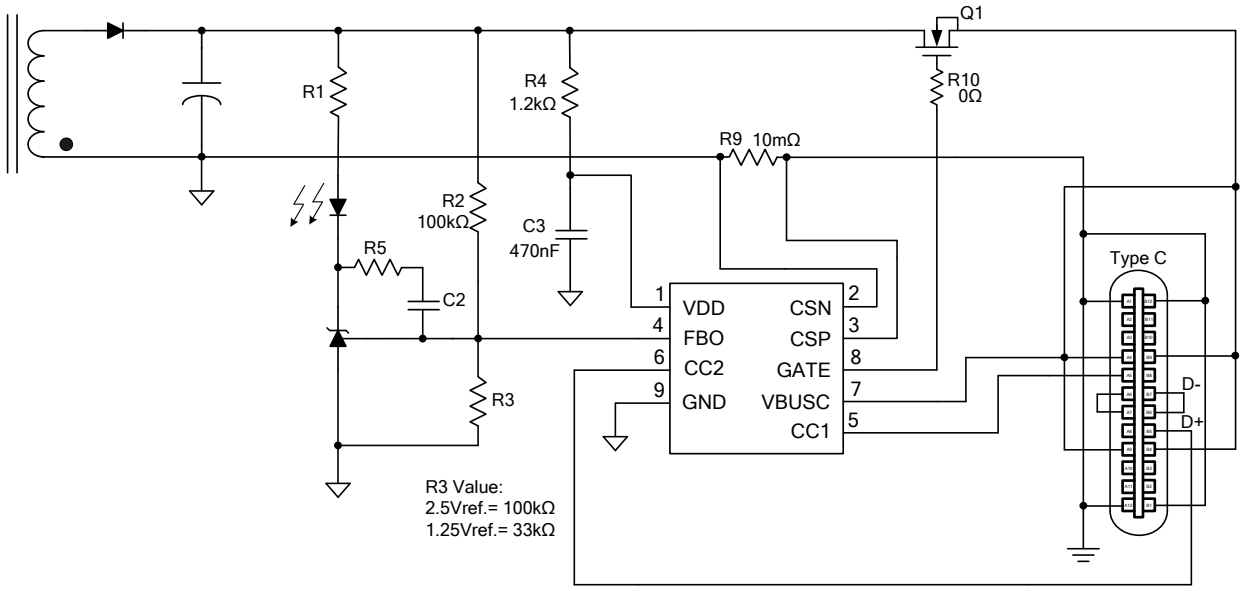


Figure 3. Typical Application Schematic for SOP-8 EP

Table 2. SOP-8 EP Package Power Configuration:

Rated Power	5V	9V	12V
20W	3A	2.22A	1.67A

Typical Application Circuit (Continued)

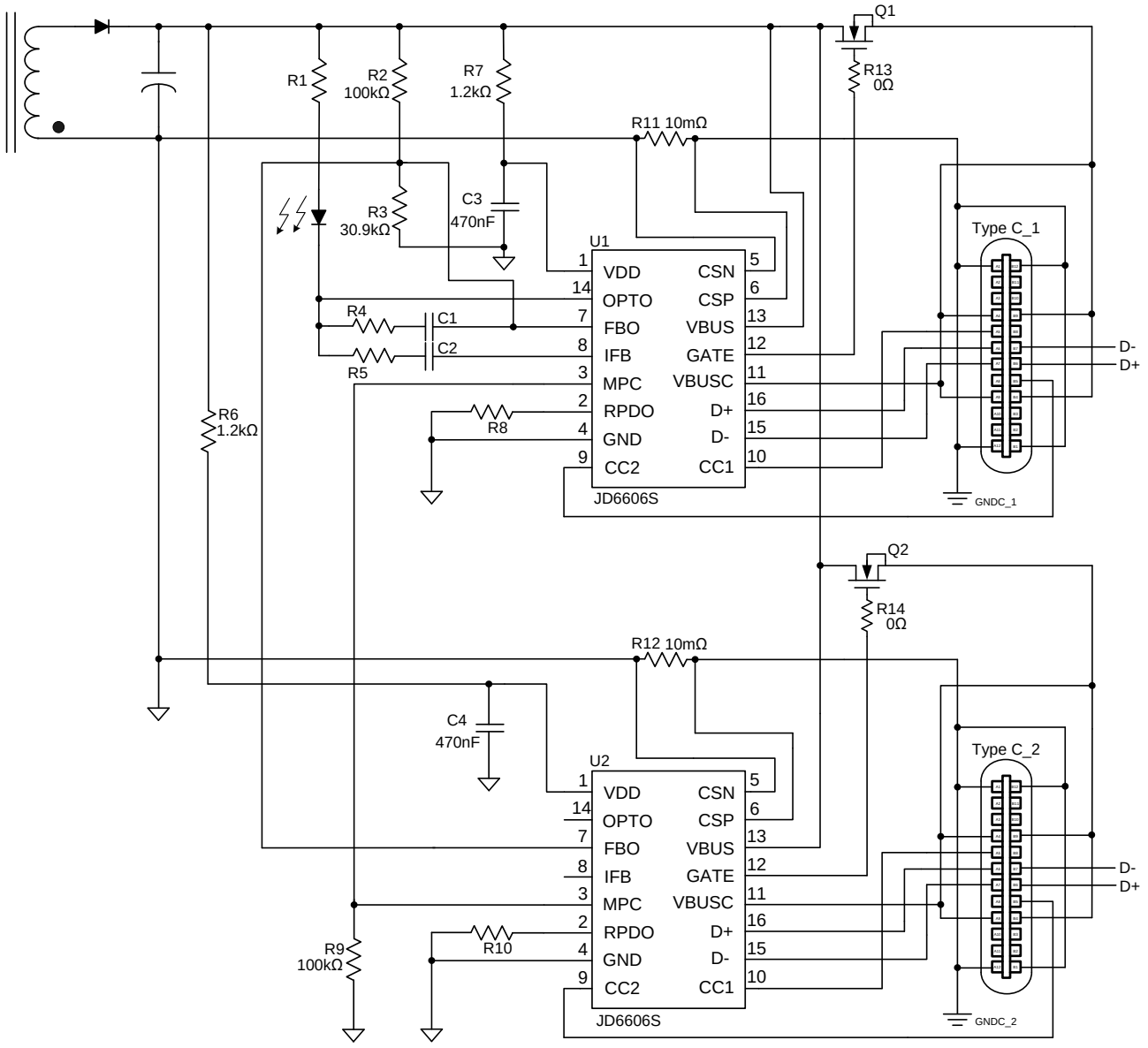


Figure 4. Dual Channel USB Type-C Typical Application Schematic

Typical Application Circuit (Continued)

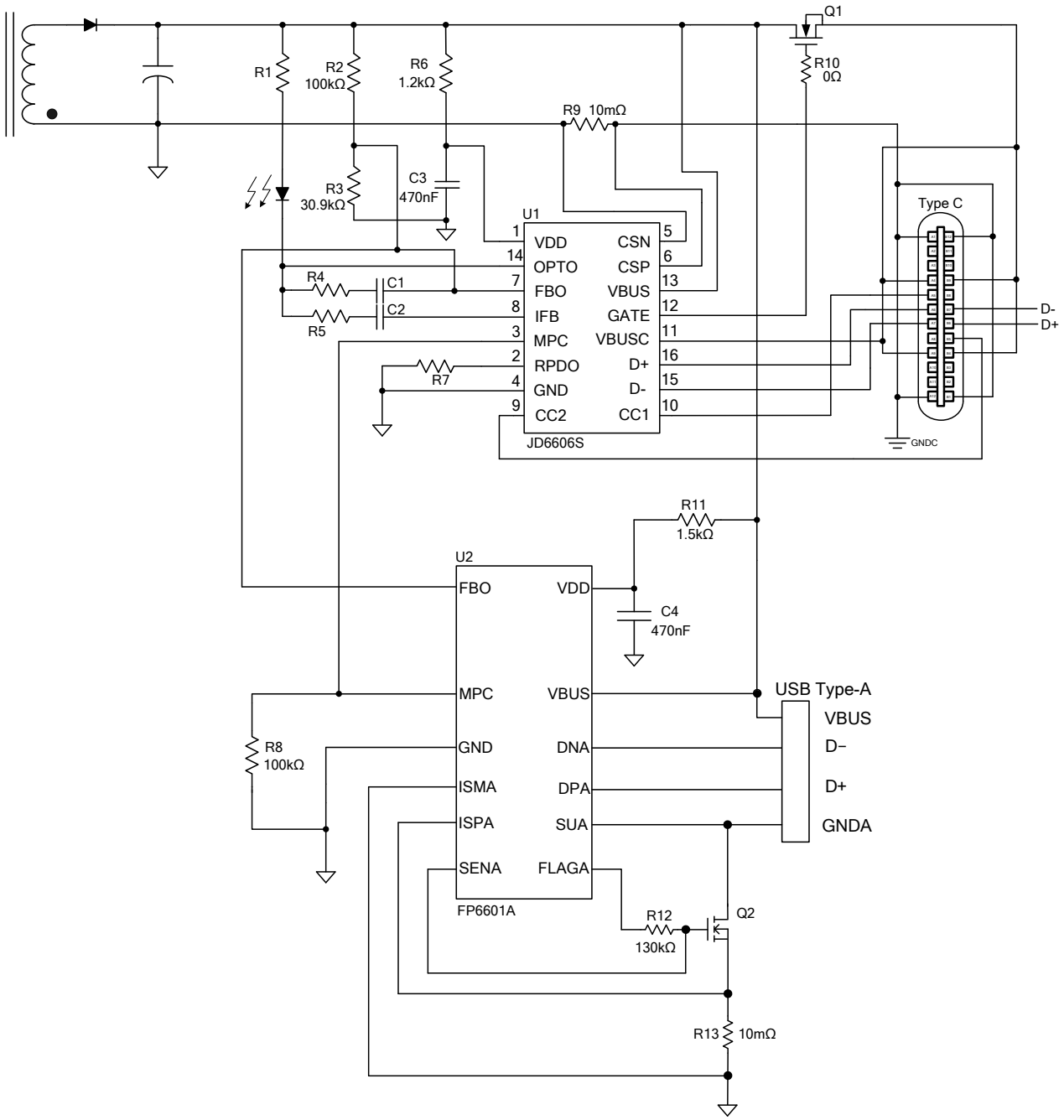


Figure 5. JD6606S+FP6601A Typical Application Schematic

Typical Application Circuit (Continued)

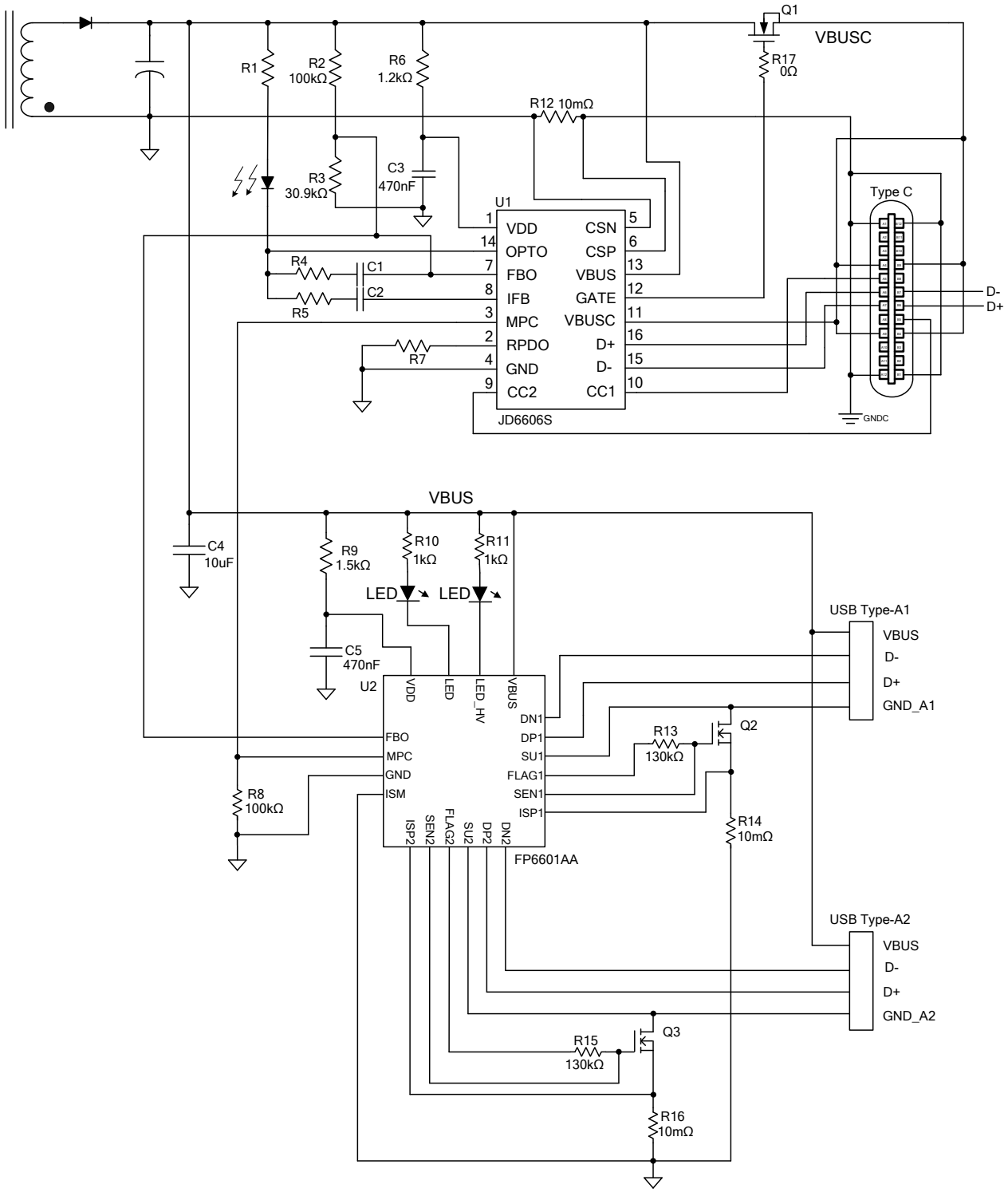


Figure 6. JD6606S+FP6601AA Typical Application Schematic

Functional Pin Description

Pin Name	CPC-16L Pin No.	Pin Function
VDD	**1**	Supply input voltage pin.
RPDO	**2**	Select the PDO VBUS voltage. Connect a resistor to ground.
MPC	**3**	Multi-ports control pin. Connect a 100kΩ resistor to GND.
GND	**4**	Power ground.
CSN	**5**	Negative input of the current sense amplifier.
CSP	**6**	Positive input of the current sense amplifier.
FBO	**7**	Voltage loop feedback.
IFB	**8**	Current loop feedback.
CC2	**9**	Type-C Configuration channel signal 2.
CC1	**10**	Type-C Configuration channel signal 1.
VBUSC	**11**	VBUS voltage detection for Type-C connector side.
GATE	**12**	N-MOSFET gate node control pin.
VBUS	**13**	VBUS voltage detection pin.
OPTO	**14**	Output voltage control pin. Current sink function for opto-coupler node.
D-	**15**	USB D- data line of Type-C.
D+	**16**	USB D+ data line of Type-C.

Functional Pin Description (Continued)

Pin Name	SOP-8 EP Pin No.	Pin Function
VDD	**1**	Supply input voltage pin.
CSN	**2**	Negative input of the current sense amplifier.
CSP	**3**	Positive input of the current sense amplifier.
FBO	**4**	Voltage loop feedback.
CC1	**5**	Type-C Configuration channel signal 1.
CC2	**6**	Type-C Configuration channel signal 2.
VBUSC	**7**	VBUS voltage detection for Type-C connector side.
GATE	**8**	N-MOSFET gate node control pin.
GND	**9**	Power ground.

Absolute Maximum Ratings (Note 3)

- Input Supply Voltage VDD ---------- -0.3V to +7V
- CC1, CC2, D-, D+, OPTO ---------- -0.3V to +24V
- GATE, VBUS, VBUSC ---------- -0.3V to +35V
- CSP, CSN ---------- -0.3V to +6.5V
- FBO, IFB, MPC, RPDO ---------- -0.3V to +6.5V
- Maximum Junction Temperature (T_J) ---------- +150°C
- Storage Temperature (T_S) ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10sec) ---------- +260°C
- Package Thermal Resistance, (θ_{JA})
  - CPC-16L ---------- TBD
  - SOP-8 EP ---------- 60°C/W
- Package Thermal Resistance, (θ_{JC})
  - CPC-16L ---------- TBD
  - SOP-8 EP ---------- 15°C/W

Note 3: Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Input Supply Voltage (VDD) ---------- +3.2V to +6.8V
- Operating Temperature Range (T_A) ---------- -40°C to +125°C

Electrical Characteristics

(VDD=5V, T_A=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Power						
VDD Input Voltage Range	V_{DD}		3.2		6.8	V
Input UVLO Threshold	V_{DD_UVLO}	V_{DD} Rising	3.1	3.3	3.5	V
	V_{DD_HYS}	V_{DD} Falling	2.45	2.6	2.75	V
VDD Supply Current	I_{DD_SUP}	V_{DD}=5V, Nothing Attach	66	100	136	μA
VDD Shunt Voltage	V_{DD_SHDN}		5.9	6.4	6.8	V
N-MOSFET Gate Driver						
GATE Sourcing Current		V_{DD}=4V 0V ≤ V_{GATE} – V_{BUSC} ≤ 6V		TBD		μA
Sourcing Voltage (ON) between GATE and VBUS		V_{DD}=3.2V to 6.8V	5		15	V
VBUS						
VBUS Over Voltage Protection			22.8	24	25.2	V
VBUS Bleed Discharge Resistance	$R_{\_Bleed}$		8	10	12.5	kΩ
VBUS Discharge Resistance	$R_{\_DIS}$			400		Ω
VBUSC Bleed Discharge Resistance	$R_{\_CBLEED}$		8	10	12.5	kΩ
VBUSC Discharge Resistance	$R_{\_CDIS}$			400		Ω
USB Type-C						
SRC CC Current	I_{CC_3A}	Cable is attached whit Rd, PD Disabled	304	330	356	μA
D+/D- OV Threshold (Note 4)	$V_{\_DPDNOV}$	In DCP mode		7		V
D+/D- OV Threshold (Note 4)	$V_{\_DPDNOV}$	In HVDCP Mode		4		V
CCOV Rising (Note 4)	$V_{\_CCOV\text{-}rising}$			1.04*V_{DD}		V
CCOV Falling (Note 4)	$V_{\_CCOV\text{-}falling}$			V_{DD}		V

Electrical Characteristics (Continued)

(VDD=5V, T_A=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High Voltage Dedicated Charging Port (HVDCP)						
Data Detect Voltage	$V_{DAT(REF)}$		0.25	0.325	0.4	V
Output Voltage Selection Reference	V_{SEL_REF}		1.8	2.0	2.2	V
D+ High Glitch Filter Time	$T_{GLITCH(BC)-DPA-H}$		1000	1250	1500	ms
D- Low Glitch Filter Time	$T_{GLITCH(BC)-DNA-L}$			1		ms
Output Voltage Glitch Filter Time	$T_{GLITCH(V)\ CHANGE}$		20	40	60	ms
D- Pull-Down Resistance	$R_{DNA(DWN)}$			20		kΩ
Continuous Mode Glitch Filter Time	$T_{GLITCH-CONT-\ CHANGE}$		100		200	ms
D+ Leakage Resistance	$R_{DAT-LKG}$	V_{DD}=3.2 to 6.4V VDPA=0.6-3.6V Switch SW1=off	300	500	800	kΩ
Switch SW1 On-Resistance	$R_{DS\_ON\_N1}$	V_{DD}=5V,SW1=200μA			40	Ω
UP/Down Current Step	I_{UP}, I_{DOWN}	I_{UP} =0μA (5V),40μA (9V), 70μA (12V),100μA (15V), 150μA (20V) I_{DOWN}=14μA (3.6V)		2		μA
DCP Charging Mode						
$D+_{\_0.48V}$ / $D-_{\_0.48V}$ Line Output Voltage			0.44	0.48	0.52	V
$D+_{\_0.48V}$ / $D-_{\_0.48V}$ Line Output Impedance				900		kΩ
Apple Mode						
$D+_{\_2.7V}$ / $D-_{\_2.7V}$ Line Output Voltage			2.57	2.7	2.84	V
$D+_{\_2.7V}$ / $D-_{\_2.7V}$ Line Output Impedance				33.6		kΩ
D- Section (FCP or SCP)						
D- Tx Valid Output High	V_{TX-VOH}		2.55		3.6	V
D- Tx Valid Output Low	V_{TX-VOL}				0.3	V
D- Rx Valid Output High	V_{RX-VIH}		1.4		3.6	V
D- Rx Valid Output Low	V_{RX-VIL}				1.0	V
D- Output Pull-Low Resistance	R_{PD}		400	500	600	Ω
Unit Interval for PHY Communication	UI	F_{CLK}=125kHz	144	160	180	μs

Electrical Characteristics (Continued)

(VDD=5V, T_A=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Regulator Section							
Voltage Control Loop Reference	V_{REF}				1.21		V
Current control Loop Reference	VCS+	Rsense =10mΩ	In SCP		60		mV
			In QC		36		
			In USB-PD		120%*I_{OUT}		
OPTO Sinking Current	I_{OPTO}				27	80	mA

Note 4: Guarantee by design.

Application Information

JD6606S is an integrated USB Power Delivery 3.0 and USB high voltage dedicated charging protocol (HVDCP) controller, which can be used for Qualcomm's QC 2.0 / 3.0 / 3 +, AFC, FCP and SCP, Apple and other protocol specifications. JD6606S supports a variety of fast charging protocols, which can fast charge most Portable devices. It can be applied to charging adapters, car chargers, power strips and other USB output power devices.

USB Type-C / USB-PD Protocol

JD6606S is used for the USB Type-C interface to support the role of Source. When the sink device is connected, JD6606S will provide 3A current capability on the CC pin. It supports USB-PD 3.0 and compatible with USB-PD 2.0 protocol. The output provides fixed voltage 5V/9V/12V/15V/20V, which can connect a external resistor to select the PDO voltage/current. (Pease refer to page 2 for select the RPDO and power configuration). It also supports Apple's 20W charging specification (9V/2.22A), which can fast charge to the Apple devices like iPhone and can also support Apple's wireless chargers for charging.

QC 2.0/3.0/3+ Protocol

JD6606S supports Qualcomm's QC 2.0/3.0/3+ charging protocol. The output voltage range is setting the class A or class B, please refer to the page 2 select the RPDO and power configuration. It supports output voltage range of QC 2.0 Class A (5V/9V/12V) and Class B (5V/9V/12V/20V), It also supports output voltage range of QC 3.0 Class A (3.6V to 12V, 200mV per step) and Class B (3.6V to 20V, 200mV per step). The step voltage of QC3+ is 20mV.

AFC/FCP/SCP Protocol

The JD6606S supports AFC protocol, the output voltage range is 5V/9V, and it supports FCP protocol, the output voltage range is 5V/9V/12V, it also supports SCP protocol, the charge capability is 4.5V/5A.

CC/CV Control

JD6606S supports constant current (CC)/constant voltage (CV) regulation. The constant voltage (CV) regulation is implemented by detecting the output voltage on the FBO pin via the resistor divider and constant voltage regulation control with compared internal reference voltage of the CV operational amplifier. The constant current (CC) regulation is implemented by detecting the output current via the resistor RSENSE and constant current regulation control with compared internal reference voltage of the CC operational amplifier. If the output current is lower than the CC threshold and the output voltage will be adjusted to the default voltage. When the output current above the CC threshold, the output voltage will drop and the output current will be limited to the maximum current.

VBUS/VBUSC Function

The VBUS and VBUSC are monitoring the voltage and discharge the output for the implementation of a compliant USB Type-C application.

Gate Driver

JD6606S provides a gate driver for controlling external N-MOSFET. The gate driver not only can control N-MOSFET smooth turn on to avoid VBUSC drops in the capacitive load condition but also provide quickly turn-off in any fault condition.

Multi-Port Control

JD6606S can realize the application of multiple USB-C ports share one power source. Connect the MPC pin of the chip to the bus, and connect a resistance of 100KΩ to the GND on the bus. Each chip transmits information through the bus, and then distributes the fixed rated power.

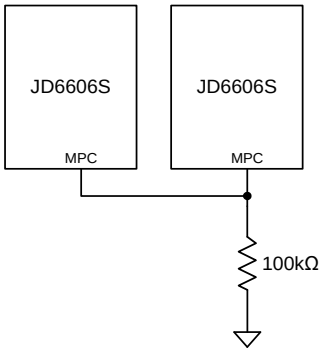


Figure 7. Multi-Port Control (MPC) Application

Application Information (Continued)

Shunt Regulator

The VDD of JD6606S is supplied by the wide output voltage through the external resistor R6. The internal Zener-Diode is utilized to clamp the VDD at 6.4V. The recommended value of R6 and C3 are 1.2kΩ and 470nF, respectively.

VBUS Over-Voltage Protection

JD6606S supports over-voltage protection of VBUS pin. When VBUS voltage is larger than the OVP threshold (24V typ.), GATE pin goes to low level to turn off blocking N-MOSFET. When the fault is removed, the GATE driver recovers to normal operation.

Configuration Channel Protection

JD6606S supports over-voltage protection of CC1/CC2 pin. When CC1/CC2 pin is touched by the external power in abnormal situation, the CC1/CC2 pin of both sink device and source device may be damaged. In order to protect the CC1/CC2 pin of the devices from damage in abnormal situation, the JD6606S will return the output voltage to default output voltage 5V.

Data Line Protection

JD6606S supports overvoltage protection of D+/D− pin. When D+/D− pin is touched by the output voltage in abnormal situation, the D+/D− pin of both sink device and source device may be damaged. In order to protect the D+/D− pin of the devices from damage in abnormal situation, the JD6606S will return the output voltage to default output voltage 5V when the voltage of D+/D− pin is touched larger than 7.5V. If operating in HVDCP mode, the over voltage protection of D+/D- pin is 4V.

PCB Layout Recommendation

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow general guidelines shown as below:

1. Place feedback resistors close to the FB pin.
2. The current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as below, and routed in parallel (differential routing), and the filter for current sense should be placed near the IC.

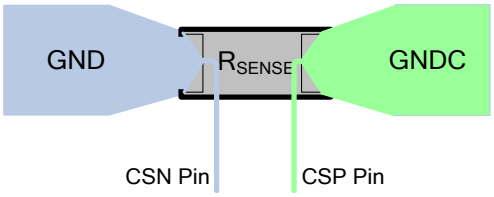
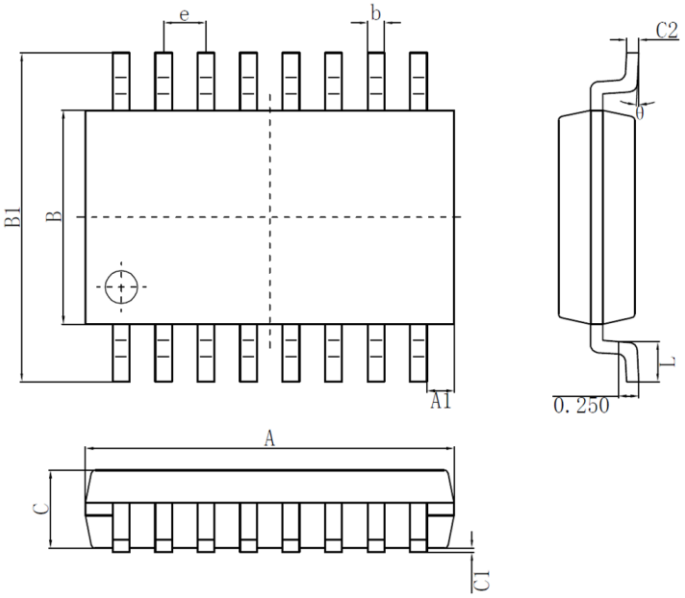


Figure 8. Current Sense

Outline Information

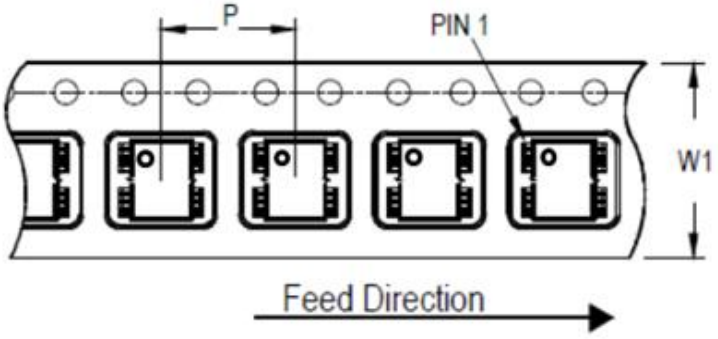
CPC-16L Package (Unit: mm)

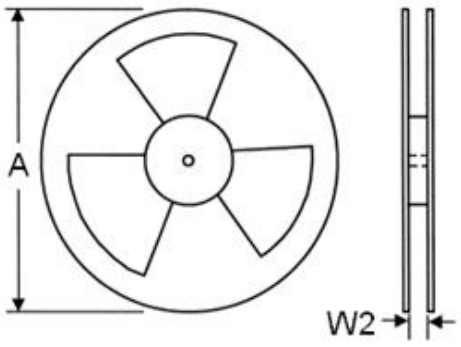


SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	4.50	4.70
A1	0.29	0.39
B	2.50	2.70
B1	3.85	4.15
C	0.85	1.05
C1	0.00	0.15
C2	0.15	0.18
e	0.53(BSC)	
b	0.16	0.26
L	0.40	0.60

Note 5: Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.3mm.

Carrier Dimensions

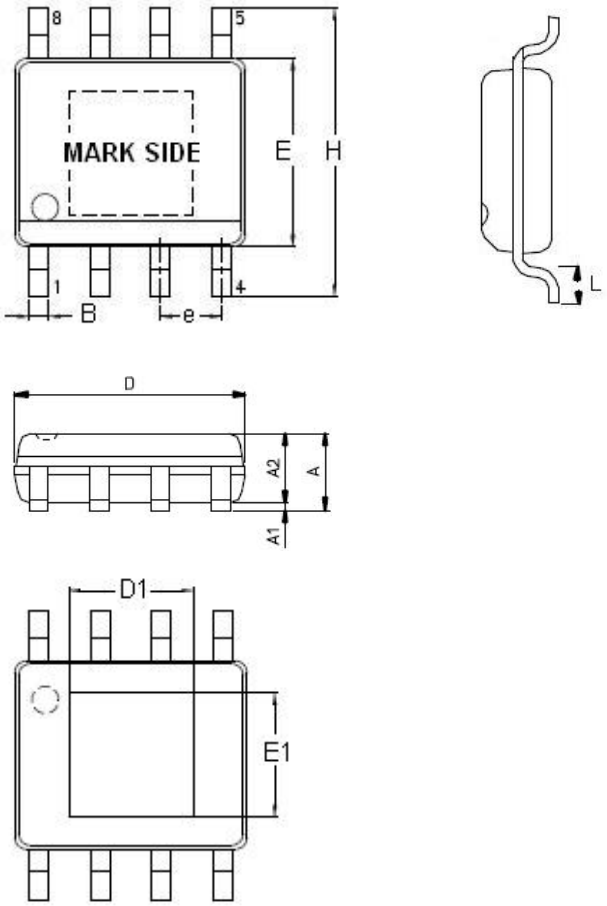




Tape Size (W1)mm	Pocket Pitch (P)mm	Reel Size (A)		Reel Width (W2)mm	Empty CavityLength (mm)	Units per Reel
		(in)	(mm)			
12	8	15	380	12.5	300~1000	6000

Outline Information (Continued)

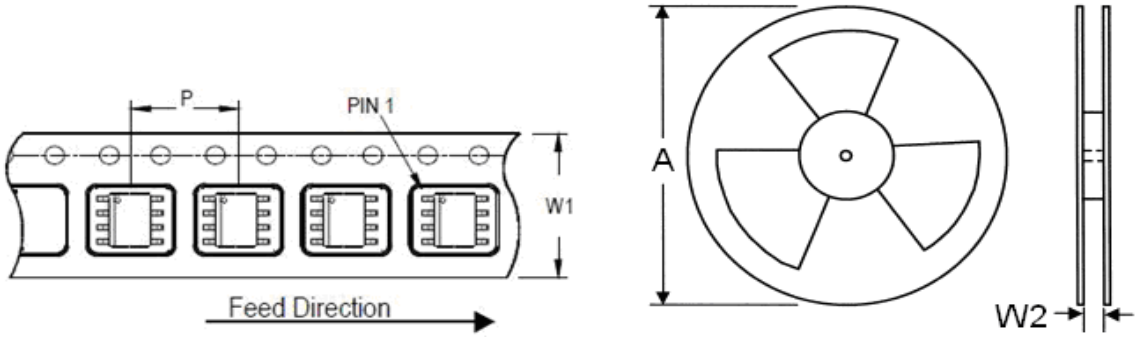
SOP-8 (Exposed Pad) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.25	1.70
A1	0.00	0.15
A2	1.25	1.55
B	0.31	0.51
D	4.80	5.00
D1	3.04	3.50
E	3.80	4.00
E1	2.15	2.41
e	1.20	1.34
H	5.80	6.20
L	0.40	1.27

Note 6: Followed From JEDEC MO-012-E.

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	2,500

Life Support Policy
Jadard's products are not authorized for use as critical components in life support devices or other medical systems.