

Recommended Application:

Calistoga Based Ultra-Mobile PC (UMPC)

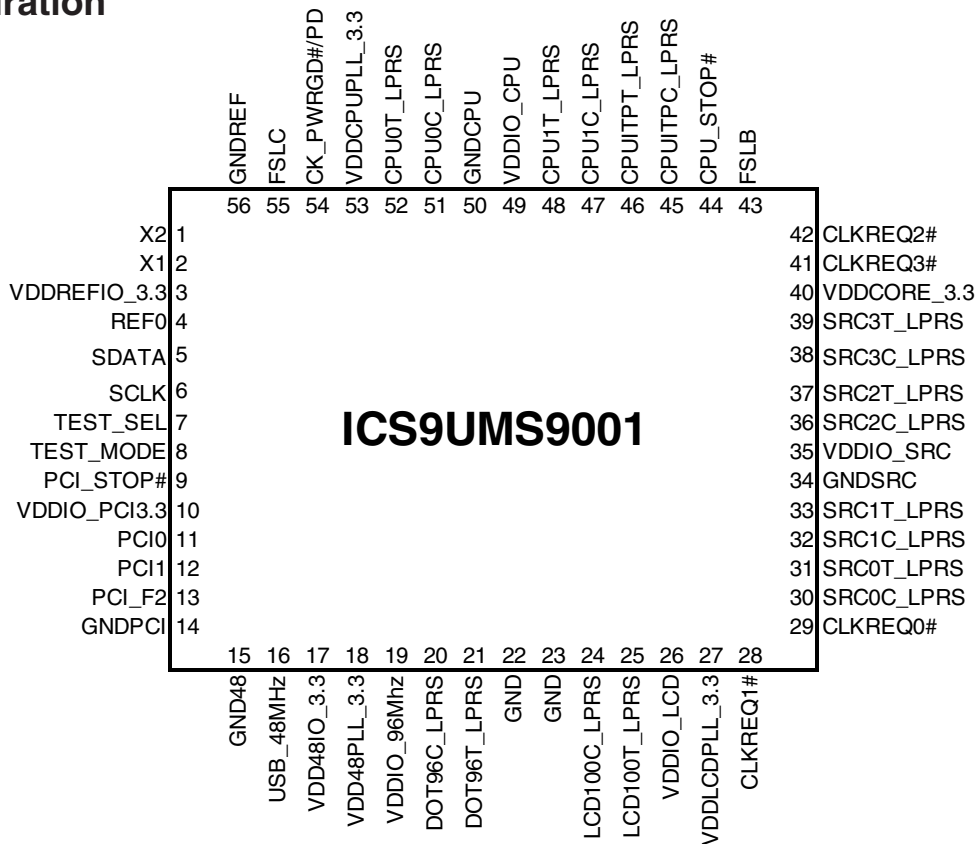
Output Features:

- 2 - CPU Low Power differential push-pull pairs
- 1 - ITP low power differential push-pull pair
- 4 - SRC low power differential push-pull pairs
- 1 - LCD100 SSCD low power differential push-pull pair
- 1 - DOT96 low power differential push-pull pair
- 3 - PCI, 33MHz
- 1 - USB, 48MHz
- 1 - REF, 14.31818MHz

Features/Benefits:

- Supports Dothan ULV CPUs with 100 and 133 MHz CPU outputs
- Dedicated TEST/SEL and TEST/MODE pins saves isolation resistors on pins
- PCI_SRC and CPU STOP inputs for power managment
- Fully integrated Vreg
- Integrated series resistors on differential outputs
- Supports split rail operation for maximum power savings
- Also runs from single 3.3V rail
- 1.05V-3.3V support for differential VDDIO

Pin Configuration



56-pin MLF

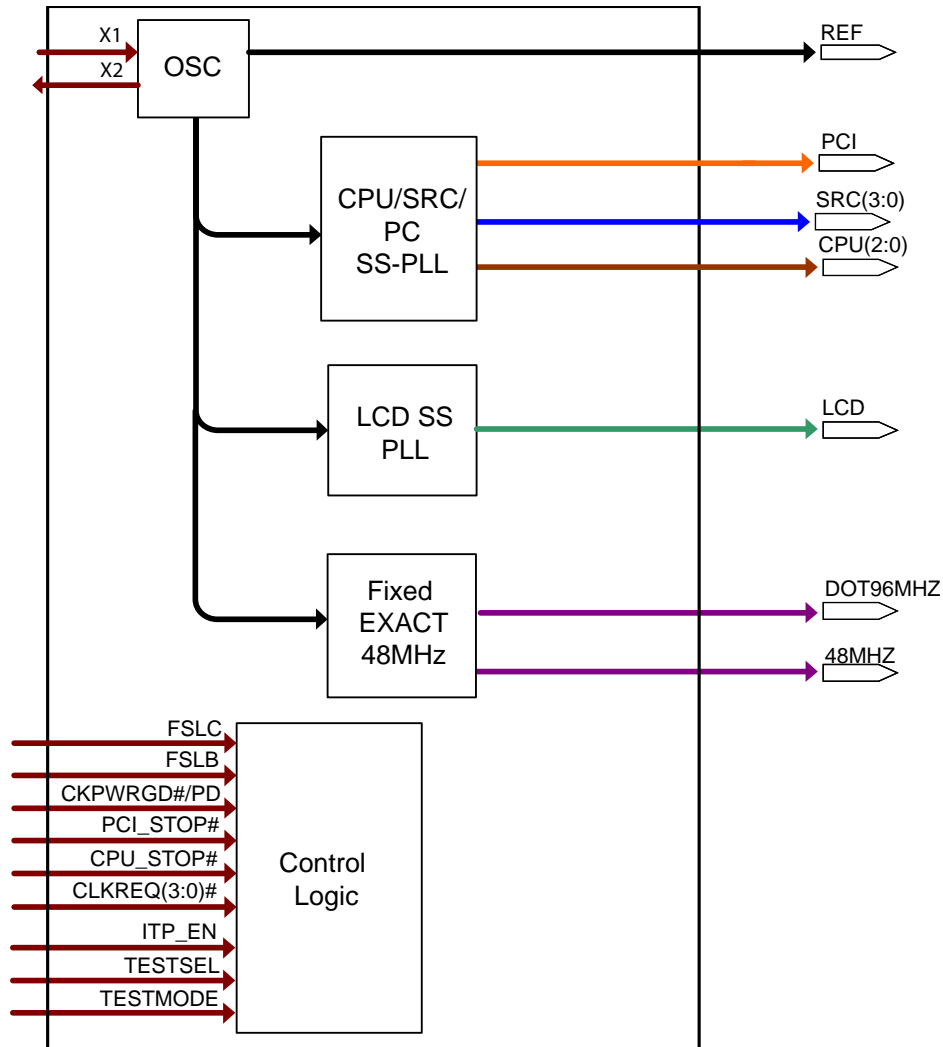
Pin Description

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|---------------|------|--|
| 1 | X2 | OUT | Crystal output, nominally 14.318MHz. |
| 2 | X1 | IN | Crystal input, Nominally 14.318MHz. |
| 3 | VDDREFIO_3.3 | PWR | Power pin for the REF output and crystal oscillator. 3.3V nominal. |
| 4 | REF0 | OUT | 3.3V 14.318MHz reference clock |
| 5 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 6 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 7 | TEST_SEL | IN | 3.3V input that puts the part in test mode. This is a realtime input. See the Test Clarification Table for details. |
| 8 | TEST_MODE | IN | When Test mode is selected, this chooses either hi-Z or REF/N for the outputs. |
| 9 | PCI_STOP# | IN | 3.3V tolerant input that stops all PCI and SRC clocks, except those set to be free running. |
| 10 | VDDIO_PCI3.3 | PWR | 3.3V power supply for the PCI outputs |
| 11 | PCI0 | OUT | 3.3V PCI clock output. |
| 12 | PCI1 | OUT | 3.3V PCI clock output. |
| 13 | PCI_F2 | OUT | Free running 3.3V PCI clock output |
| 14 | GNDPCI | PWR | Ground for PCI output clocks. |
| 15 | GND48 | PWR | Ground for the USB clock. |
| 16 | USB_48MHz | OUT | Fixed 3.3V 48MHz USB clock output |
| 17 | VDD48IO_3.3 | PWR | 3.3V Power supply for the 48MHz output |
| 18 | VDD48PLL_3.3 | PWR | 3.3V Power supply for the 48/96MHz PLL |
| 19 | VDDIO_96Mhz | PWR | Power supply for DOT96 output. VDD_IO = 1.05 to 3.3V +/-5%. |
| 20 | DOT96C_LPRS | OUT | Complement side of low-power CK505-type 96MHz differential clock. Rs is integrated (No external series resistor required). |
| 21 | DOT96T_LPRS | OUT | True side of low-power CK505-type 96MHz differential clock. Rs is integrated (No external series resistor required). |
| 22 | GND | PWR | Ground for 96MHz output |
| 23 | GND | PWR | Ground for LCD 100 MHz output. |
| 24 | LCD100C_LPRS | OUT | Complement side of low-power CK505-type LCD100MHz spreading differential clock. Rs is integrated (No external series resistor required). |
| 25 | LCD100T_LPRS | OUT | True side of low-power CK505-type LCD100MHz spreading differential clock. Rs is integrated (No external series resistor required). |
| 26 | VDDIO_LCD | PWR | Power supply for LCD100 output. VDD_IO = 1.05 to 3.3V +/-5%. |
| 27 | VDDLCDPLL_3.3 | PWR | 3.3V Power supply for the LCD100 Spreading PLL |
| 28 | CLKREQ1# | IN | Clock request input for SRC output pair 1. See the SRC, LCD, DOT Power Management Table for details |

Pin Description (continued)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|---------------|------|---|
| 29 | CLKREQ0# | IN | Clock request input for SRC output pair 0. See the SRC, LCD, DOT Power Management Table for details |
| 30 | SRC0C_LPRS | OUT | Complement side of low-power CK505-type SRC0 differential clock. Rs is integrated (No external series resistor required). |
| 31 | SRC0T_LPRS | OUT | True side of low-power CK505-type SRC0 differential clock. Rs is integrated (No external series resistor required). |
| 32 | SRC1C_LPRS | OUT | Complement side of low-power CK505-type SRC1 differential clock. Rs is integrated (No external series resistor required). |
| 33 | SRC1T_LPRS | OUT | True side of low-power CK505-type SRC1 differential clock. Rs is integrated (No external series resistor required). |
| 34 | GNSRC | PWR | Ground for SRC clocks |
| 35 | VDDIO_SRC | PWR | Power supply for SRC outputs. VDD_IO = 1.05 to 3.3V +/-5%. |
| 36 | SRC2C_LPRS | OUT | Complement side of low-power CK505-type SRC2 differential clock. Rs is integrated (No external series resistor required). |
| 37 | SRC2T_LPRS | OUT | True side of low-power CK505-type SRC2 differential clock. Rs is integrated (No external series resistor required). |
| 38 | SRC3C_LPRS | OUT | Complement side of low-power CK505-type SRC3 differential clock. Rs is integrated (No external series resistor required). |
| 39 | SRC3T_LPRS | OUT | True side of low-power CK505-type SRC3 differential clock. Rs is integrated (No external series resistor required). |
| 40 | VDDCORE_3.3 | PWR | 3.3V Power supply for 3.3V core |
| 41 | CLKREQ3# | IN | Clock request input for SRC output pair 3. See the SRC, LCD, DOT Power Management Table for details |
| 42 | CLKREQ2# | IN | Clock request input for SRC output pair 2. See the SRC, LCD, DOT Power Management Table for details |
| 43 | FSLB | IN | Low threshold Frequency Select input. See Table 1: CPU Frequency Select Table and the Vih_fs and Vil_fs specifications. |
| 44 | CPU_STOP# | IN | Stops all CPU clocks except those set to be free running. |
| 45 | CPUITPC_LPRS | OUT | Complement side of low-power CK505-type CPUITP differential clock. Rs is integrated (No external series resistor required). Note that this pin is NOT muxed with an SRC output. |
| 46 | CPUITPT_LPRS | OUT | True side of low-power CK505-type CPUITP differential clock. Rs is integrated (No external series resistor required). |
| 47 | CPU1C_LPRS | OUT | Complement side of low-power CK505-type CPU1 differential clock. Rs is integrated (No external series resistor required). Note that this pin is NOT muxed with an SRC output. |
| 48 | CPU1T_LPRS | OUT | True side of low-power CK505-type CPU1 differential clock. Rs is integrated (No external series resistor required). |
| 49 | VDDIO_CPU | PWR | Power supply for CPU outputs. VDD_IO = 1.05 to 3.3V +/-5%. |
| 50 | GNDCPU | PWR | Ground Pin for CPU Outputs |
| 51 | CPU0C_LPRS | OUT | Complement side of low-power CK505-type CPU1 differential clock. Rs is integrated (No external series resistor required). Note that this pin is NOT muxed with an SRC output. |
| 52 | CPU0T_LPRS | OUT | True side of low-power CK505-type CPU1 differential clock. Rs is integrated (No external series resistor required). |
| 53 | VDDCPUPLL_3.3 | PWR | 3.3V Power Supply for CPU PLL. |
| 54 | CK_PWRGD#/PD | IN | Notifies 9UMS9001 to sample latched inputs or enter power down mode. 1 = Power down mode Falling Edge = Sample latched inputs 0 = Normal operation |
| 55 | FSLC | IN | Low threshold Frequency Select input. See Table 1: CPU Frequency Select Table and the Vih_fs and Vil_fs specifications. |
| 56 | GNDREF | PWR | Ground pin for crystal oscillator circuit and REF output |

Functional Block Diagram



Power Groups

| Pin Number | | | Description |
|------------|-----------------|-----|----------------------|
| VDD3.3V | VDDIO 1.05~3.3V | GND | |
| | 49 | 50 | CPUCLK |
| 53 | | | Low power outputs |
| | | | Analog |
| 53 | | | Master Clock, Analog |
| | 35 | 34 | SRCCLK |
| 40 | | | Low power outputs |
| | | | Analog |
| | 26 | 23 | LCDCLK |
| 27 | | | Low power outputs |
| | | | PLL |
| | 19 | 22 | DOT 96Mhz |
| | | | Low power outputs |
| 17, 18 | | 15 | USB 48 |
| 3 | | 56 | Xtal, REF |
| 10 | | 14 | PCICLK |

Table 1: CPU Frequency Select Table

| FS _{LC} ¹ B0b7 | FS _L ¹ B0b6 | CPU MHz | SRC MHz | PCI MHz | REF MHz | USB MHz | DOT MHz |
|---------------------------------------|--------------------------------------|------------|------------|------------|------------|------------|------------|
| 0 | 0 | 133.33 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 |
| 0 | 1 | Reserved | | | | | |
| 1 | 0 | 100.00 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 |
| 1 | 1 | 200.00 | | | | | |

1. FS_{LC} is a low-threshold input. Please see V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.

Table 2: LCD Quick Configuration

| B1b3 | B1b2 | B1b1 | B1b0 | Pin 24/25 | Spread | Comment |
|------|------|------|------|-----------|---------------------|---------|
| | | | | MHz | % | |
| 0 | 0 | 0 | 0 | 100.00 | 0.25% Down Spread | LCDCLK |
| 0 | 0 | 0 | 1 | 100.00 | 0.5% Down Spread | LCDCLK |
| 0 | 0 | 1 | 0 | 100.00 | 1% Down Spread | LCDCLK |
| 0 | 0 | 1 | 1 | 100.00 | 1.25% Down Spread | LCDCLK |
| 0 | 1 | 0 | 0 | 100.00 | 1.5% Down Spread | LCDCLK |
| 0 | 1 | 0 | 1 | 100.00 | 2% Down Spread | LCDCLK |
| 0 | 1 | 1 | 0 | 100.00 | 2.5% Down Spread | LCDCLK |
| 0 | 1 | 1 | 1 | 100.00 | 3.0% Down Spread | LCDCLK |
| 1 | 0 | 0 | 0 | 100.00 | 0.25% Center Spread | LCDCLK |
| 1 | 0 | 0 | 1 | 100.00 | 0.5% Center Spread | LCDCLK |
| 1 | 0 | 1 | 0 | 100.00 | 1% Center Spread | LCDCLK |
| 1 | 0 | 1 | 1 | 100.00 | 1.25% Center Spread | LCDCLK |
| 1 | 1 | 0 | 0 | 100.00 | 1.5% Center Spread | LCDCLK |
| 1 | 1 | 0 | 1 | 100.00 | 2% Center Spread | LCDCLK |
| 1 | 1 | 1 | 0 | 100.00 | 2.5% Center Spread | LCDCLK |
| 1 | 1 | 1 | 1 | 100.00 | 3.0% Center Spread | LCDCLK |

Table 3: IO Vout select table

| B5b2 | B5b1 | B5b0 | IO_Vout |
|------|------|------|---------|
| 0 | 0 | 0 | 0.3V |
| 0 | 0 | 1 | 0.4V |
| 0 | 1 | 0 | 0.5V |
| 0 | 1 | 1 | 0.6V |
| 1 | 0 | 0 | 0.7V |
| 1 | 0 | 1 | 0.8V |
| 1 | 1 | 0 | 0.9V |
| 1 | 1 | 1 | 1.0V |

Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|------------------------|-----------------|-------------------------------------|-----------|-----|-------|-------|
| Maximum Supply Voltage | VDDxxx_3.3 | Supply Voltage | | 4.6 | V | 1,7 |
| Maximum Supply Voltage | VDDxxx_1.8 | Supply Voltage | | 2.3 | V | 1,7 |
| Maximum Supply Voltage | VDDxxx_IO | Low-Voltage Differential I/O Supply | | 3.8 | V | 1,7 |
| Maximum Input Voltage | V _{IH} | 3.3V LVCMOS Inputs | | 4.6 | V | 1,7,8 |
| Minimum Input Voltage | V _{IL} | Any Input | GND - 0.5 | | V | 1,7 |
| Storage Temperature | T _s | - | -65 | 150 | °C | 1,7 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | V | 1,7 |

Electrical Characteristics - Input/Supply/Common Output Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|--|-------------------------|--|-----------------------|-----------------------|-------|-------|
| Ambient Operating Temp | T _{ambient} | - | 0 | 70 | °C | 1 |
| Supply Voltage | VDDxxx_3.3 | Supply Voltage | 3.135 | 3.465 | V | 1 |
| Supply Voltage | VDDxxx_1.8 | Supply Voltage | 1.71 | 1.89 | V | 1 |
| Supply Voltage | VDDxxx_IO | Low-Voltage Differential I/O Supply | 1.05 | 3.465 | V | 1 |
| Input High Voltage | V _{IHSE} | Single-ended inputs | 2 | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{ILSE} | Single-ended inputs | V _{SS} - 0.3 | 0.8 | V | 1 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | 5 | uA | 1 |
| Input Leakage Current | I _{INRES} | Inputs with pull or pull down resistors V _{IN} = V _{DD} , V _{IN} = GND | -200 | 200 | uA | 1 |
| Output High Voltage | V _{OHSE} | Single-ended outputs, I _{OH} = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OLSE} | Single-ended outputs, I _{OL} = 1 mA | | 0.4 | V | 1 |
| Output High Voltage | V _{OHDF} | Differential Outputs | 0.7 | 0.9 | V | 1 |
| Output Low Voltage | V _{OLDIF} | Differential Outputs | | 0.4 | V | 1 |
| Low Threshold Input-High Voltage (Test Mode) | V _{IH_FS_TEST} | 3.3 V +/-5% | 2 | V _{DD} + 0.3 | V | 1 |
| Low Threshold Input-High Voltage | V _{IH_FS} | 3.3 V +/-5% | 0.7 | 1.5 | V | 1 |
| Low Threshold Input-Low Voltage | V _{IL_FS} | 3.3 V +/-5% | V _{SS} - 0.3 | 0.35 | V | 1 |
| Operating Supply Current | I _{DD_DEFAULT} | 3.3V supply, LCDPLL off | | 80 | mA | 1 |
| | I _{DD_LCDEN} | 3.3V supply, LCDPLL enabled | | 100 | mA | 1 |
| | I _{DD_IO} | 0.8V supply, Differential IO current, all outputs enabled | | 25 | mA | 1 |
| Power Down Current | I _{DD_PD3.3} | 3.3V supply, Power Down Mode | | 1 | mA | 1 |
| | I _{DD_PDIO} | 0.8V IO supply, Power Down Mode | | 0.1 | mA | 1 |
| Input Frequency | F _i | V _{DD} = 3.3 V | | 15 | MHz | 2 |
| Pin Inductance | L _{pin} | | | 7 | nH | 1 |
| Input Capacitance | C _{IN} | Logic Inputs | 1.5 | 5 | pF | 1 |
| | C _{OUT} | Output pin capacitance | | 6 | pF | 1 |
| | C _{INX} | X1 & X2 pins | | 7 | pF | 1 |
| Spread Spectrum Modulation Frequency | f _{SSMOD} | Triangular Modulation | 30 | 33 | kHz | 1 |

AC Electrical Characteristics - Input/Common Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|-------------------|-------------|---|-----|-----|-------|-------|
| Clk Stabilization | T_{STAB} | From VDD Power-Up or de-assertion of PD# to 1st clock | | 1.8 | ms | 1 |
| Tdrive_SRC | T_{DRSRC} | SRC output enable after PCI_STOP# de-assertion | | 15 | ns | 1 |
| Tdrive_PD# | T_{DRPD} | Differential output enable after PD# de-assertion | | 300 | us | 1 |
| Tdrive_CPU | T_{DRSRC} | CPU output enable after CPU_STOP# de-assertion | | 10 | ns | 1 |
| Tfall_PD# | T_{FALL} | Fall/rise time of PD#, PCI_STOP# and CPU_STOP# inputs | | 5 | ns | 1 |
| Trise_PD# | T_{RISE} | | | 5 | ns | 1 |

AC Electrical Characteristics - Low Power Differential Outputs

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|-----------------------------|----------------|--------------------------|------|------|-------|-------|
| Rising Edge Slew Rate | t_{SLR} | Differential Measurement | 1 | 4 | V/ns | 1,2 |
| Falling Edge Slew Rate | t_{FLR} | Differential Measurement | 1 | 4 | V/ns | 1,2 |
| Rise/Fall Time Variation | t_{SLVAR} | Single-ended Measurement | | 125 | ps | 1 |
| Maximum Output Voltage | V_{HIGH} | Includes overshoot | | 1150 | mV | 1 |
| Minimum Output Voltage | V_{LOW} | Includes undershoot | -300 | | mV | 1 |
| Differential Voltage Swing | V_{SWING} | Differential Measurement | 300 | | mV | 1 |
| Crossing Point Voltage | V_{XABS} | Single-ended Measurement | 300 | 550 | mV | 1,3,4 |
| Crossing Point Variation | $V_{XABSVAR}$ | Single-ended Measurement | | 140 | mV | 1,3,5 |
| Duty Cycle | D_{CYC} | Differential Measurement | 45 | 55 | % | 1 |
| CPU Jitter - Cycle to Cycle | $CPUJ_{C2C}$ | Differential Measurement | | 85 | ps | 1 |
| SRC Jitter - Cycle to Cycle | $SRCJ_{C2C}$ | Differential Measurement | | 125 | ps | 1 |
| DOT Jitter - Cycle to Cycle | $DOTJ_{C2C}$ | Differential Measurement | | 250 | ps | 1 |
| CPU[1:0] Skew | CPU_{SKEW10} | Differential Measurement | | 100 | ps | 1 |
| CPU[2:ITP:0] Skew | CPU_{SKEW20} | Differential Measurement | | 150 | ps | 1 |
| SRC[3:0] Skew | SRC_{SKEW} | Differential Measurement | | 250 | ps | 1 |

Electrical Characteristics - PCICLK/PCICLK_F

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|---------------------------|---------------|---|-----------|----------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -300 | 300 | ppm | 1,6 |
| Clock period | T_{period} | 33.33MHz output nominal | 29.99100 | 30.00900 | ns | 6 |
| | | 33.33MHz output spread | | 30.15980 | ns | 6 |
| Absolute min/max period | T_{abs} | 33.33MHz output nominal/spread | 29.49100 | 30.65980 | ns | 6 |
| Output High Voltage | V_{OH} | $I_{OH} = -1 \text{ mA}$ | 2.4 | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{OL} = 1 \text{ mA}$ | | 0.4 | V | 1 |
| Output High Current | I_{OH} | $V_{OH} @ \text{MIN} = 1.0 \text{ V}$ | -33 | | mA | 1 |
| | | $V_{OH} @ \text{MAX} = 3.135 \text{ V}$ | | -33 | mA | 1 |
| Output Low Current | I_{OL} | $V_{OL} @ \text{MIN} = 1.95 \text{ V}$ | 30 | | mA | 1 |
| | | $V_{OL} @ \text{MAX} = 0.4 \text{ V}$ | | 38 | mA | 1 |
| Rising Edge Slew Rate | t_{SLR} | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1 |
| Falling Edge Slew Rate | t_{FLR} | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1 |
| Duty Cycle | d_{t1} | $V_T = 1.5 \text{ V}$ | 45 | 55 | % | 1 |
| Skew | t_{skew} | $V_T = 1.5 \text{ V}$ | | 250 | ps | 1 |
| Intentional PCI-PCI delay | t_{delay} | $V_T = 1.5 \text{ V}$ | 0 nominal | | ps | 1,9 |
| Jitter, Cycle to cycle | $t_{cyc-cyc}$ | $V_T = 1.5 \text{ V}$ | | 500 | ps | 1 |

Electrical Characteristics - USB48MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|-------------------------|---------------|---|----------|----------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | 100 | ppm | 1,2 |
| Clock period | T_{period} | 48.00MHz output nominal | 20.83125 | 20.83542 | ns | 2 |
| Absolute min/max period | T_{abs} | 48.00MHz output nominal | 20.48130 | 21.18540 | ns | 2 |
| Output High Voltage | V_{OH} | $I_{OH} = -1 \text{ mA}$ | 2.4 | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{OL} = 1 \text{ mA}$ | | 0.4 | V | 1 |
| Output High Current | I_{OH} | $V_{OH} @ \text{MIN} = 1.0 \text{ V}$ | -29 | | mA | 1 |
| | | $V_{OH} @ \text{MAX} = 3.135 \text{ V}$ | | -23 | mA | 1 |
| Output Low Current | I_{OL} | $V_{OL} @ \text{MIN} = 1.95 \text{ V}$ | 29 | | mA | 1 |
| | | $V_{OL} @ \text{MAX} = 0.4 \text{ V}$ | | 27 | mA | 1 |
| Rising Edge Slew Rate | t_{SLR} | Measured from 0.8 to 2.0 V | 1 | 2 | V/ns | 1 |
| Falling Edge Slew Rate | t_{FLR} | Measured from 2.0 to 0.8 V | 1 | 2 | V/ns | 1 |
| Duty Cycle | d_{11} | $V_T = 1.5 \text{ V}$ | 45 | 55 | % | 1 |
| Jitter, Cycle to cycle | $t_{jcy-cyc}$ | $V_T = 1.5 \text{ V}$ | | 350 | ps | 1 |

Electrical Characteristics - SMBus Interface

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|---|--------------|---|-----|------|-------|-------|
| SMBus Voltage | V_{DD} | | 2.7 | 5.5 | V | 1 |
| Low-level Output Voltage | V_{OLSMB} | @ I_{PULLUP} | | 0.4 | V | 1 |
| Current sinking at $V_{OLSMB} = 0.4 \text{ V}$ | I_{PULLUP} | SMB Data Pin | 4 | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time | T_{RI2C} | (Max VIL - 0.15) to (Min VIH + 0.15) | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time | T_{FI2C} | (Min VIH + 0.15) to (Max VIL - 0.15) | | 300 | ns | 1 |
| Maximum SMBus Operating Frequency | F_{SMBUS} | Block Mode | | 100 | kHz | 1 |

Electrical Characteristics - REF-14.318MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|-------------------------|----------------------|---|---------|----------|-------|-------|
| Long Accuracy | ppm | see T _{period} min-max values | -300 | 300 | ppm | 1,2 |
| Clock period | T _{period} | 14.318MHz output nominal | 69.8203 | 69.8622 | ns | 2 |
| Absolute min/max period | T _{abs} | 14.318MHz output nominal | 69.8203 | 70.86224 | ns | 2 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | 0.4 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @ MIN = 1.0 V, V _{OH} @ MAX = 3.135 V | -33 | -33 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @ MIN = 1.95 V, V _{OL} @ MAX = 0.4 V | 30 | 38 | mA | 1 |
| Rising Edge Slew Rate | t _{SLR} | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1 |
| Falling Edge Slew Rate | t _{FLR} | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1 |
| Duty Cycle | d _{t1} | V _T = 1.5 V | 45 | 55 | % | 1 |
| Jitter | t _{jyc-cyc} | V _T = 1.5 V | | 1000 | ps | 1 |

Notes on Electrical Characteristics:

¹Guaranteed by design and characterization, not 100% tested in production.

²Slew rate measured through V_{swing} centered around differential zero

³V_{xabs} is defined as the voltage where CLK = CLK#

⁴Only applies to the differential rising edge (CLK rising and CLK# falling)

⁵Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#. The average cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations

⁶All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

⁷Operation under these conditions is neither implied, nor guaranteed.

⁸Maximum input voltage is not to exceed maximum VDD

⁹See PCI Clock-to-Clock Delay Figure

General I²C serial interface information for the 9UMS9001

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
(see Note 2)
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | |
|---------------------------------|-----------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address D2 _(H) | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | | X Byte |
| | ○ | |
| | ○ | |
| | ○ | |
| | ○ | |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if X_(H) was written to byte 8)**.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|---------------------------------|-----------------|----------------------|------------------|
| Controller (Host) | | ICS (Slave/Receiver) | |
| T | starT bit | | |
| Slave Address D2 _(H) | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| RT | Repeat starT | | |
| Slave Address D3 _(H) | | | |
| RD | ReaD | | |
| | | ACK | |
| | | Data Byte Count = X | |
| ACK | | | |
| ACK | | X Byte | |
| | | | Beginning Byte N |
| | | | ○ |
| | | | ○ |
| | | | ○ |
| | | ○ | |
| | | Byte N + X - 1 | |
| N | Not acknowledge | | |
| P | stoP bit | | |

Byte 0 FS Readback, SS Enable, STOP Control Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|------------|--|------|----------------------------|--------------------------------------|---------|
| 7 | - | FSLC | CPU Freq. Sel. Bit MSB | RW | See Frequency Select Table | | Latch |
| 6 | | FSLB | CPU Freq. Sel. Bit LSB | RW | | | Latch |
| 5 | | CPU_SS_EN | Spread spectrum enable for CPU/SRC/PCI outputs | RW | SS Disabled | SS Enabled | 1 |
| 4 | | LCD_Enable | Turns On LCD PLL | RW | Off | On | 1 |
| 3 | | SRC3_STOP | SRC 3 Stop Control | RW | Free Running | Stops with PCI_STOP# Assertion | 0 |
| 2 | | SRC2_STOP | SRC 2 Stop Control | RW | | | 0 |
| 1 | | SRC1_STOP | SRC 1 Stop Control | RW | | | 0 |
| 0 | | SRC0_STOP | SRC 0 Stop Control | RW | | | 0 |

Byte 1 LCD Quick Config and CPU Stop Control Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|--------------|---------------------------|------|--------------------------------------|--------------------------------------|---------|
| 7 | | CPU_ITP_STOP | CPU ITP Stop Control | RW | Free Running | Stops with CPU_STOP# assertion | 0 |
| 6 | | CPU1_STOP | CPU1 Stop Control | RW | | | 1 |
| 5 | | CPU0_STOP | CPU0 Stop Control | RW | | | 1 |
| 4 | | LCD_SS_EN | Turns on SS for LCD PLL | RW | Off | On | 1 |
| 3 | | LCD_SSC_SEL | Select down or center SSC | RW | Down spread | Center spread | 0 |
| 2 | | LCD_CF2 | PLL3 Quick Config Bit 2 | RW | See Table 2: LCD Quick Configuration | | 0 |
| 1 | | LCD_CF1 | PLL3 Quick Config Bit 1 | RW | | | 0 |
| 0 | | LCD_CF0 | PLL3 Quick Config Bit 0 | RW | | | 1 |

Byte 2 Output Enable and Stop Control Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|-------------|-------------------------------|------|-----------------|--------------------------------------|---------|
| 7 | | PCI_F2_STOP | Free running PCI Stop Control | RW | Free Running | Stops with PCI_STOP# assertion | 0 |
| 6 | | PCI1_STOP | PCI1 Stop Control | RW | | | 1 |
| 5 | | PCI0_STOP | PCI 0 Stop Control | RW | | | 1 |
| 4 | | REF_OE | Output enable for REF | RW | Output Disabled | Output Enabled | 1 |
| 3 | | USB_OE | Output enable for USB | RW | Output Disabled | Output Enabled | 1 |
| 2 | | PCIF2_OE | Output enable for PCI2 | RW | Output Disabled | Output Enabled | 1 |
| 1 | | PCI1_OE | Output enable for PCI1 | RW | Output Disabled | Output Enabled | 1 |
| 0 | | PCI0_OE | Output enable for PCI0 | RW | Output Disabled | Output Enabled | 1 |

Byte 3 Output Enable Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|------------|---------------------------|------|-----------------|----------------|---------|
| 7 | | CPU_ITP_OE | Output enable for CPU_ITP | RW | Output Disabled | Output Enabled | 1 |
| 6 | | CPU1_OE | Output enable for CPU1 | RW | Output Disabled | Output Enabled | 1 |
| 5 | | CPU0_OE | Output enable for CPU0 | RW | Output Disabled | Output Enabled | 1 |
| 4 | | Reserved | Reserved | RW | | | 0 |
| 3 | | SRC3_OE | Output enable for SRC4 | RW | Output Disabled | Output Enabled | 1 |
| 2 | | SRC2_OE | Output enable for SRC4 | RW | Output Disabled | Output Enabled | 1 |
| 1 | | SRC1_OE | Output enable for SRC4 | RW | Output Disabled | Output Enabled | 1 |
| 0 | | SRC0_OE | Output enable for SRC4 | RW | Output Disabled | Output Enabled | 1 |

Byte 4 Output Enable and CLKREQ# Control Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|-----------|--------------------------|------|------------------------------|--------------------------|---------|
| 7 | | DOT96_OE | Output enable for DOT96 | RW | Output Disabled | Output Enabled | 1 |
| 6 | | LCD100_OE | Output enable for LCD100 | RW | Output Disabled | Output Enabled | 1 |
| 5 | | Reserved | Reserved | RW | | | 0 |
| 4 | | Reserved | Reserved | RW | | | 0 |
| 3 | | SRC3_CR | SRC3 CLKREQ3# Enable | RW | Not controlled by CLKREQ# | Controlled by CLKREQ# | 0 |
| 2 | | SRC2_CR | SRC2 CLKREQ2# Enable | RW | | | 0 |
| 1 | | SRC1_CR | SRC1 CLKREQ1# Enable | RW | | | 0 |
| 0 | | SRC0_CR | SRC0 CLKREQ0# Enable | RW | | | 0 |

Byte 5 Drive Strength Control Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|-----------------|--|------|--|---------|---------|
| 7 | | PCI_F2 Strength | Sets the PCI_F2 output drive strength | RW | 1 Load | 2 Loads | 1 |
| 6 | | PCI1 Strength | Sets the PCI1 output drive strength | RW | | | 1 |
| 5 | | PCI0 Strength | Sets the PCI0 output drive strength | RW | | | 1 |
| 4 | | 48MHz Strength | Sets the 48MHz output drive strength | RW | | | 1 |
| 3 | | REF Strength | Sets the REF output drive strength | RW | 2 Loads | 3 Loads | 1 |
| 2 | | IO_VOUT2 | IO Output Voltage Select (Most Significant Bit) | RW | See Table 3: V_IO Selection (Default is 0.8V) | | 1 |
| 1 | | IO_VOUT1 | IO Output Voltage Select | RW | | | 0 |
| 0 | | IO_VOUT0 | IO Output Voltage Select (Least Significant Bit) | RW | | | 1 |

Byte 6 Reserved Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|----------|-------------|------|---|---|---------|
| 7 | | Reserved | Reserved | RW | | | 0 |
| 6 | | Reserved | Reserved | RW | | | 0 |
| 5 | | Reserved | Reserved | RW | | | 0 |
| 4 | | Reserved | Reserved | RW | | | 0 |
| 3 | | Reserved | Reserved | RW | | | 0 |
| 2 | | Reserved | Reserved | RW | | | 0 |
| 1 | | Reserved | Reserved | RW | | | 0 |
| 0 | | Reserved | Reserved | RW | | | 0 |

Byte 7 Vendor ID/ Revision ID

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|-----------------|----------------------------------|------|-----------------|---|---------|
| 7 | | Rev Code Bit 3 | Revision ID | R | Vendor specific | | X |
| 6 | | Rev Code Bit 2 | | R | | | X |
| 5 | | Rev Code Bit 1 | | R | | | X |
| 4 | | Rev Code Bit 0 | | R | | | X |
| 3 | | Vendor ID bit 3 | Vendor ID ICS is 0001, binary | R | | | 0 |
| 2 | | Vendor ID bit 2 | | R | | | 0 |
| 1 | | Vendor ID bit 1 | | R | | | 0 |
| 0 | | Vendor ID bit 0 | | R | 1 | | |

Byte 8 Device ID Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|------------|-----------------|------|------------------------------------|---|---------|
| 7 | | Device_ID3 | Package ID code | R | Device ID = 0011 Hex 56-pin QFN | | 0 |
| 6 | | Device_ID2 | | R | | | 0 |
| 5 | | Device_ID1 | | R | | | 1 |
| 4 | | Device_ID0 | | R | | | 1 |
| 3 | | Reserved | Reserved | RW | | | 0 |
| 2 | | Reserved | Reserved | RW | | | 0 |
| 1 | | Reserved | Reserved | RW | | | 0 |
| 0 | | Reserved | Reserved | RW | | | 1 |

Byte 9 Test Mode Register

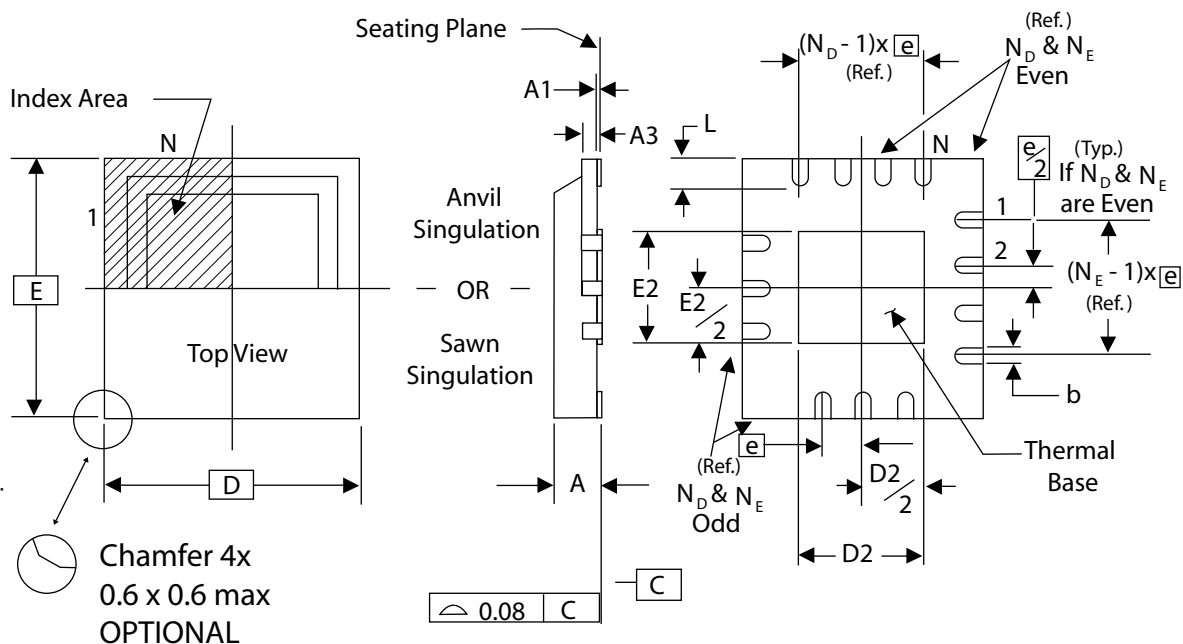
| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|------------------|--|------|------------------|--------------------------------------|---------|
| 7 | | LCD_STOP | LCD Stop Control | RW | Free Running | Stops with PCI_STOP# assertion | 0 |
| 6 | | Reserved | Reserved | RW | | | 0 |
| 5 | | Reserved | Reserved | RW | | | 0 |
| 4 | | Test Mode Select | Allows test select, ignores Test Sel input pin | RW | Outputs HI-Z | Outputs = REF/N | 0 |
| 3 | | Test Mode Entry | Enters into test mode, ignores input pin | RW | Normal operation | Test mode | 0 |
| 2 | | Reserved | Reserved | RW | | | 0 |
| 1 | | Reserved | Reserved | RW | | | 0 |
| 0 | | PLL1_SS | PLL1 Spread Spectrum Mode | RW | Down-spread | Center-spread | 0 |

Test Clarification Table

| Comments | HW | | SW | | OUTPUT |
|--|--------------------|---------------------|---------------------------|--------------------------|--------|
| | TEST_SEL HW PIN | TEST_MODE HW PIN | TEST ENTRY BIT B9b3 | REF/N or HI-Z B9b4 | |
| | <2.0V | X | 0 | 0 | NORMAL |
| Power-up w/ TEST_SEL = 1 to enter test mode Cycle power to disable test mode TEST_MODE -->low Vth input TEST_MODE is a real time input | >2.0V | 0 | X | 0 | HI-Z |
| | >2.0V | 0 | X | 1 | REF/N |
| | >2.0V | 1 | X | 0 | REF/N |
| | >2.0V | 1 | X | 1 | REF/N |
| If TEST_SEL HW pin is 0 during power-up, test mode can be invoked through B9b3. If test mode is invoked by B9b3, only B9b4 is used to select HI-Z or REF/N FSLB/TEST_Mode pin is not used. Cycle power to disable test mode, one shot control | <2.0V | X | 1 | 0 | HI-Z |
| | <2.0V | X | 1 | 1 | REF/N |

B9b3: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)

B9b4: 1= REF/N, Default = 0 (HI-Z)



THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS

| SYMBOL | MIN. | MAX. |
|--------|----------------|------|
| A | 0.8 | 1.0 |
| A1 | 0 | 0.05 |
| A3 | 0.25 Reference | |
| b | 0.18 | 0.3 |
| e | 0.50 BASIC | |

DIMENSIONS

| SYMBOL | ICS 56L TOLERANCE |
|----------------|-------------------|
| N | 56 |
| N_D | 14 |
| N_E | 14 |
| D x E BASIC | 8.00 x 8.00 |
| D2 MIN. / MAX. | 4.35 / 4.65 |
| E2 MIN. / MAX. | 5.05 / 5.35 |
| L MIN. / MAX. | 0.30 / 0.50 |

Ordering Information

| Part / Order Number | Shipping Package | Package | Temperature |
|---------------------|------------------|------------|-------------|
| 9UMS9001AKLF | Tubes | 56-pin MLF | 0 to +70° C |
| 9UMS9001AKLFT | Tape and Reel | 56-pin MLF | 0 to +70° C |

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

Revision History

| Rev. | Issue Date | Who | Description | Page # |
|------|------------|-----|--|----------|
| A | 8/28/2008 | RDW | 1. Removed CK505 reference is Device ID byte of SMBus 2. Moved SMBus AFTER electrical characteristics 3. Made Data sheet Rev A device. 4. Move to Final | 8, 9, 10 |
| B | 7/19/2010 | RDW | 1. Corrected Pin type for Pins 8, 21, 23. | 2 |
| C | 6/16/2011 | RDW | 1. Corrected typo in pin name for pin 29. 2. Corrected typo in pin description for pin 41. | 1, 2, 3 |

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