ISL6615

High-Frequency 6A Sink Synchronous MOSFET Drivers with Protection Features

FN6481
Rev 0.00
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The ISL6615 is a high-speed MOSFET driver optimized to drive upper and lower power N-Channel MOSFETs in a synchronous rectified buck converter topology. This driver, combined with an Intersil Digital or Analog multiphase PWM controller, forms a complete high frequency and high efficiency voltage regulator.

The ISL6615 drives both upper and lower gates over a range of 4.5V to 13.2V. This drive-voltage provides the flexibility necessary to optimize applications involving trade-offs between gate charge and conduction losses.

The ISL6615 features 6A typical sink current for the low-side gate driver, enhancing the lower MOSFET gate hold-down capability during PHASE node rising edge, preventing power loss caused by the self turn-on of the lower MOSFET due to the high dV/dt of the switching node.

An advanced adaptive zero shoot-through protection is integrated to prevent both the upper and lower MOSFETs from conducting simultaneously and to minimize the dead time. The ISL6615 includes an overvoltage protection feature operational before VCC exceeds its turn-on threshold, at which the PHASE node is connected to the gate of the low side MOSFET (LGATE). The output voltage of the converter is then limited by the threshold of the low side MOSFET, which provides some protection to the load if the upper MOSFET(s) is shorted.

The ISL6615 also features an input that recognizes a high-impedance state, working together with Intersil multiphase PWM controllers to prevent negative transients on the controlled output voltage when operation is suspended. This feature eliminates the need for the Schottky diode that may be utilized in a power system to protect the load from negative output voltage damage.

Features

- Dual MOSFET Drives for Synchronous Rectified Bridge
- Advanced Adaptive Zero Shoot-Through Protection
  - Body Diode Detection
  - LGATE Detection
  - Auto-zero of $r_{DS(ON)}$ Conduction Offset Effect
- Adjustable Gate Voltage for Optimal Efficiency
- 36V Internal Bootstrap Schottky Diode
- Bootstrap Capacitor Overcharging Prevention
- Supports High Switching Frequency (up to 1MHz)
  - 6A LGATE Sinking Current Capability
  - Fast Rise/Fall Times and Low Propagation Delays
- Support 3.3V PWM Input logic
- Tri-State PWM Input for Safe Output Stage Shutdown
- Tri-State PWM Input Hysteresis for Applications with Power Sequencing Requirement
- Pre-POR Overvoltage Protection
- VCC Undervoltage Protection
- Expandable Bottom Copper PAD for Better Heat Spreading
- Dual Flat No-Lead (DFN) Package
  - Near Chip-Scale Package Footprint; Improves PCB Efficiency and Thinner in Profile
- Pb-Free (RoHS Compliant)

Applications

- Optimized for POL DC/DC Converters for IBA Systems
- Core Regulators for Intel® and AMD® Microprocessors
- High Current Low-Profile DC/DC Converters
- High Frequency and High Efficiency VRM and VRD
- Synchronous Rectification for Isolated Power Supplies

Related Literature

Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

Technical Brief TB389 “PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages”

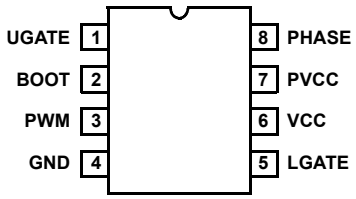
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6615CBZ*	6615 CBZ	0 to +70	8 Ld SOIC	M8.15
ISL6615CRZ*	6615	0 to +70	10 Ld 3x3 DFN	L10.3x3
ISL6615IBZ*	6615 IBZ	-40 to +70	8 Ld SOIC	M8.15
ISL6615IRZ*	615I	-40 to +70	10 Ld 3x3 DFN	L10.3x3

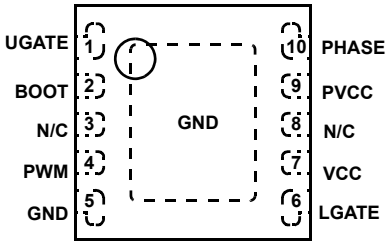
*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

ISL6615
(8 LD SOIC)
TOP VIEW



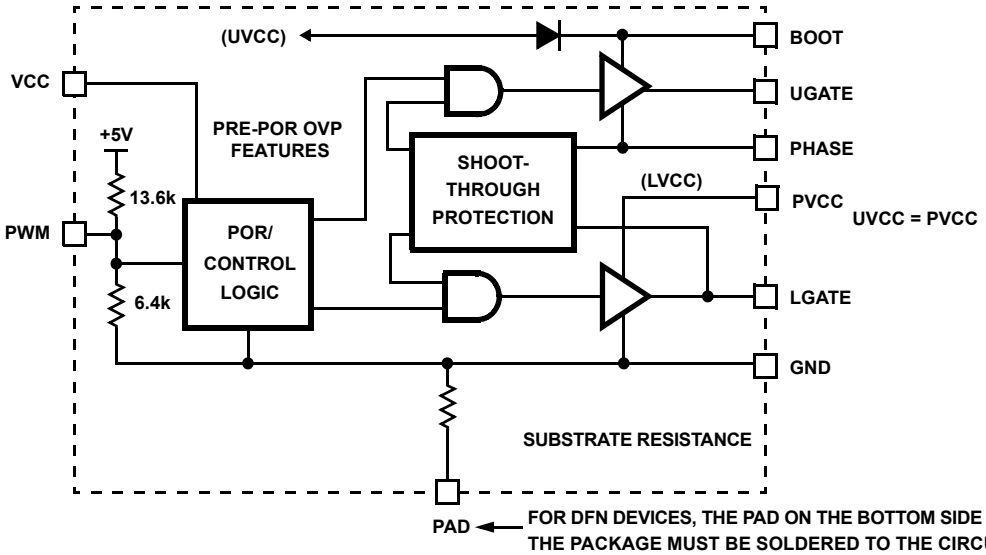
ISL6615
(10 LD 3x3 DFN)
TOP VIEW



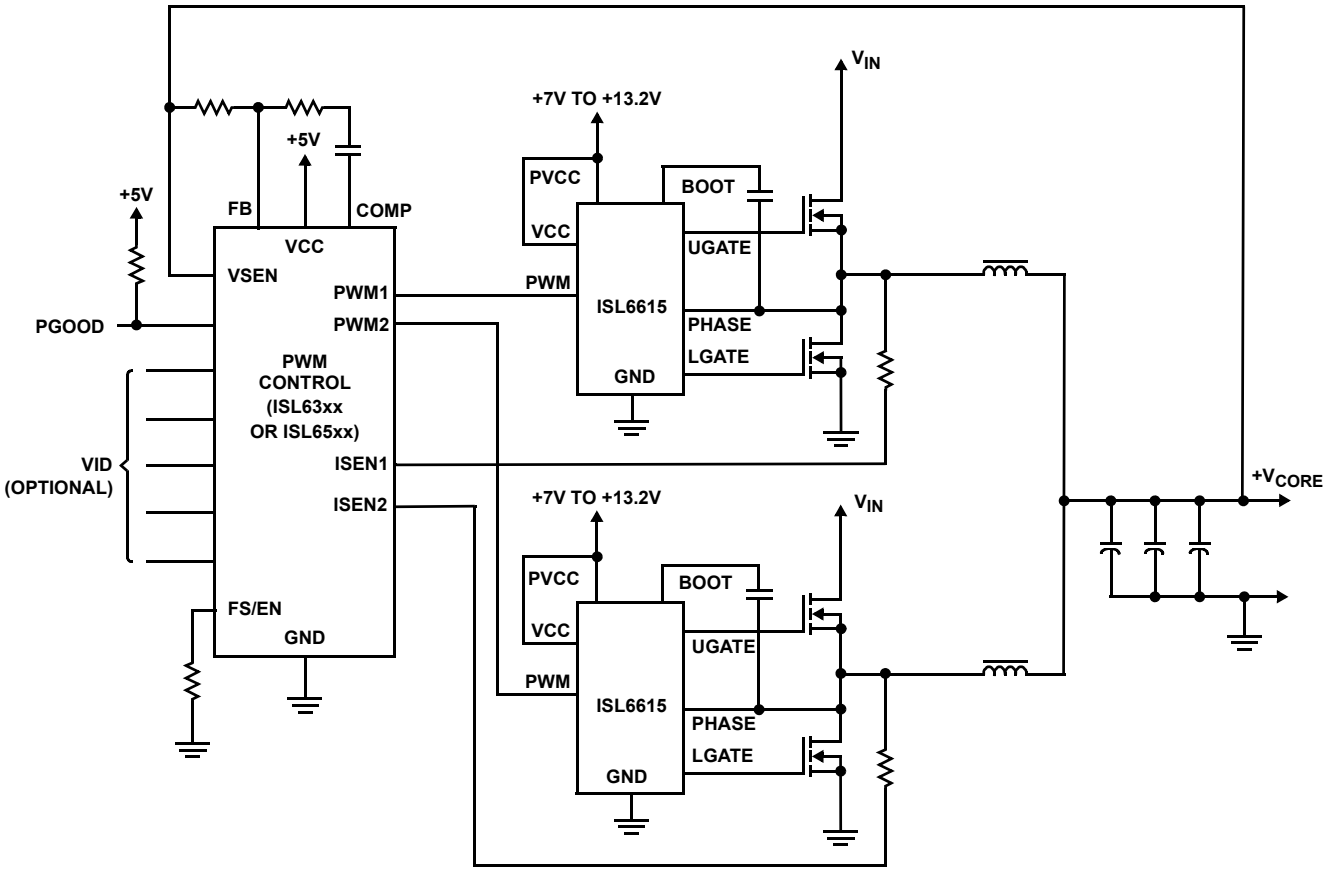
RECOMMEND TO CONNECT PIN 3 TO GND AND PIN 8 TO PVCC

Block Diagram

ISL6615



Typical Application - 2 Channel Converter



ISL6615 CAN SUPPORT 3.3V OR 5V PWM INPUT

Absolute Maximum Ratings

Supply Voltage (VCC) 15V
Supply Voltage (PVCC) . . . . . VCC + 0.3V
BOOT Voltage ($V_{BOOT-GND}$) 36V
Input Voltage (V_{PWM}) . . . . . GND - 0.3V to 7V
UGATE . . . . . V_{PHASE} - 0.3V_{DC} to V_{BOOT} + 0.3V
V_{PHASE} - 3.5V (<100ns Pulse Width, 2µJ) to V_{BOOT} + 0.3V
LGATE . . . . . GND - 0.3V_{DC} to V_{PVCC} + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to V_{PVCC} + 0.3V
PHASE . . . . . GND - 0.3V_{DC} to 15V_{DC}
GND - 8V (<400ns, 20µJ) to 30V (<200ns, $V_{BOOT-GND}$ < 36V))
ESD Rating
Human Body Model . . . . . Class I JEDEC STD

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	100	N/A
DFN Package (Notes 2, 3)	48	7

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range
ISL6615CRZ, ISL6615CBZ . . . . . 0°C to +70°C
ISL6615IRZ, ISL6615IBZ . . . . . -40°C to +85°C
Maximum Operating Junction Temperature . . . . . +125°C
VCC Supply Voltage . . . . . 6.8V to 13.2V
PVCC Supply Voltage . . . . . 5V to 12V ±10%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Bias Supply Current	I_{VCC}	f_{PWM} = 300kHz, V_{VCC} = 12V	-	4.5	-	mA
Gate Drive Bias Current	I_{PVCC}	f_{PWM} = 300kHz, V_{PVCC} = 12V	-	8	-	mA
POWER-ON RESET AND ENABLE						
VCC Rising Threshold			6.1	6.4	6.7	V
VCC Falling Threshold			4.7	5.0	5.3	V
PWM INPUT (See “TIMING DIAGRAM” on page 6)						
Input Current	I_{PWM}	V_{PWM} = 3.3V	-	365	-	µA
		V_{PWM} = 0V	-	-350	-	µA
PWM Rising Threshold (Note 4)		VCC = 12V	-	1.70	-	V
PWM Falling Threshold (Note 4)		VCC = 12V	-	1.30	-	V
Typical Tri-State Shutdown Window		VCC = 12V	1.32	-	1.82	V
Tri-State Lower Gate Falling Threshold		VCC = 12V	-	1.18	-	V
Tri-State Lower Gate Rising Threshold		VCC = 12V	-	0.76	-	V
Tri-State Upper Gate Rising Threshold		VCC = 12V	-	2.36	-	V
Tri-State Upper Gate Falling Threshold		VCC = 12V	-	1.96	-	V
Shutdown Holdoff Time	t_{TSSHD}		-	65	-	ns
UGATE Rise Time (Note 4)	t_{RU}	V_{PVCC} = 12V, 3nF Load, 10% to 90%	-	13	-	ns
LGATE Rise Time (Note 4)	t_{RL}	V_{PVCC} = 12V, 3nF Load, 10% to 90%	-	10	-	ns
UGATE Fall Time (Note 4)	t_{FU}	V_{PVCC} = 12V, 3nF Load, 90% to 10%	-	10	-	ns
LGATE Fall Time (Note 4)	t_{FL}	V_{PVCC} = 12V, 3nF Load, 90% to 10%	-	10	-	ns

Electrical Specifications Recommended Operating Conditions; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UGATE Turn-On Propagation Delay (Note 4)	t_{PDHU}	V_{PVCC} = 12V, 3nF Load, Adaptive	-	10	-	ns
LGATE Turn-On Propagation Delay (Note 4)	t_{PDHL}	V_{PVCC} = 12V, 3nF Load, Adaptive	-	10	-	ns
UGATE Turn-Off Propagation Delay (Note 4)	t_{PDLU}	V_{PVCC} = 12V, 3nF Load	-	10	-	ns
LGATE Turn-Off Propagation Delay (Note 4)	t_{PDLL}	V_{PVCC} = 12V, 3nF Load	-	10	-	ns
LG/UG Tri-State Propagation Delay (Note 4)	t_{PDTS}	V_{PVCC} = 12V, 3nF Load	-	10	-	ns
OUTPUT (Note 4)						
Upper Drive Source Current	I_{U_SOURCE}	V_{PVCC} = 12V, 3nF Load	-	2.5	-	A
Upper Drive Source Impedance	R_{U_SOURCE}	150mA Source Current	-	1	-	Ω
Upper Drive Sink Current	I_{U_SINK}	V_{PVCC} = 12V, 3nF Load	-	4	-	A
Upper Drive Sink Impedance	R_{U_SINK}	150mA Sink Current	-	0.8	-	Ω
Lower Drive Source Current	I_{L_SOURCE}	V_{PVCC} = 12V, 3nF Load	-	4	-	A
Lower Drive Source Impedance	R_{L_SOURCE}	150mA Source Current	-	0.7	-	Ω
Lower Drive Sink Current	I_{L_SINK}	V_{PVCC} = 12V, 3nF Load	-	6	-	A
Lower Drive Sink Impedance	R_{L_SINK}	150mA Sink Current	-	0.45	-	Ω

NOTE:

4. Limits established by characterization and are not production tested.

Functional Pin Description

PACKAGE PIN #		PIN SYMBOL	FUNCTION
SOIC	DFN		
1	1	UGATE	Upper gate drive output. Connect to gate of high-side power N-Channel MOSFET.
2	2	BOOT	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the “TIMING DIAGRAM” on page 6 under Description for guidance in choosing the capacitor value.
-	3, 8	N/C	No Connection. Recommend to connect pin 3 to GND and pin 8 to PVCC.
3	4	PWM	The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the “TIMING DIAGRAM” on page 6 section under Description for further details. Connect this pin to the PWM output of the controller.
4	5	GND	Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver.
5	6	LGATE	Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.
6	7	VCC	Its operating range is +6.8V to 13.2V. Place a high quality low ESR ceramic capacitor from this pin to GND.
7	9	PVCC	This pin supplies power to both upper and lower gate drives. Its operating range is +4.5V to 13.2V. Place a high quality low ESR ceramic capacitor from this pin to GND.
8	10	PHASE	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET. This pin provides a return path for the upper gate drive.
9	11	PAD	Connect this pad to the power ground plane (GND) via thermally enhanced connection.

Description

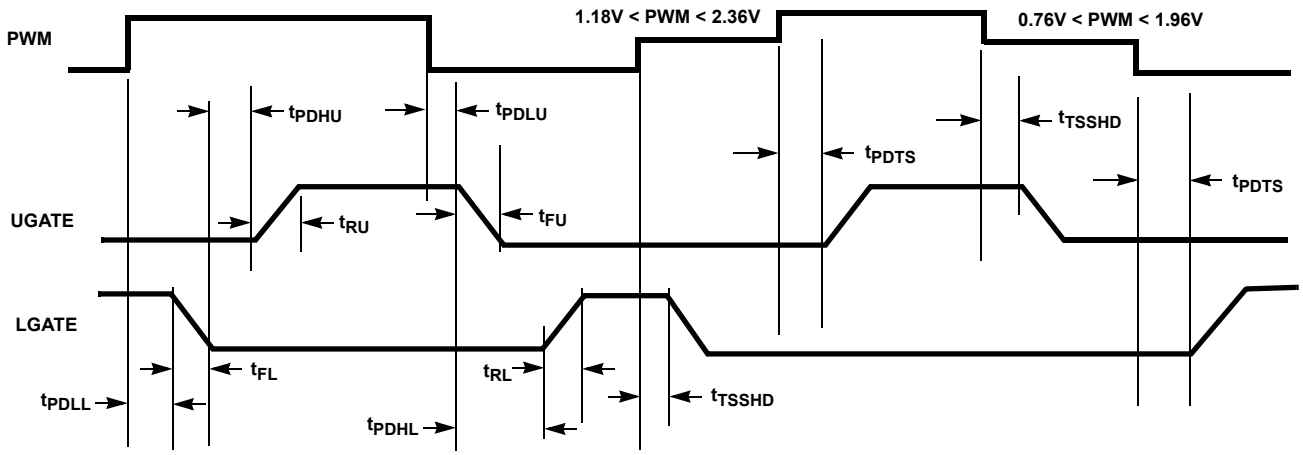


FIGURE 1. TIMING DIAGRAM

Operation

Designed for versatility and speed, the ISL6615 MOSFET driver controls both high-side and low-side N-Channel FETs of a half-bridge power train from one externally provided PWM signal.

Prior to VCC exceeding its POR level, the Pre-POR overvoltage protection function is activated during initial start-up; the upper gate (UGATE) is held low and the lower gate (LGATE), controlled by the Pre-POR overvoltage protection circuits, is connected to the PHASE. Once the VCC voltage surpasses the VCC Rising Threshold (see "Electrical Specifications" on page 4), the PWM signal takes control of gate transitions. A rising edge on PWM initiates the turn-off of the lower MOSFET (see Figure 1). After a short propagation delay [t_{PDLL}], the lower gate begins to fall. Typical fall times [t_{FL}] are provided in the "Electrical Specifications" on page 4. Adaptive shoot-through circuitry monitors the LGATE voltage and determines the upper gate delay time [t_{PDHU}]. This prevents both the lower and upper MOSFETs from conducting simultaneously. Once this delay period is complete, the upper gate drive begins to rise [t_{RU}] and the upper MOSFET turns on.

A falling transition on PWM results in the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [t_{PDLU}] is encountered before the upper gate begins to fall [t_{FU}]. Again, the adaptive shoot-through circuitry determines the lower gate delay time, t_{PDHL}. The PHASE voltage and the UGATE voltage are monitored, and the lower gate is allowed to rise after PHASE drops below a level or the voltage of UGATE to PHASE reaches a level depending upon the current direction (see the following section titled "Advanced Adaptive Zero Shoot-through Dead-time Control" for details). The lower gate then rises [t_{RL}], turning on the lower MOSFET.

Advanced Adaptive Zero Shoot-through Dead-time Control

The ISL6615 driver incorporates a unique adaptive dead-time control technique to minimize dead-time, resulting in high efficiency from the reduced freewheeling time of the lower MOSFETs' body-diode conduction, and to prevent the upper and lower MOSFETs from conducting simultaneously. This is accomplished by ensuring the rising gate turns on its MOSFET with minimum and sufficient delay after the other has turned off.

During turn-off of the lower MOSFET, the LGATE voltage is monitored until it drops below 1.75V. Prior to reaching this level, there is a 25ns blanking period to protect against sudden dips in the LGATE voltage. Once 1.75V is reached the UGATE is released to rise after 20ns of propagation delay. Once the PHASE is high, the adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during PWM falling edge and subsequent UGATE turn-off. If PHASE falls to less than +0.8V, the LGATE is released to turn on after 10ns of propagation delay. If the UGATE-PHASE falls to less than 1.75V and after 40ns of propagation delay, LGATE is released to rise.

Tri-state PWM Input

A unique feature of these drivers and other Intersil drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the driver outputs are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the "Electrical Specifications" on page 4 determine when the lower and upper gates are enabled.

This feature helps prevent a negative transient on the output voltage when the output is shut down, eliminating the

Schottky diode that is used in some systems for protecting the load from reversed output voltage events.

In addition, more than 400mV hysteresis also incorporates into the Tri-state shutdown window to eliminate PWM input oscillations due to the capacitive load seen by the PWM input through the body diode of the controller's PWM output when the power-up and/or power-down sequence of bias supplies of the driver and PWM controller are required.

Power-On Reset (POR) Function

During initial start-up, the VCC voltage rise is monitored. Once the rising VCC voltage exceeds 6.4V (typically), operation of the driver is enabled and the PWM input signal takes control of the gate drives. If VCC drops below the falling threshold of 5.0V (typically), operation of the driver is disabled.

Pre-POR Overvoltage Protection

Prior to VCC exceeding its POR level, the upper gate is held low and the lower gate is controlled by the overvoltage protection circuits. The upper gate driver is powered from PVCC and will be held low when a voltage of 2.75V or higher is present on PVCC as VCC surpasses its POR threshold. The PHASE is connected to the gate of the low side MOSFET (LGATE), which provides some protection to the microprocessor if the upper MOSFET(s) is shorted during start-up, normal, or shutdown conditions. For complete protection, the low side MOSFET should have a gate threshold well below the maximum voltage rating of the load/microprocessor.

Internal Bootstrap Device

Both drivers feature an internal bootstrap Schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the trailing-edge of the PHASE node. This reduces voltage stress on the boot to phase pins.

The bootstrap capacitor must have a maximum voltage rating above PVCC + 5V and its capacitance value can be chosen from Equation 1:

$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}} \qquad \text{(EQ. 1)}$$

$$Q_{GATE} = \frac{Q_{G1} \bullet PVCC}{V_{GS1}} \bullet N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive.

As an example, suppose two IRLR7821 FETs are chosen as the upper MOSFETs. The gate charge, Q_G, from the data sheet is 10nC at 4.5V (V_{GS}) gate-source voltage. Then the Q_{GATE} is calculated to be 53nC for PVCC = 12V. We will assume a 200mV droop in drive voltage over the PWM cycle. We find that a bootstrap capacitance of at least 0.267µF is required. The next larger standard value capacitance is 0.33µF. A good quality ceramic capacitor is recommended.

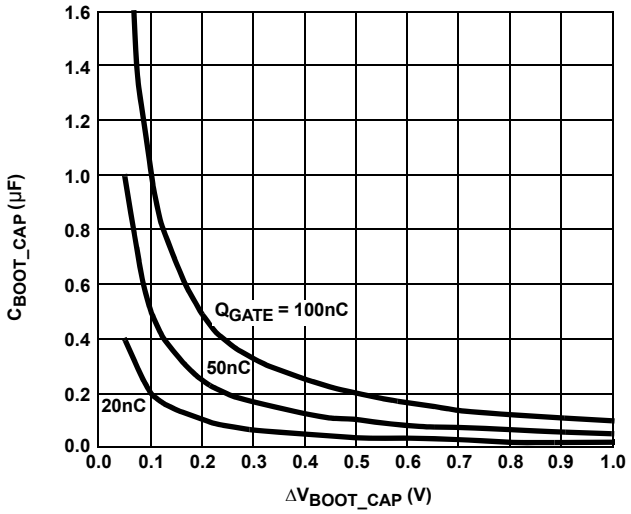


FIGURE 2. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Gate Drive Voltage Versatility

The ISL6615 provides the user with flexibility in choosing the gate drive voltage for efficiency optimization. The ISL6615 ties the upper and lower drive rails together. Simply applying a voltage from +4.5V up to 13.2V on PVCC sets both gate drive rail voltages simultaneously, while VCC's operating range is from +6.8V up to 13.2V.

Power Dissipation

Package power dissipation is mainly a function of the switching frequency (F_{SW}), the output drive impedance, the external gate resistance, and the selected MOSFET's internal gate resistance and total gate charge. Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. The maximum allowable IC power dissipation for the SO8 package is approximately 800mW at room temperature, while the power dissipation capacity in the DFN package, with an exposed heat escape pad, is more than 1.5W. The DFN package is more suitable for high frequency applications. See "Layout Considerations" on page 8 for thermal transfer improvement suggestions. When designing the driver into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for the selected MOSFETs. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated with Equations 2 and 3, respectively.

$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \bullet VCC \quad \text{(EQ. 2)}$$

$$P_{Qg\_Q1} = \frac{Q_{G1} \bullet PVCC^2}{V_{GS1}} \bullet F_{SW} \bullet N_{Q1}$$

$$P_{Qg\_Q2} = \frac{Q_{G2} \bullet PVCC^2}{V_{GS2}} \bullet F_{SW} \bullet N_{Q2}$$

$$I_{DR} = \left(\frac{Q_{G1} \bullet PVCC \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet PVCC \bullet N_{Q2}}{V_{GS2}} \right) \bullet F_{SW} + I_Q \quad \text{(EQ. 3)}$$

where the gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate to source voltage ($V_{GS1}$and V_{GS2}) in the corresponding MOSFET datasheet; I_Q is the driver's total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are the number of upper and lower MOSFETs, respectively; PVCC is the drive voltage for both upper and lower FETs. The I_Q*VCC product is the quiescent power of the driver without capacitive load and is typically 200mW at 300kHz and VCC = PVCC = 12V.

The total gate drive power losses are dissipated among the resistive components along the transition path. The drive resistance dissipates a portion of the total gate drive power losses, the rest will be dissipated by the external gate resistors (R_{G1} and R_{G2}) and the internal gate resistors (R_{GI1} and R_{GI2}) of MOSFETs. Figures 3 and 4 show the typical upper and lower gate drives turn-on transition path. The power dissipation on the driver can be roughly estimated, as shown in Equation 4.

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + I_Q \bullet VCC \quad \text{(EQ. 4)}$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}} \right) \bullet \frac{P_{Qg\_Q1}}{2}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}} \right) \bullet \frac{P_{Qg\_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

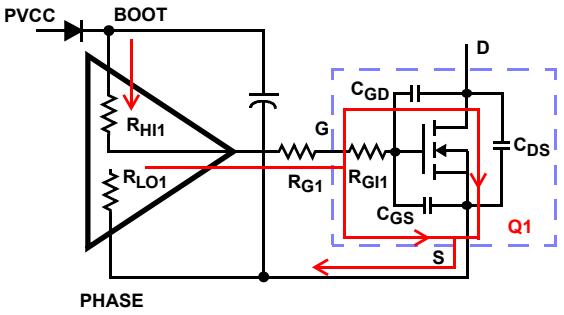


FIGURE 3. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

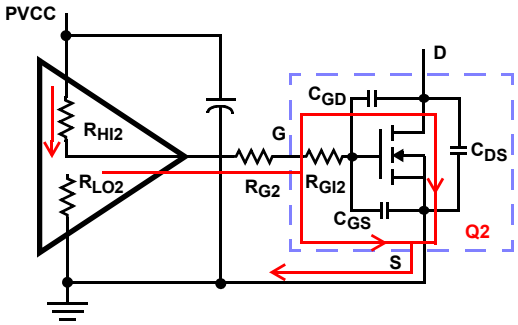


FIGURE 4. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

Application Information

Layout Considerations

The parasitic inductances of the PCB and of the power devices' packaging (both upper and lower MOSFETs) can cause serious ringing, exceeding the device's absolute maximum ratings. A good layout helps reduce the ringing on the switching node (PHASE) and significantly lowers the stress applied to the output drives. The following advice is meant to lead to an optimized layout and performance:

- Keep decoupling loops (VCC-GND, PVCC-GND and BOOT-PHASE) short and wide (at least 25 mils). Avoid using vias on decoupling components other than their ground terminals, which should be on a copper plane with at least two vias.
- Minimize trace inductance, especially on low-impedance lines. All power traces (UGATE, PHASE, LGATE, GND, PVCC, VCC, GND) should be short and wide (at least 25 mils). Try to place power traces on a single layer, otherwise, two vias on interconnection are preferred where possible. For no connection (NC) pins on the QFN part, connect it to the adjacent net (LGATE2/PHASE2) can reduce trace inductance.

- Shorten all gate drive loops (UGATE-PHASE and LGATE-GND) and route them closely spaced.
- Minimize the inductance of the PHASE node. Ideally, the source of the upper and the drain of the lower MOSFET should be as close as thermally allowable.
- Minimize the current loop of the output and input power trains. Short the source connection of the lower MOSFET to ground as close to the transistor pin as feasible. Input capacitors (especially ceramic decoupling) should be placed as close to the drain of upper and source of lower MOSFETs as possible.
- Avoid routing relatively high impedance nodes (such as PWM and ENABLE lines) close to high dV/dt UGATE and PHASE nodes.

In addition, for heat spreading, place copper underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried power ground plane(s) with thermal vias. This combination of vias for vertical heat escape, extended copper plane, and buried planes for heat spreading allows the IC to achieve its full thermal potential.

Upper MOSFET Self Turn-On Effects at Start-up

Should the driver have insufficient bias voltage applied, its outputs are floating. If the input bus is energized at a high dV/dt rate while the driver outputs are floating, due to the self-coupling via the internal C_{GD} of the MOSFET, the UGATE could momentarily rise up to a level greater than the threshold voltage of the MOSFET. This could potentially turn on the upper switch and result in damaging inrush energy. Therefore, if such a situation (when input bus powered up before the bias of the controller and driver is ready) could conceivably be encountered, it is a common practice to place a resistor (R_{UGPH}) across the gate and source of the upper MOSFET to suppress the Miller coupling effect. The value of the resistor depends mainly on the input voltage's rate of rise, the C_{GD}/C_{GS} ratio, as well as the gate-source threshold of the upper MOSFET. A higher dV/dt, a lower C_{DS}/C_{GS} ratio, and a lower gate-source threshold upper FET will require a smaller resistor to diminish the effect of the internal capacitive coupling. For most applications, the integrated 20kΩ typically sufficient, not affecting normal performance and efficiency.

The coupling effect can be roughly estimated with the formulas in Equation 5, which assume a fixed linear input ramp and neglect the clamping effect of the body diode of the upper drive and the bootstrap capacitor. Other parasitic components such as lead inductances and PCB capacitances are also not taken into account. These equations are provided for guidance purpose only. Therefore, the actual coupling effect should be examined using a very high impedance (10MΩ or greater) probe to ensure a safe design margin.

$$V_{GS\_MILLER} = \frac{dV}{dt} \cdot R \cdot C_{rss}\left(1 - e^{\frac{-V_{DS}}{\frac{dV}{dt} \cdot R \cdot C_{iss}}}\right) \quad \text{(EQ. 5)}$$

$$R = R_{UGPH} + R_{GI} \qquad C_{rss} = C_{GD} \qquad C_{iss} = C_{GD} + C_{GS}$$

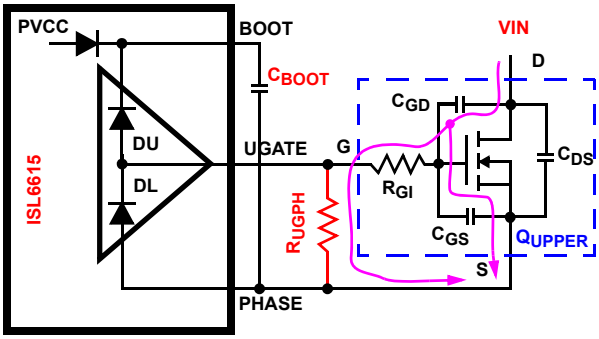
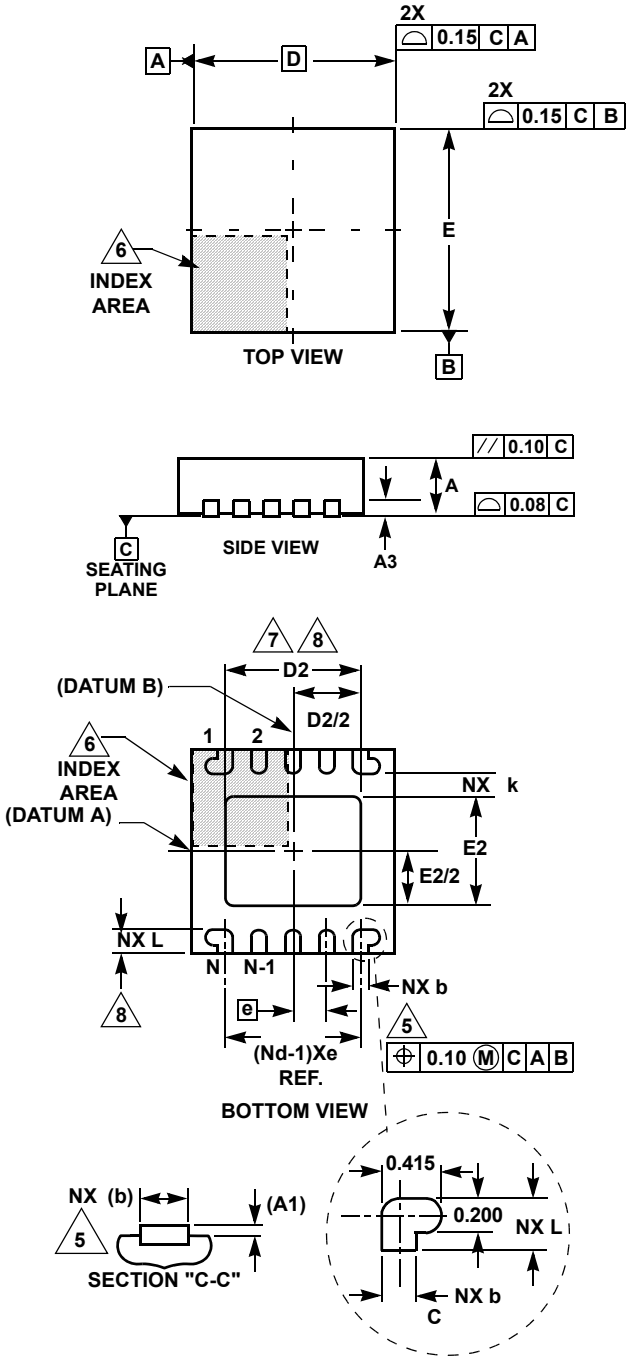


FIGURE 5. GATE-TO-SOURCE RESISTOR TO REDUCE UPPER MOSFET MILLER COUPLING

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.28	5,8
D		3.00 BSC		-
D2	1.95	2.00	2.05	7,8
E		3.00 BSC		-
E2	1.55	1.60	1.65	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.35	0.40	8
N		10		2
Nd		5		3

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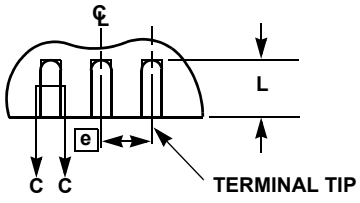
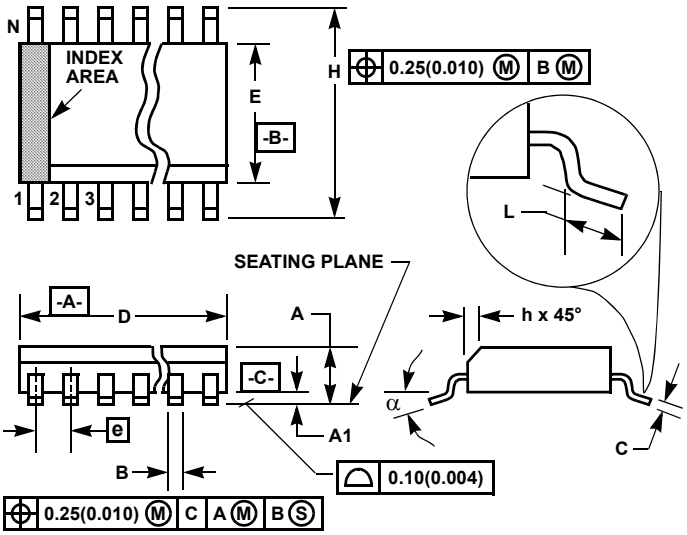
NOTES:

1. Dimensioning and trancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.



FOR ODD TERMINAL/SIDE

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerances per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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