ISL8115

High Voltage Synchronous Buck PWM Controller with Integrated Gate Driver and Current Sharing Capability

FN8272
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The ISL8115 is a synchronous buck PWM controller with current sharing capability. The current sharing function allows multiple modules to be connected in parallel to achieve higher output current and to reduce input and output ripple current, resulting in fewer components and reduced output dissipation.

Utilizing voltage-mode control with input voltage feed-forward compensation, the ISL8115 maintains a constant loop gain for optimal transient response, especially for applications with a wide input voltage range.

The ISL8115 protects against overcurrent conditions by inhibiting the PWM operation while monitoring the current with DCR of the output inductor, or a precision resistor. It also has a pre-POR overvoltage protection option, which provides some protection to the load if the upper MOSFET(s) is shorted.

The ISL8115 features remote ground sensing, programmable input voltage UVLO, output under/overvoltage protection, power-good indication, and fault Hand Shake capability.

Applications

- Power supply for datacom/telecom and POL
- Wide input voltage range buck regulators
- High current density power supplies RF power amplifier bias compensation

Features

- Wide V_{IN} range operation: 2.97V to 36V; up to 5.5V output and 30A load current per phase
- Fast transient response
  - Voltage-mode PWM leading-edge modulation with non-linear control
  - Input voltage feed-forward
- Integrated 5V high speed 4A MOSFET gate drivers
  - Internal bootstrap diode
- Excellent output voltage regulation
  - 0.6V ±1.0% internal reference (-40°C ~ 125°C)
  - 0.6V ±0.7% internal reference (-40°C ~ 105°C)
  - Differential voltage sensing
- Excellent current balancing and overcurrent protection
  - Peak and average overcurrent protection
  - Output current monitor on the ISET pin
- Oscillator programmable from 150kHz to 1.5MHz
  - Frequency synchronization to external clock signal
- Diode emulation mode for light load efficiency improvement
- Power-good open drain output
- Pre-bias start-up function
- Output OVP, UVP; OTP
- Adjustable Soft-Start

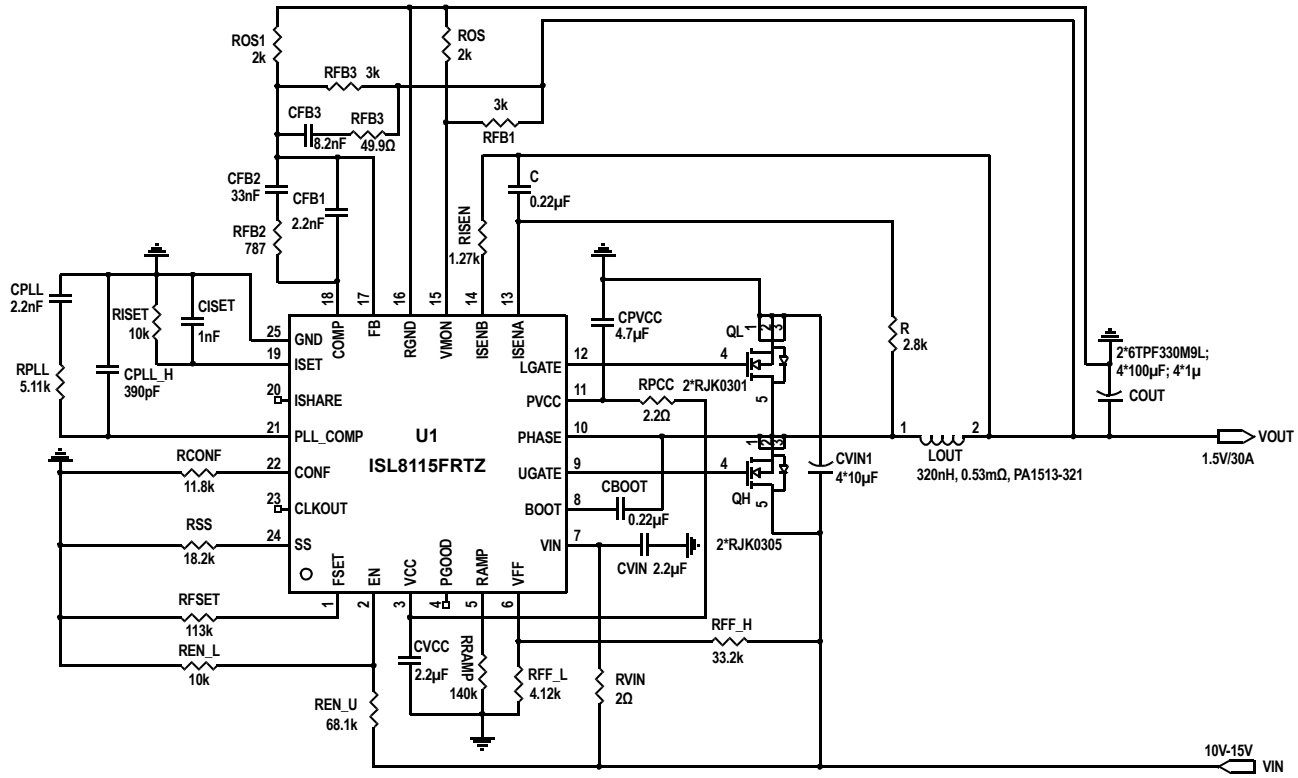

FIGURE 1. TYPICAL APPLICATION CIRCUIT, 10V-15V INPUT, 1.5V/30A OUTPUT

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Application Diagrams

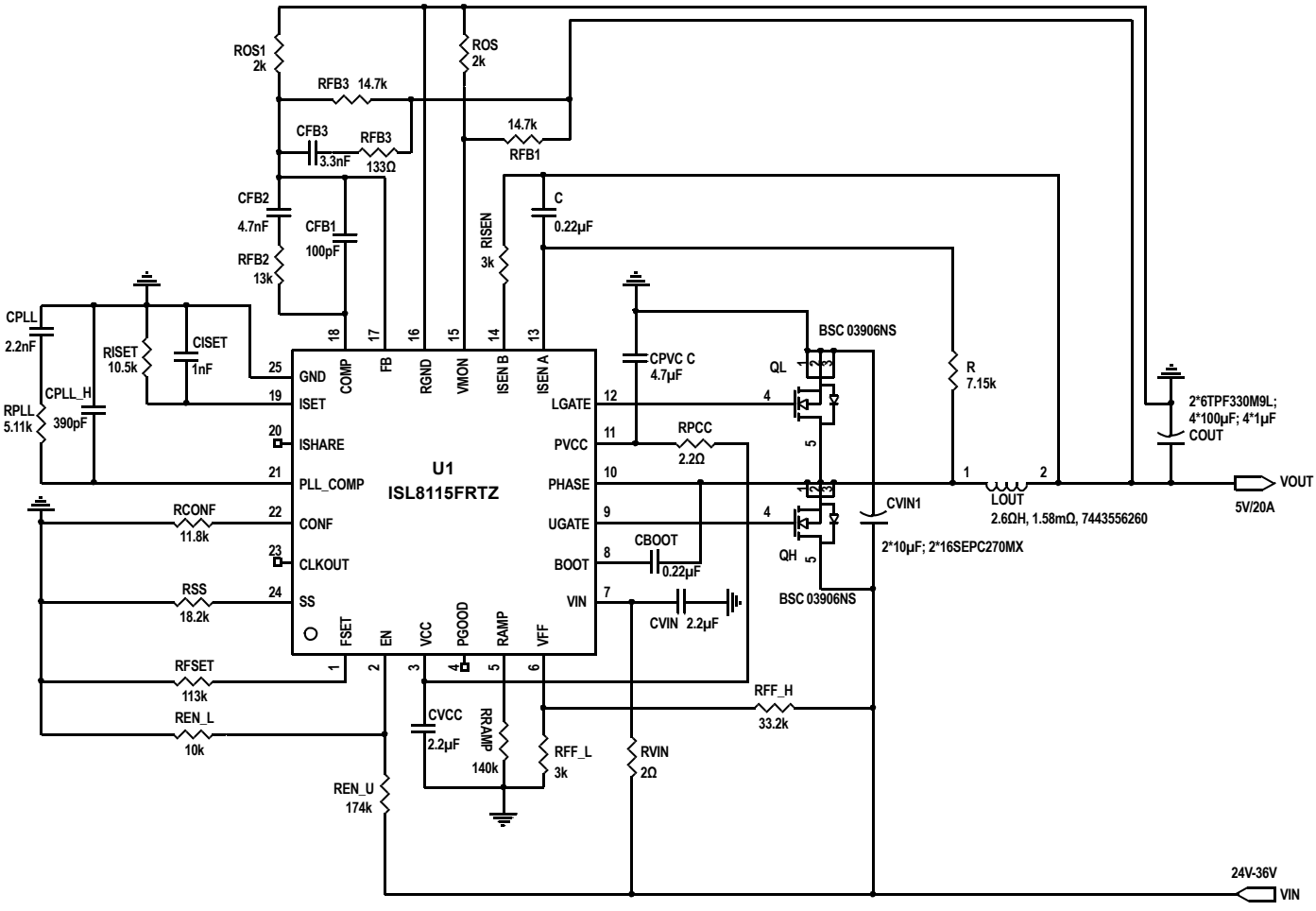


FIGURE 2. TYPICAL APPLICATION CIRCUIT, 24V-36V INPUT, 5V/20A OUTPUT

Application Diagrams (Continued)

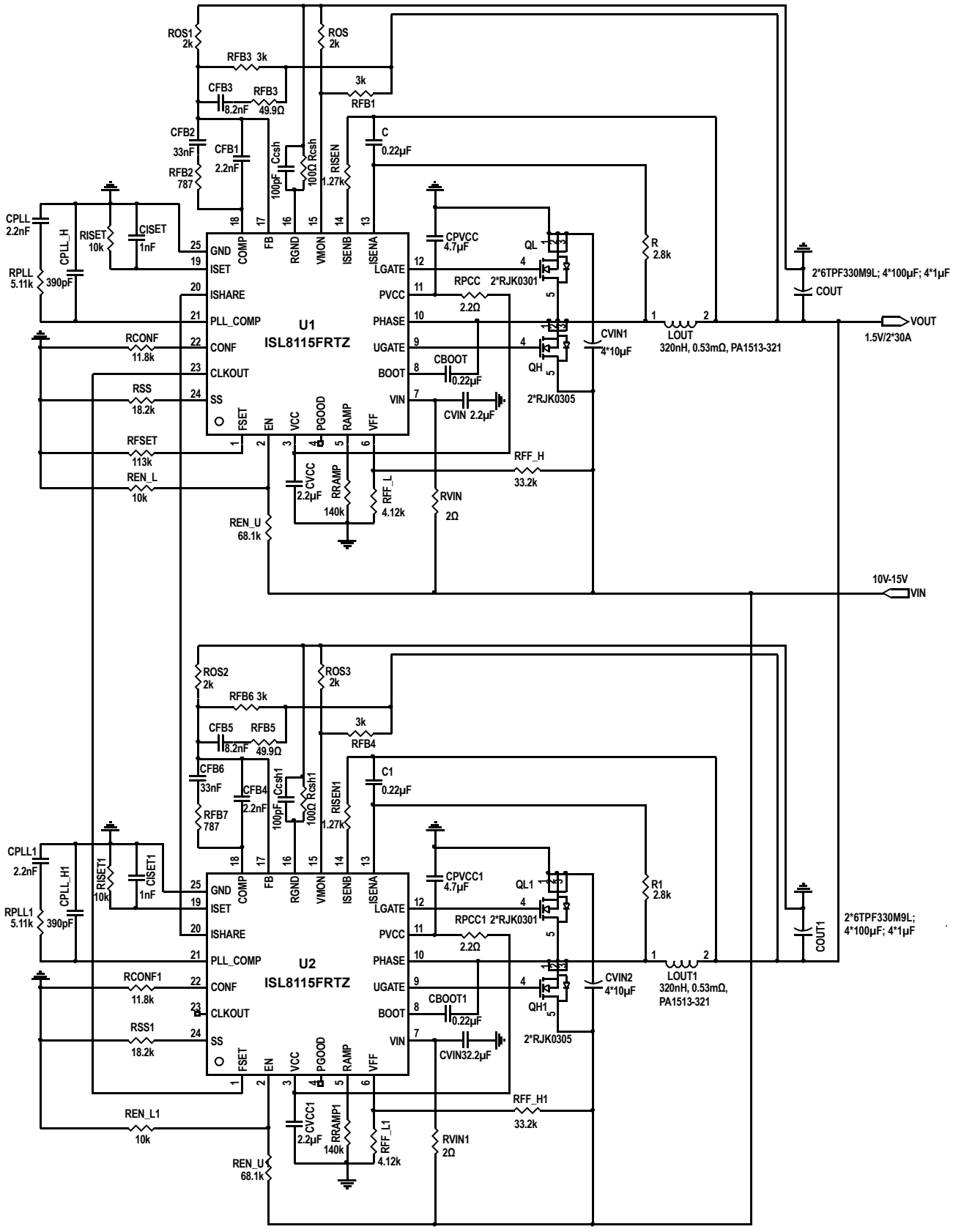
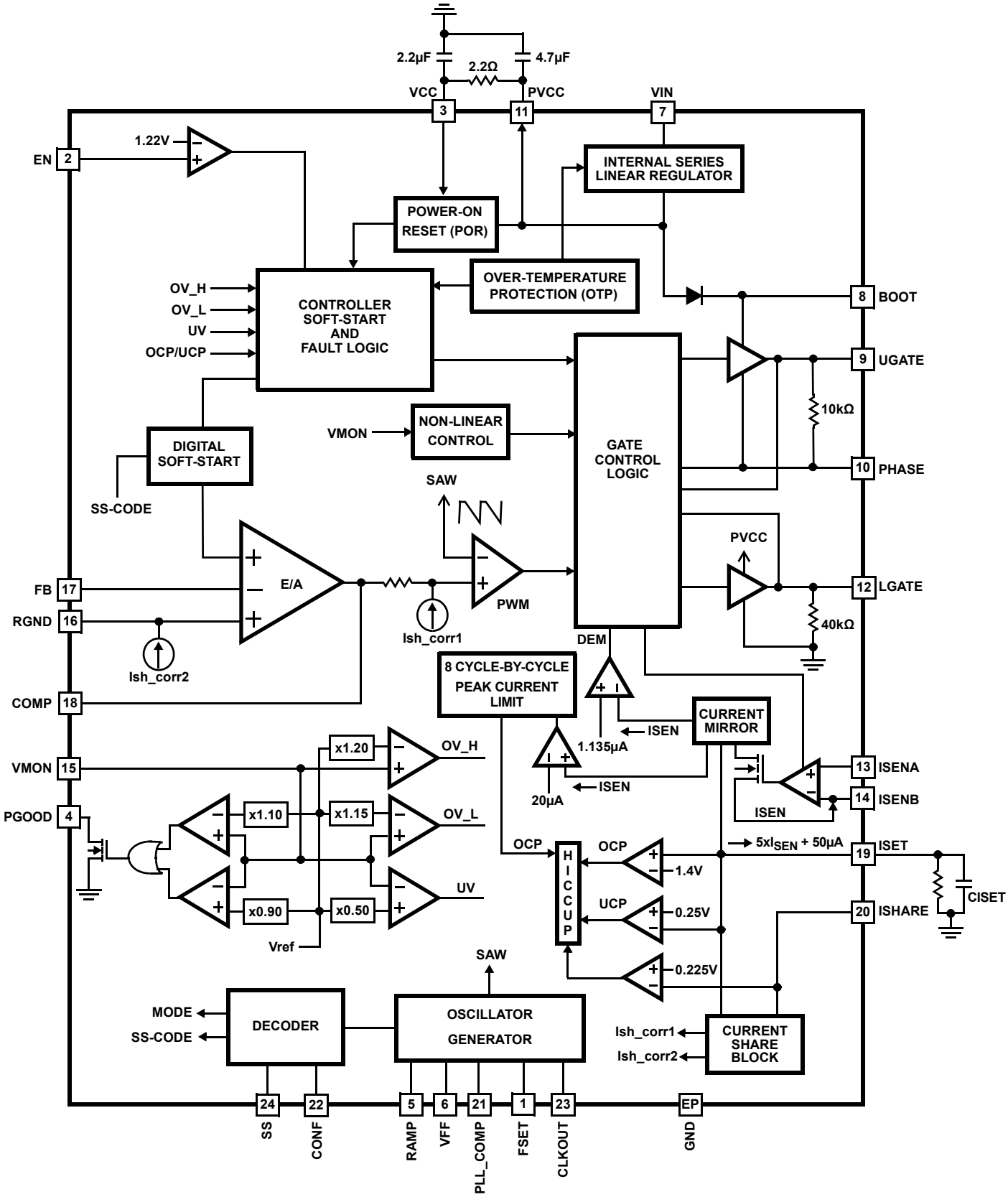


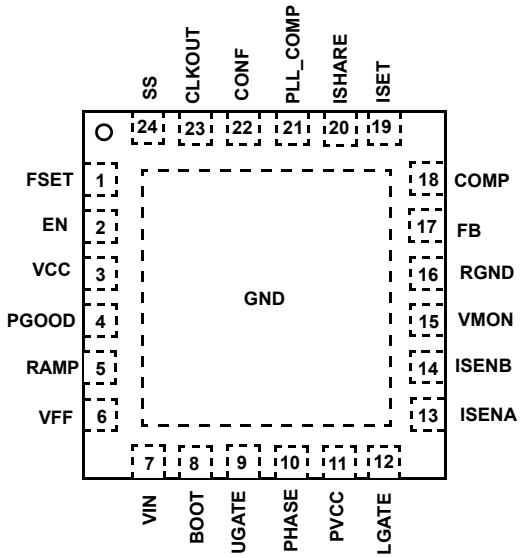
FIGURE 3. 2-PHASE, 10V-15V INPUT, 1.5V/60A OUTPUT

Block Diagram



Pin Configuration

ISL8115 (24 LD 4x4 QFN)
TOP VIEW



Functional Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	FSET	Placing a resistor (R_{FSET}) from this pin to GND to adjust the switching frequency. Input an external clock signal to this pin and the internal oscillator synchronizes with the leading edge of the input signal.
2	EN	The input voltage to this pin is compared with a precision 1.22V reference. Tie this pin to ground to disable the part. Tie this pin to VIN through a resistor divider to realize undervoltage lock-out.
3	VCC	This pin provides power for the analog circuitry. Connect this pin to a 2.97V to 5.15V bias through a recommended RC filter. This pin can be powered up by the internal or external linear regulator. A 2.2µF filter capacitor is recommended to connect closely to the pin.
4	PGOOD	Provides an open drain Power-Good signal when the voltage at VMON is within ±10% of nominal output regulation point after soft-start is complete.
5	RAMP	A resistor to GND to set the sawtooth ramp. Select the resistor value to make the ramp amplitude the same as the voltage on VFF. Refer to Voltage Feedforward Section on Page 15. $R_{ramp} = \frac{T_s - 275ns}{3 \times 10pF}; Ts = \frac{1}{F_{SW}}$
6	VFF	Pin for input voltage feed-forward. The voltage at this pin sets the internal oscillator ramp peak-to-peak amplitude at 1xVFF. A resistor divider network from input voltage to this pin is required and an additional decoupling capacitor may be required at this pin in noisy input environments. Make sure VFF is in the range of the clamp voltage (0.53V to 2.59V) specified in “Electrical Specifications” on page 9.
7	VIN	This pin should be tied directly to the input rail when using the internal linear regulator. It provides power to the internal linear drive circuitry.
8	BOOT	This pin provides the bootstrap bias for the high-side driver.
9	UGATE	This pin provides the drive signals for the high-side devices and should be connected to the high-side MOSFETs’ gates.
10	PHASE	Connect this pin to the source of the high-side MOSFETs and the drain of the low-side MOSFETs. This pin represents the return path for the high-side gate drivers.
11	PVCC	Connect a 4.7µF capacitor closely to this pin. This pin is the output of the internal series linear regulator. It provides the bias for both low-side and high-side drivers. Its operational voltage range is 2.97V to 5.3V. When the input supply is ≤5V, this pin should be tied directly to VIN to eliminate the dropout voltage in the internal linear regulator.

Functional Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
12	LGATE	This pin provides the drive for the low-side devices and should be connected to the lower MOSFETs' gates.
13	ISENA	The positive input of the current sensing amplifier. Provide DCR, or precision resistor current sensing.
14	ISENB	The negative input of the current sensing amplifier. Provide DCR, or precision resistor current sensing.
15	VMON	This pin monitors the regulator's output for OV and UV protection. PGOOD refers to the voltage on VMON. Connect a resistor divider from VOUT to RGND, with the same ratio as the FB resistor divider. It is not recommended to share the resistor divider for both FB and VMON; the response to a fault may not be as quick or robust. The voltage on this pin is also monitored for the non-linear control.
16	RGND	Pin for remote ground sensing. There's a current sourcing out from RGND if ISET voltage is lower than ISHARE in the multi-phase configuration. A typical 100Ω resistor is required connected between RGND and negative terminal of the load.
17	FB	FB is the inverting input of the error amplifier. This pin is connected to the feedback resistor divider and provides the voltage feedback signal for the controller.
18	COMP	This pin is the error amplifier's output. It should be connected to the FB pin through a desired compensation network. The lower limit of the voltage at COMP is 0.85V.
19	ISET	This pin sources a current equal to 5 times I_{SEN} with 50µA offset. Connect R_{ISET} to the pin to adjust the OCP trigger point. Parallel C_{ISET} with R_{ISET} to obtain the average output current signal at this pin. The voltage V_{ISET} set by an external resistor R_{ISET} represents the sensed current for the controller which compares with the internal reference to implement over current protection. Refer to the ""Average Overcurrent Protection" on page 18.
20	ISHARE	This pin is used for current sharing purpose and is configured to the current share bus representing all module's reference current. The voltage V_{ISHARE} represents the highest voltage of V_{ISET} of all active ISL8115(s) that connected together to the current share bus. Float in single phase operation. Pulling this pin low will disable the ISL8115.
21	PLL_COMP	Compensation pin for the internal PLL circuit. A compensation network shows in the typical application diagram is required. R_{PLL}(5.11kΩ); C_{PLL}(2.2nF); C_{PLL_H} (390pF) are recommended.
22	CONF	A resistor at this pin is used to set: 1.) Enable or disable Diode emulation mode, and 2) Phase delay of clock out signal with respect to input clock signal. See Table 1 for the resistor values.
23	CLKOUT	This pin provides clock signal to synchronize with other ISL8115(s). The phase delay of the CLKOUT with respect to the external clock signal is configured through CONF pin.
24	SS	A resistor connected from this pin to ground is used to select the length of soft-start period. See Table 2 for the resistor values.
25	GND	All voltage levels are referenced to this pad. This pad provides a return path for the low side MOSFET drivers and internal power circuitries as well as analog signals. Connect this pad to the board ground with the shortest possible path (9 vias to the internal ground plane, placed on the soldering pad are recommended).

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL8115FRTZ	81 15FRTZ	-40 to +125	24 Ld Exposed Pad 4x4 TQFN	L24.4x4F
ISL8115EVAL1Z	12V to 1.5V/30A Evaluation Board			
ISL8115EVAL2Z	28V to 5V/20A Evaluation Board			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL8115. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

VIN . . . . . -0.3V to 38V
PVCC. . . . . -0.3V to +6V
VCC. . . . . -0.3V to +6V
PVCC to VCC . . . . . -1V to +1V
BOOT . . . . . -0.3V to +44V
PHASE . . . . . -0.3V to +41V
PHASE Voltage Transient (20ns max) . . . . . GND - 2V
Boot to Phase Voltage, BOOT-PHASE. . . . . -0.3V to +6V
LGATE. . . . . -0.3V to +6V
LGATE Voltage Transient (20ns max). . . . . GND - 2.6V
ISENA, ISENB. . . . . -0.3V to +6.675V
Voltage on All Other Pins. . . . . -0.3V to V_{CC} + 0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114E). 2.5kV
Machine Model (Tested per JESD22-A115-A). 250V
Latch Up (Tested per JESD-78B; Class 1, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld QFN Package (Note 5).	39	3.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature . . . . . -40°C to +125°C
Input Voltage, V_{IN} . . . . . 2.97V to 36V
Driver Bias Voltage, PVCC . . . . . 2.97V to 5.5V
Signal Bias Voltage, VCC . . . . . 2.97V to 5.5V
Boot-to-Phase Voltage (Overcharged), BOOT- PHASE. . . . . <6V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. Unless otherwise specified, voltages are from the indicated pins to GND
5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions (V_{IN} = 12V; V_{CC} = PVCC = 5.15V; F_{SW} = 500kHz; EN = High), Unless Otherwise Noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
POWER SUPPLY						
I_{Q_VIN}	Nominal Supply VIN Current	UGATE = LGATE = Open		10	**15**	mA
		V_{IN} = 3.3V; V_{CC} = PVCC; UGATE = LGATE = Open		10	**15**	mA
$I_{Q\_VIN\_disable}$	Disable Supply VIN Current	EN = 0V, V_{IN} = 24V		17	**25**	µA
$I_{PVCC\_disable}$	PVCC Shutdown Current (sinking)	EN = 0V, PVCC = V_{IN} = 5.2V			**1.0**	µA
$I_{VCC\_disable}$	VCC Shutdown Current (sinking)	EN = 0V, V_{CC} = V_{IN} = 5.2V			**1.0**	µA
INTERNAL LINEAR REGULATOR						
PVCC	PVCC Voltage Level	I_{PVCC} = 0mA to 50 mA	**5.0**	5.15	**5.3**	V
I_{PVCC_LIMIT}	Output Current Limit	V_{CC} = PVCC = 3V; V_{IN} = 5.4V	**85**	140		mA
R_{LIN}	Saturated Equivalent Impedance	P-Channel MOSFET; V_{IN}= 5V		7		Ω
POWER-ON RESET						
	Rising VCC Threshold			2.88	**2.95**	V
	VCC POR Hysteresis			170		mV
	Rising PVCC Threshold			2.88	**2.95**	V
	PVCC POR Hysteresis			170		mV
ENABLE						
	Turn-On Threshold Voltage		**1.12**	1.22	**1.32**	V
I_{EN_HYS}	Enable Hysteresis			65		mV
OSCILLATOR						
	Oscillator Frequency Range		**150**		**1500**	kHz
	Oscillator Frequency	R_{FSET} = 165kΩ	**135**	150	**165**	kHz

Electrical Specifications Recommended Operating Conditions (V_{IN} = 12V; V_{CC} = PVCC = 5.15V; F_{SW} = 500kHz; EN = High), Unless Otherwise Noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
	Oscillator Frequency	R_{FSET} = 47.8kΩ	**450**	500	**550**	kHz
	Oscillator Frequency	R_{FSET} = 14.54kΩ	**1350**	1500	**1650**	kHz
	Oscillator Frequency Total Variation	VCC = 5.15V, From 150kHz to 1500kHz	**-10**		**+10**	%
	Frequency Synchronization Range		**150**		**1500**	kHz
	Input Signal Duty Cycle	Apply a input clock signal on FSET pin	**10**		**90**	%
$CLKOUT_H$	Clock Output High	I = 500µA (sourcing)	**4.9**			V
$CLKOUT_L$	Clock Output Low	I = 500µA (sinking)			**0.3**	V
$CLKOUT_{tR}$	Clock Output Rise Time	C_{LOAD} = 100pF		27		ns
$CLKOUT_{tF}$	Clock Output Fall Time	C_{LOAD} = 100pF		27		ns
SAWTOOTH RAMP						
V_{SRAMP_offset}	Sawtooth Ramp Offset	R_{RAMP} = (Ts-275n)/30p		1		V
V_{SRAMP_Max}	Sawtooth Ramp Peak Clamp Value			V_{CC}-1.2V		V
G_{SRAMP}	Linear Gain of Sawtooth Ramp Over V_{FF}	$G_{RAMP} = DV_{RAMP\_PK-PK}/V_{FF}$ R_{RAMP} = (Ts-275n)/30p		1		V/V
V_{SRAMP_pk-pk}	Sawtooth Ramp Peak-to-Peak Voltage	V_{CC} = 5.15V; VFF = 1V		1		V
V_{RAMP_max}	Upper Clamp Voltage of RAMP PIN		**2.59**	2.98	**3.36**	V
V_{RAMP_min}	Lower Clamp Voltage of RAMP PIN		**0.48**	0.5	**0.53**	V
PWM						
	Minimum LGATE On-TIME		**150**	200	**250**	ns
REFERENCE ACCURACY						
V_{FB}	Voltage on FB			0.6		V
	Accuracy	From -40°C to +125°C	**-1.0**		**+1.0**	%
	Accuracy	From -40°C to +105°C	-0.7		+0.7	%
ERROR AMPLIFIER						
	DC Gain	R_L = 10k, C_L = 1pF at COMP pin		98		dB
UGBW	Unity Gain-Bandwidth	R_L = 10k, C_L = 1pF at COMP pin		25		MHz
	Output Minimum Voltage Swing			0.85		V
	Output Maximum Voltage Swing			V_{CC}-0.8		V
SR_EA	Output Slew Rate	R_L = 10k, C_L = 1pF at COMP pin		±20		V/µs
I_{FB}	FB Input Current			20		nA
I_{COMP}	Output Source/Sink Current			±3		mA
	Effective RGND Range	With respect to GND		±200		mV
GATE DRIVER						
R_{UGATE_SOURCE}	Upper Drive Source Resistance	45mA Source Current		1.2		Ω
R_{UGATE_SINK}	Upper Drive Sink Resistance	45mA Sink Current		0.55		Ω
R_{LGATE_SOURCE}	Lower Drive Source Resistance	45mA Source Current		0.9		Ω
R_{LGATE_SINK}	Lower Drive Sink Resistance	45mA Sink Current		0.4		Ω
	UGATE to PHASE Internal Resistor			10		kΩ
	LGATE to GND Internal Resistor			40		kΩ

Electrical Specifications Recommended Operating Conditions (V_{IN} = 12V; V_{CC} = PVCC = 5.15V; F_{SW} = 500kHz; EN = High), Unless Otherwise Noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
CURRENT SENSE AMPLIFIER						
	DC Gain			70		dB
	Unity Gain-Bandwidth			5		MHz
	ISENA Pin Input current			10		nA
	Input Common Mode Range	V_{IN} > 9V	**-0.2**		**6.375**	V
	Input offset		**-0.6**		**0.6**	mV
	Differential Current Sense Voltage Range	R_{ISEN} = 2kΩ	**-8**		**40**	mV
I_{SET_OFFSET}	ISET Offset Current		**44**	50	**55**	µA
$I_{DEM\_threshold}$	ISEN Threshold of DEM	R_{ISEN} = 2kΩ	**0.38**	1.135	**2.76**	µA
OVERCURRENT PROTECTION						
I_{OC}	ISEN Overcurrent Limit	V_{CC} = 5.15V	**17.6**	20	**22.4**	µA
		V_{CC} = 2.97V to 5.15V		20		µA
V_{ISET_OC}	ISET Pin OC Threshold	V_{CC} = 2.97V to 5.15V		1.40		V
		V_{CC} = 5.15V	**1.35**	1.40	**1.45**	V
	ISET Pin Under Current Threshold		**0.22**	0.25	**0.28**	V
	ISHARE Pin Fault Threshold		**0.22**	0.225	**0.24**	V
	ISHARE Pull-Down Voltage Capability	I_{SHARE} = 500µA			**0.2**	V
POWER GOOD MONITOR AND UNDER/OVERVOLTAGE PROTECTION						
V_{PG-}	Power-Good Lower Threshold	Voltage from VMON to RGND; ~3 clock cycles noise filter	**0.51**	0.54	**0.57**	V
V_{PG+}	Power-Good Upper Threshold	Voltage from VMON to RGND; ~3 clock cycles noise filter	**0.63**	0.66	**0.69**	V
	PGOOD Low Output Voltage	I_{PGOOD} = 2mA			**0.35**	V
UNDER/OVER VOLTAGE PROTECTION WITH VMON						
$V_{OV\_NONLatch}$	Overvoltage Non-Latching Off Threshold	Voltage from VMON to RGND; **above the Power-Good Upper Threshold**		30		mV
V_{OV_Latch}	Overvoltage Latching Off Threshold	Voltage from VMON to RGND; **above the OV Non-Latching UP Threshold**		30		mV
	Overvoltage LGATE Release Trip Point	Voltage from VMON to RGND		0.51		V
V_{UV}	Undervoltage Protection Trip Point	Voltage from VMON to RGND; after soft-start completed		0.3		V
V_{UV}	Undervoltage Protection Trip Point Hysteresis			0.032		V
NON-LINEAR CONTROL						
	Offset of the non-linear control	Refer to Figure 23		20		mV
OVER-TEMPERATURE PROTECTION						
T_{OTP}	Over-Temperature Protection Trip Point			160		°C
	OTP Release Threshold			145		°C

NOTE:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested

Typical Performance Curves

Unless otherwise stated, all curves were tested with example circuit in Figure 1.

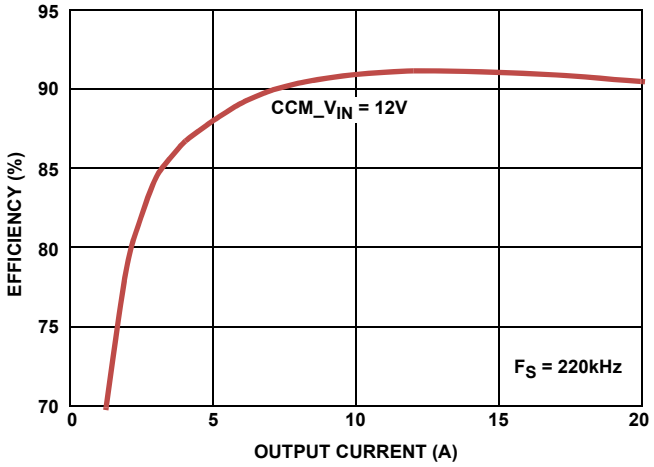


FIGURE 4. EFFICIENCY AT 12V INPUT, 1.5V OUTPUT

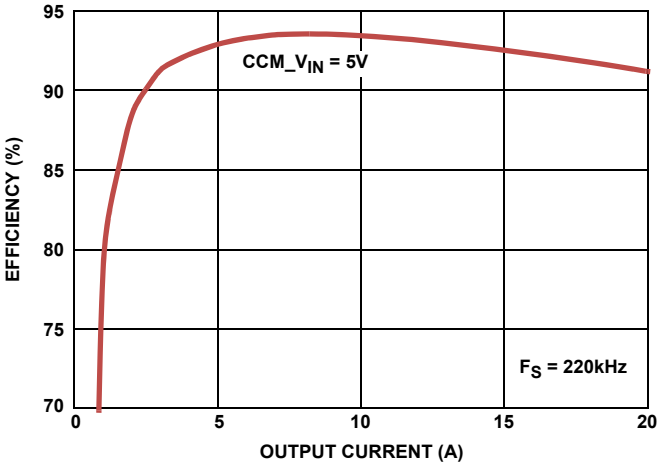


FIGURE 5. EFFICIENCY AT 5V INPUT, 1.5V OUTPUT

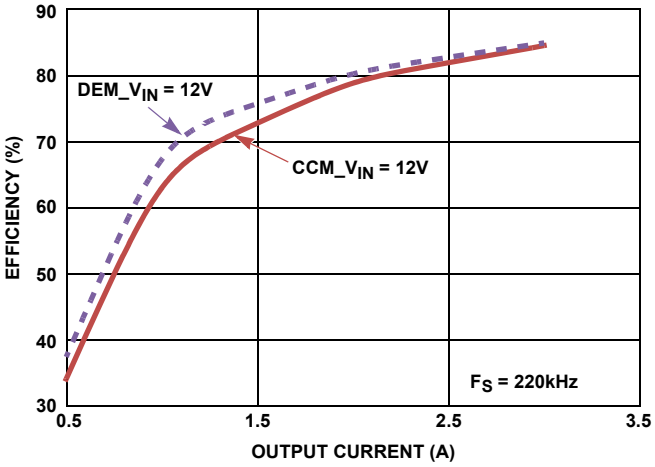


FIGURE 6. EFFICIENCY vs LOAD CURRENT AT 12V INPUT

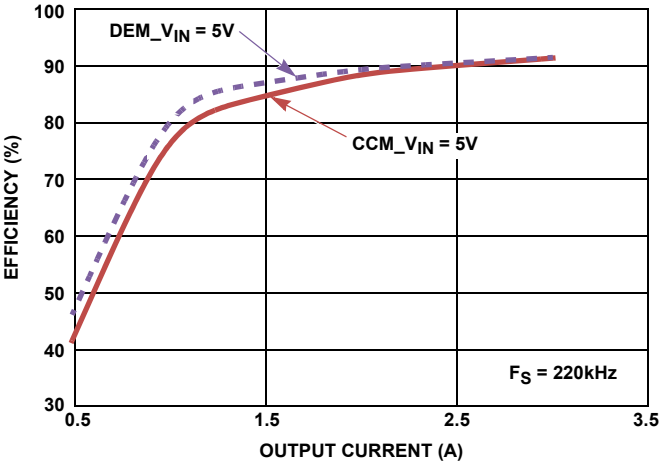


FIGURE 7. EFFICIENCY vs LOAD CURRENT AT 5V INPUT

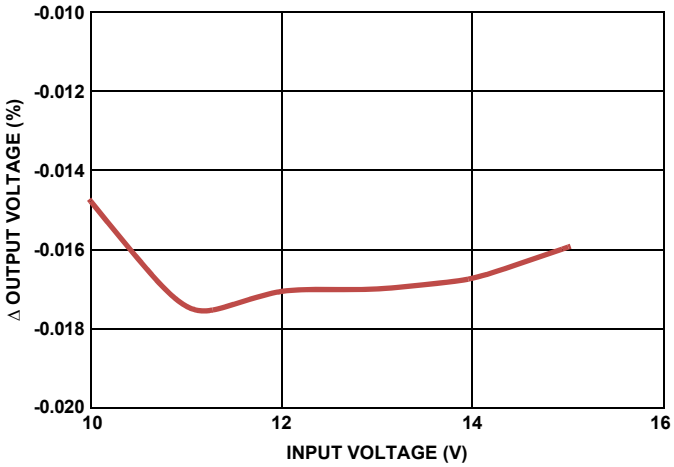


FIGURE 8. LINE REGULATION, V_{OUT} = 1.5V, I_O = 20A

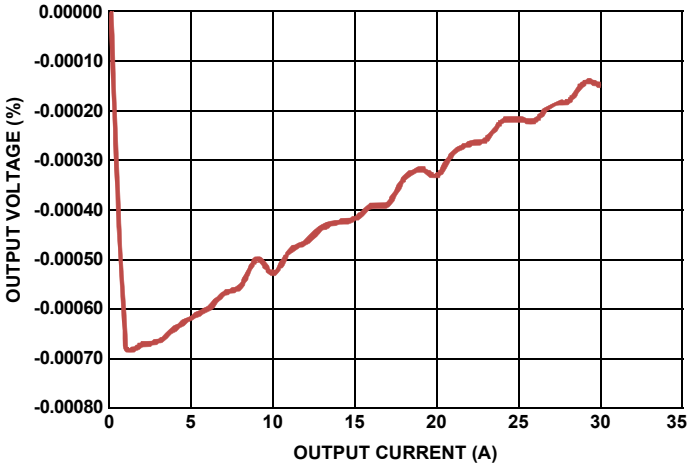


FIGURE 9. LOAD REGULATION, V_{IN} = 12V, V_{OUT} = 1.5V

Typical Performance Curves

Unless otherwise stated, all curves were tested with example circuit in Figure 1. **(Continued)**

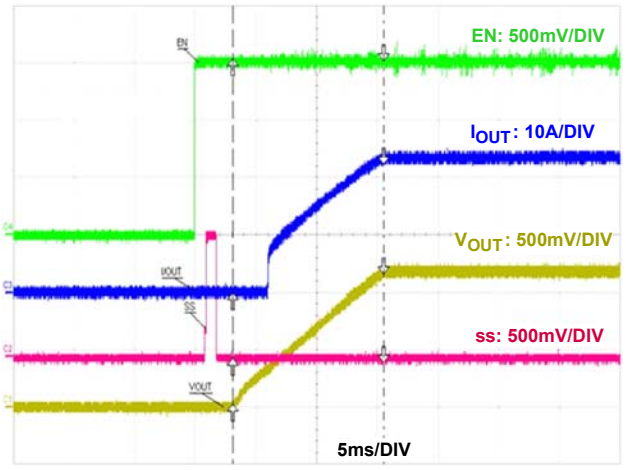


FIGURE 10. FULL LOAD START-UP

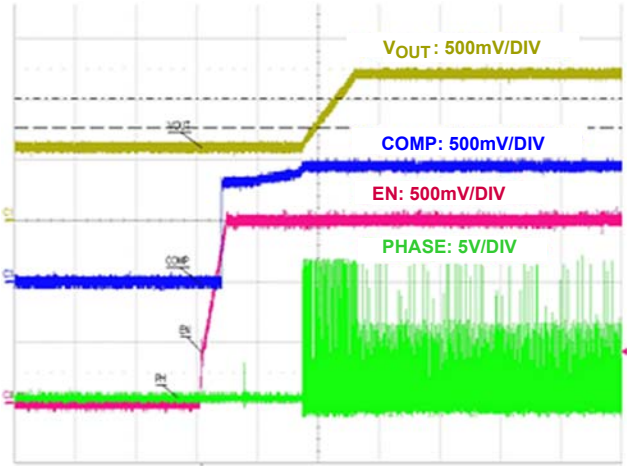


FIGURE 11. PRE-BIAS START-UP

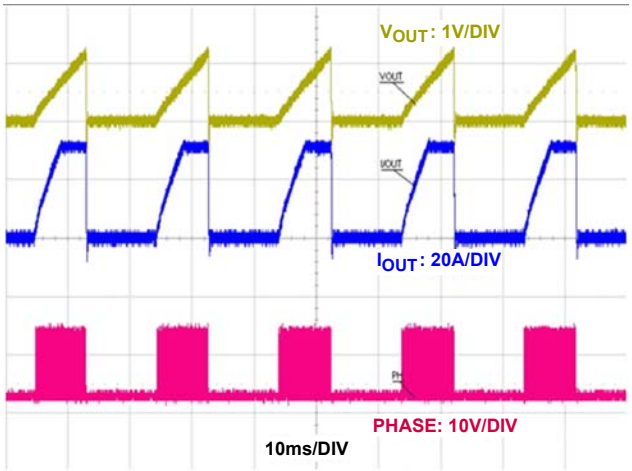


FIGURE 12. HICCUP OCP

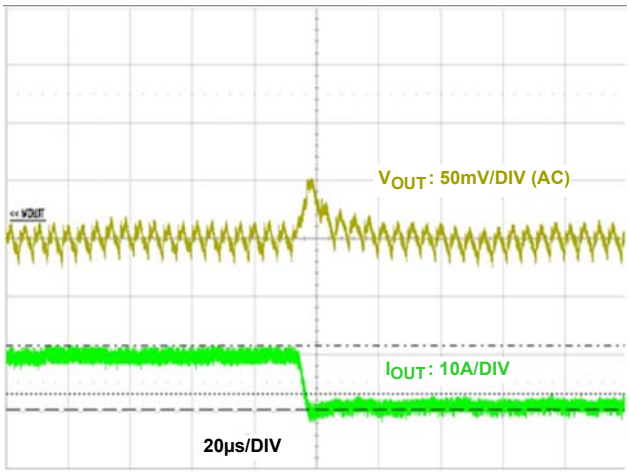


FIGURE 13. TRANSIENT RESPONSE 2A/µs

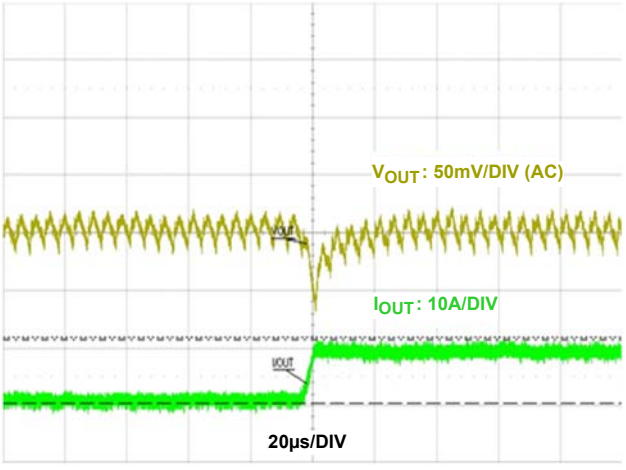


FIGURE 14. TRANSIENT RESPONSE 2A/µs

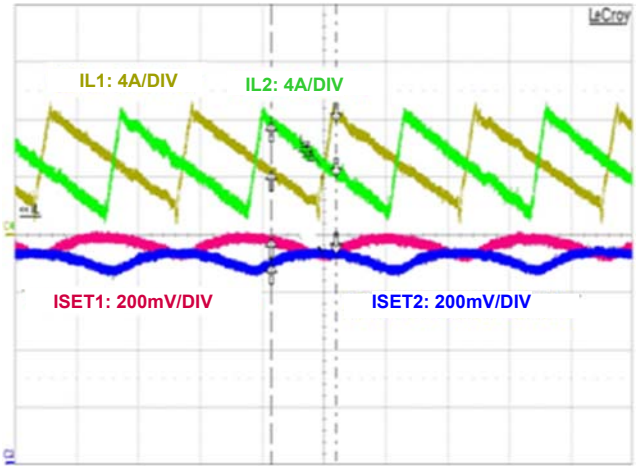


FIGURE 15. CURRENT SHARING WITH 2-PHASE CONFIGURATION

Typical Performance Curves

Unless otherwise stated, all curves were tested with example circuit in Figure 1. **(Continued)**

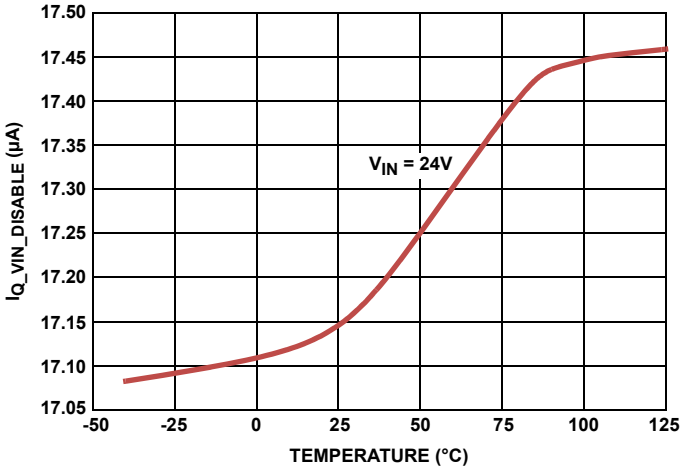


FIGURE 16. SHUTDOWN CURRENT vs TEMPERATURE

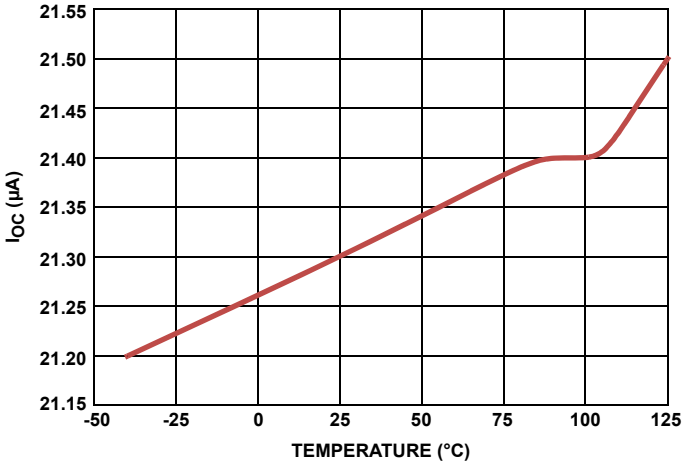


FIGURE 17. OVERCURRENT THRESHOLD vs TEMPERATURE

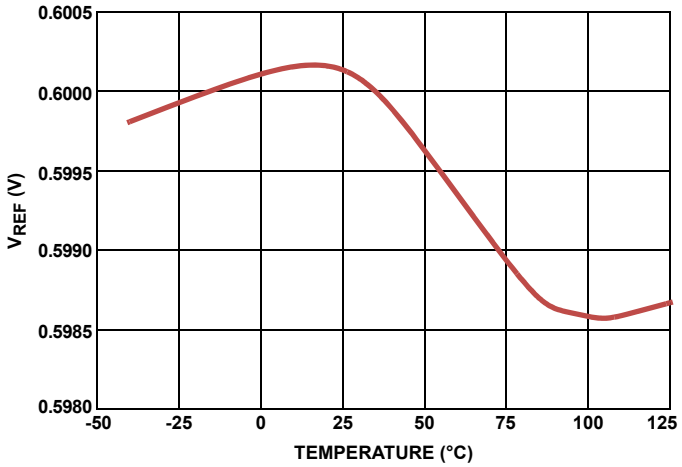


FIGURE 18. FEEDBACK VOLTAGE REFERENCE vs TEMPERATURE

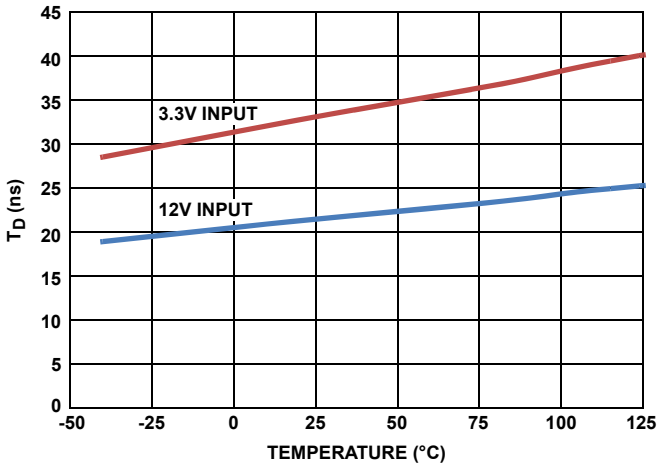


FIGURE 19. DEAD TIME vs TEMPERATURE

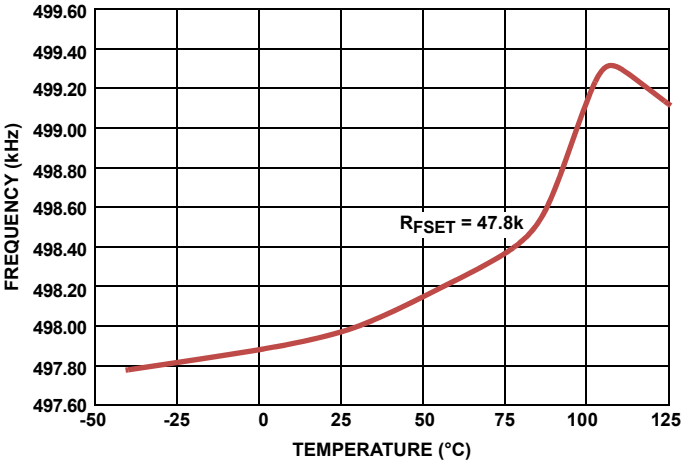


FIGURE 20. FREQUENCY vs TEMPERATURE

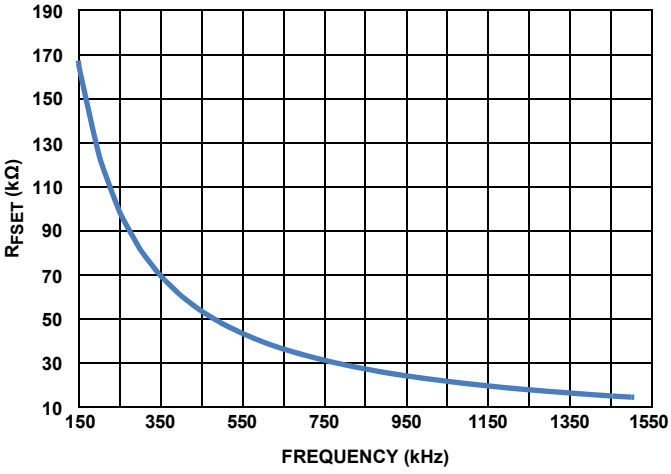


FIGURE 21. FREQUENCY vs R_{FSET}

Functional Description

Functional Overview

The ISL8115 is a synchronous buck PWM controller with current sharing capability. The current sharing function allows multiple modules to be connected in parallel to achieve higher output current. The controller also features multi-phase operation to reduce input and output ripple current, resulting in fewer components and reduced output dissipation.

Utilizing voltage-mode control with input voltage feed-forward compensation, the ISL8115 maintains a constant loop gain for optimal transient response, especially for applications with a wide input voltage range.

Initialization

The ISL8115 requires V_{CC} and PVCC biased by a single supply. The Power-On Reset (POR) function continually monitors the input supply voltages (PVCC and V_{CC}) and the voltage at EN pin.

With PVCC, V_{CC} and EN above their POR thresholds, the IC will initialize a process to read the resistor value on the CONF and SS pins. This process can take up to 2ms. Failure to read the resistor values will stop the soft-start process.

After successfully reading the resistor values on the CONF and SS pins, there is another 1ms delay for the PLL.

If the system voltage drops below the falling POR threshold, then UGATE and LGATE are forced off. Also ISHARE is pulled low.

Enable and Input Voltage UVLO

When the voltage on EN pin is greater than the 1.22V threshold, the controller is enabled. If the EN voltage is less than 1.22V minus the hysteresis (typical 65mV), the controller is disabled.

The EN pin can be used as a voltage monitor for the input undervoltage lock-out by connecting the EN pin to the input rail through a resistor divider.

Pre-bias Startup

A pre-bias voltage may exist at the output before the controller is enabled. The ISL8115 can support a pre-bias startup condition by keeping UGATE and LGATE off until the internal soft-start voltage exceeds the feedback voltage. This feature prevents the output voltage from discharging through the lower MOSFET during the soft-start.

Setting CONF Pin

A resistor connected from the CONF pin to ground is used to:

- Enable or disable diode emulation mode (DEM) after soft-start.
- Set the phase delay of CLKOUT with respect to an external clock signal applied to the FSET pin.

Use a resistor with 1% tolerance on the CONF pin.

TABLE 1. RESISTOR VALUES TO SET CONF PIN

PHASE DELAY (°)	DEM	1% TOLERANCE RESISTOR VALUE (kΩ)
0	ENABLE	46.4
60		73.2
90		105
120		137
180		11.8
240		18.2
270		26.1
300		34
0	DISABLE (Force CCM)	2.94
60		4.53
90		6.49
120		8.66
180		0.732
240		1.13
270		1.62
300		2.15

Setting SS pin

A resistor connected from the SS pin to ground is used to set the length of the output soft-start time. The internal soft-start DAC operates with and internal 2MHz clock. The value of the resistor on this pin set number on steps for the soft-start. The resistor value and the corresponding soft-start duration is shown in Table 2. Use a resistor with 1% tolerance on the SS pin.

TABLE 2. RESISTOR VALUES TO SET SOFT-START TIME

1% TOLERANCE RESISTOR VALUE (kΩ)	SOFT-START TIME (ms)
46.4	0.4
73.2	0.8
105	1.2
137	2.2
11.8	4.8
18.2	8.8
26.1	12.8
34	25.6

When using multiple ISL8115s in parallel module configuration, all soft-start times must be set to the same value.

Frequency Setting

The switching frequency is set by the R_{FSET} connected between the FSET pin and ground. Figure 21 shows the typical R_{FSET} vs Frequency variation curve. Equation 1 illustrates the relationship between R_{FSET} and switching frequency.

To synchronize with an external clock, apply a clock signal in the programmable oscillator range of 150kHz to 1.5MHz to the FSET pin. A duty cycle in the range of 10% to 90% is required.

$$R_{FSET} = 25\times10^{9}\cdot\left(\frac{1}{Fsw} - 85\times10^{-9}\right) \quad \text{(EQ. 1)}$$

Voltage Feed-forward

The voltage applied to the VFF pin can adjust the amplitude of the internal sawtooth ramp. It is recommended to set the amplitude equal to V_{FF}. This helps to maintain a constant gain contributed by the modulator and the input voltage to achieve optimum loop response over a wide input voltage range. Figure 22 shows the feed-forward circuits.

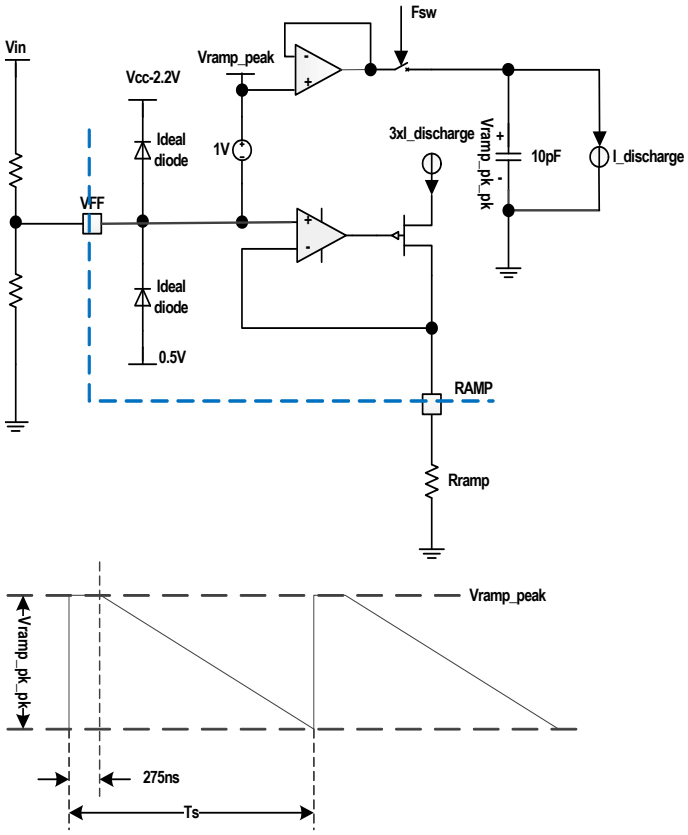


FIGURE 22. FEED-FORWARD CIRCUITRY

V_{FF} voltage is clamped between 0.5V (typical) and V_{CC}-2.2V (typical). To make the feed forward work for all input voltage, the voltage on VFF pin should be designed within this range.

The peak-to-peak amplitude of the sawtooth yields as:

$$V_{ramp-pk-pk} = I_{discharge}\times\frac{T_s - 275ns}{10pF} \quad \text{(EQ. 2)}$$

where:

$$I_{discharge} = \frac{V_{FF}}{3R_{ramp}} \quad \text{(EQ. 3)}$$

$$T_s = \frac{1}{F_{sw}}$$

According to the Equations 2 and 3, design the resistor at the RAMP pin to make the amplitude of sawtooth equal to V_{FF}.

$$R_{ramp} = \frac{T_s - 275ns}{3\times10pF} \quad \text{(EQ. 4)}$$

For example, select 113kΩ for R_{FSET} to achieve 220kHz switching frequency and 140kΩ for R_{ramp} to make the $V_{ramp\_pk\_pk} = V_{FF}$. The sawtooth ramp offset voltage is 1V and the peak of the sawtooth is to V_{FF} +1V.

Non Linear Control

In order to respond faster to a load step, non-linear control has been introduced in ISL8115. If the feedback voltage at VMON is greater than the voltage of the previous cycle plus 20mV (typical), the LG turns on immediately without waiting for the next clock signal. This function helps to improve the transient response especially for a controller with leading-edge modulator.

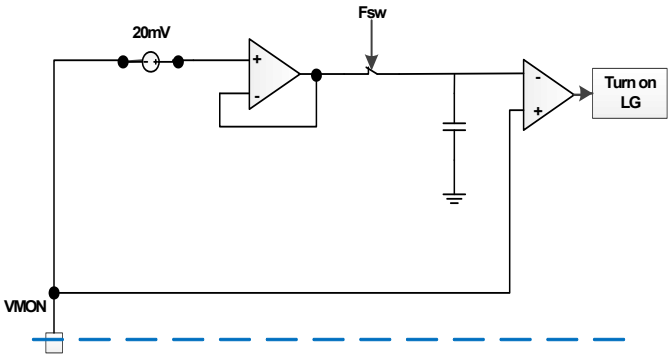


FIGURE 23. NON-LINEAR CONTROL CIRCUIT

Power-Good

The Power-Good comparator monitors the voltage on the VMON pin. The trip points are shown in Figure 24. Power-Good will not be asserted until the completion of the soft-start cycle. The Power-Good pulls low when EN is low or VMON is out of the threshold window. PGOOD stays high until the fault exists for three consecutive clock cycles.

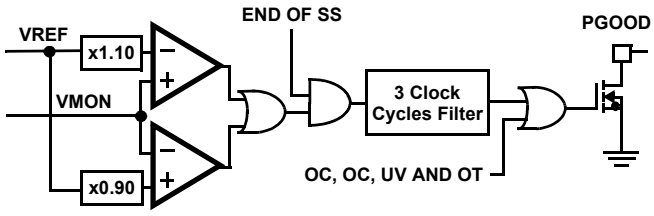


FIGURE 24. PGOOD CIRCUIT

Undervoltage and Overvoltage Protection

The Undervoltage (UV) and Overvoltage (OV) protection circuitry monitors the voltage on the VMON pin.

The UV functionality is not enabled until the end of soft-start. If the VMON drops below 50% of the 0.6V internal reference, the controller goes into hiccup mode and recovers until VMON rises up to 0.332V.

ISL8115 has 2 level OV thresholds: 115% (non-latch), and 120% (Latch). In an OV event with VMON between 115% and 120%, the high-side MOSFET is turned off, while the low-side MOSFET turns on. At the same time PGOOD is also pulled down. When the VMON voltage drops to 85% of reference voltage, the LGATE is turned off, then hiccup restart occurs.

An OV event (V_{OUT} > 120%) causes the high-side MOSFET to latch off permanently, while the low-side MOSFET turns on and then turns off after the output voltage drops below 85%. At the same time, the PGOOD and ISHARE are also latched low. The latch condition can be reset only by re-cycling V_{CC} or EN.

POR Overvoltage Protection (POR-OVP)

When both the VCC and PVCC are below the POR thresholds, the UGATE is low and LGATE is floating (high impedance). EN has no control over LGATE when below POR. When above POR, the LGATE will toggle with its PWM pulses. An external 10kΩ resistor can be placed between the PHASE and LGATE node to implement a PRE-POR-OVP circuit. The output of the converter is equal to the phase node voltage via output inductor and then is effectively clamped to the low-side MOSFET's gate threshold voltage, which provides some protection to the load if the upper MOSFET(s) is shorted during start-up, shutdown, or normal operations. For complete protection, the low-side MOSFET should have a gate threshold that is much smaller than the maximum voltage rating of the load.

The PRE-POR-OVP works against pre-biased start-up when pre-charged output voltage is higher than the threshold of the low-side MOSFET.

Over-Temperature Protection (OTP)

When the junction temperature of the IC is greater than +160°C (typically), the Ugate and Lgate are forced off. The ISHARE and PGOOD pins are forced low indicating a fault. In a multi-phase configuration, this pulls the ISHARE bus low and informs other channels to turn off. All connected ISHARE pins stay low, but release after the IC's junction temperature drops below the +15°C hysteresis (typical). The device now starts the initialization process of reading the CONFIG and SS resistors, PLL locking, and soft-start.

Inductor Current Sensing

The ISL8115 supports inductor DCR sensing techniques up to 5.5V output voltage, as shown in Figure 25.

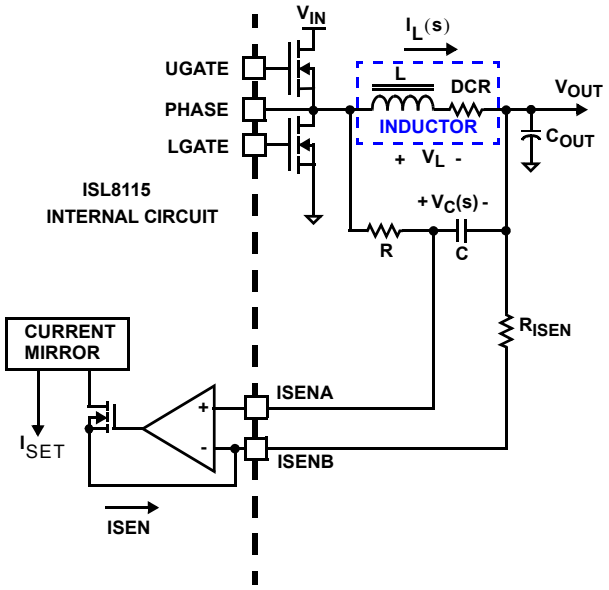


FIGURE 25. DCR SENSING CONFIGURATION

An inductor's winding is characteristic of a distributed resistance as measured by the DCR (Direct Current Resistance) parameter. Consider the inductor DCR as a separate lumped quantity, as shown in Figure 25. The inductor current, I_L, will also pass through the DCR. Equation 5 shows the S-domain equivalent voltage across the inductor V_L.

$$V_L = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 5)}$$

A simple R-C network across the inductor extracts the DCR voltage, as shown in Figure 25. The voltage on the capacitor V_C, can be shown to be proportional to the inductor current I_L, see Equation 6.

$$V_C = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{(s \cdot RC + 1)} \quad \text{(EQ. 6)}$$

If the R-C network components are selected such that the RC time constant (= R*C) matches the inductor time constant (= L/DCR), the voltage across the capacitor V_C is equal to the voltage drop across the DCR, i.e., proportional to the inductor current. The value of R should be as small as feasible for best signal-to-noise ratio. Make sure the resistor package size is appropriate for the power dissipated and include this loss in efficiency calculations.

In calculating the minimum value of R, the average voltage across C (average of $I_L DCR$ product) is small and can be neglected. Therefore, the minimum value of R may be approximated Equation 7:,

$$R_{min} = \frac{D \cdot (V_{IN-max} - V_{OUT})^2 + (1-D) \cdot V_{OUT}^2}{k \cdot P_{R-pkg} \cdot \delta_P} \quad \text{(EQ. 7)}$$

where $P_{R\text{-}pkg}$ is the maximum power dissipation specification for the resistor package and δ_P is the derating factor for the same parameter (e.g., $P_{R\text{-}pkg}$ = 0.063W for 0402 package, δ_P = 80% @ +85°C). k is the margin factor, also to limit temperature raise in the resistor package, recommend using 0.4. Once R_{min} has been calculated, solve for the maximum value of C from Equation 8:

$$C_{max} = \frac{L}{R_{min} \cdot DCR} \quad \text{(EQ. 8)}$$

Next, choose the next-lowest readily available value. Then substitute the chosen value into the same equation and re-calculate the value of R. Choose a 1% resistor standard value closest to this re-calculated value of R. For example, when V_{IN}-Max = 14.4V, V_{OUT} = 2.5V, L = 1mH and DCR = 1.5mΩ, with 0402 package Equation 7 yields R_{min} of 1476Ω and Equation 8 yields C_{max} of 0.45µF. Choose 0.39µF and re-calculate, the resistor yields 1.69kΩ.

With the internal low-offset current amplifier, the capacitor voltage Vc is replicated across the sense resistor R_{ISEN}. Therefore, the current out of ISENB pin, I_{SEN}, is proportional to the inductor current.

Peak Current Limit

The ISL8115 contains a peak current limit circuit to protect the converter.

When a peak current limit occurs, the UG is turned off immediately. An internal counter begins to record the number of OC events detected. Two consecutive clock cycles without a current limit will reset the counter. If 8 consecutive clock cycles of overcurrent is detected, the ISL8115 enters into a hiccup mode. The ISL8115 operation during the peak current limit event is illustrated in Figure 26.

The sensed current signal and peak current signal in Figure 25 can be derived by the following equations:

$$I_{SEN} = \frac{I_L \cdot DCR}{R_{ISEN}} \quad \text{(EQ. 9)}$$

$$I_{SEN-PK} = \frac{\left(I_L + \frac{V_{out}}{L} \cdot \frac{1-D}{2F_{sw}}\right) \cdot DCR}{R_{ISEN}} \quad \text{(EQ. 10)}$$

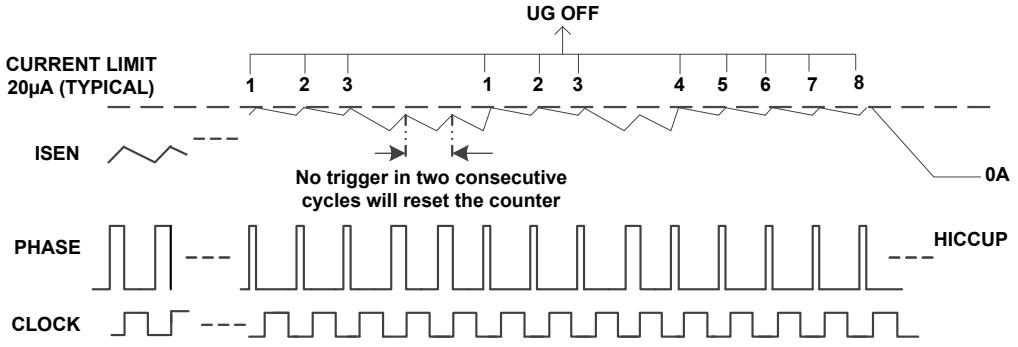


FIGURE 26. CURRENT LIMIT TIMING

Average Overcurrent Protection

The ISL8115 provides an average overcurrent protection circuit to protect the converter during an overcurrent fault.

The voltage on pin ISET represents the average inductor current signal which compares with an internal reference of 1.4V to implement positive overcurrent protection and 0.25V for negative current protection. If the overcurrent event is detected, the ISL8115 will enter hiccup mode. This consists of a 10ms shut down and then a restart. The voltage on pin ISET can be obtained from Equation 11. The circuit of average OCP is shown in Figure 27.

$$V_{ISET} = (5I_{SEN} + 50\mu A) \cdot R_{ISET} \quad \text{(EQ. 11)}$$

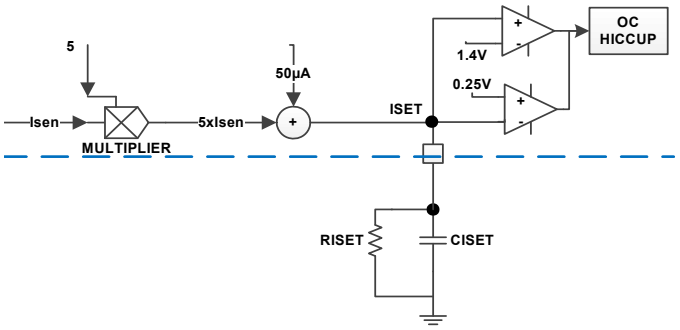


FIGURE 27. AVERAGE OCP CIRCUIT

Select a suitable R_{ISET} for setting the OCP trigger point. Also, a filer capacitor C_{ISET} is required in parallel with R_{ISET} to get the average inductor current signal.

Generally, set the average OCP trigger point lower than the peak current limit.

For example, L = 2.5µH; DCR = 1.6mΩ; I_{OUT} = 20A; di = 8A; F_{SW} = 220kHz. To set 24A as the output peak current limit. R_{SEN} can be derived by:

$$R_{SEN} = \frac{\left(I_{OC} + \frac{1}{2}di\right) \cdot DCR}{20uA} = \frac{(24A + 4A) \times 1.6m\Omega}{20uA} = 2.24k\Omega \quad \text{(EQ. 12)}$$

Considering DCR increases as the temperature rises. Select 3kΩ (2.24kΩ x 1.34) for R_{SEN}.

To set 22A for the average OCP, the value of R_{ISET} can be yield as:

$$R_{ISET} = \frac{1.4V}{\frac{22A \times 1.34DCR}{3k\Omega} \times 5 + 50uA} = 10.7k\Omega \quad \text{(EQ. 13)}$$

To filter the inductor ripple current and achieve the average inductor current signal from ISET, the roll off frequency of the low pass filter should be much lower than the switching frequency. Capacitor at ISET C_{ISET} is obtained by Equation 14:

$$\frac{1}{2\pi R_{ISET} \cdot C_{ISET}} < \frac{1}{10} \cdot F_{SW}$$

$$C_{ISET} > \frac{10}{F_{SW}} \cdot \frac{1}{2\pi R_{ISET}} = 0.68nF \quad \text{(EQ. 14)}$$

Select a 1nF Capacitor for C_{ISET}.

DEM

Diode emulation allows for higher converter efficiency under light load situations. With diode emulation active, the ISL8115 will detect the zero current crossing of the output inductor and turn off LGATE. This ensures that discontinuous conduction mode (DCM) is achieved. This prevents the low side MOSFET from sinking current and discharging of the output during pre-biased startup. DEM can only be disabled after soft-start. Please refer to the “Electrical Specifications” table on page 10 for the threshold of DEM.

Current Sharing

The ISL8115 can support up to 6 phase operation. Connecting the ISHARE pins together allows for communication between the phases. In a single phase application, the voltage on the ISHARE pin follows the ISET voltage and the ISHARE pin can be floated. However, in multi-phase applications, the voltage on the ISHARE bus represents the highest ISET voltage of all phases. This voltage becomes the current reference of each phase. Figure 28 illustrates the relation between ISHARE and ISET.

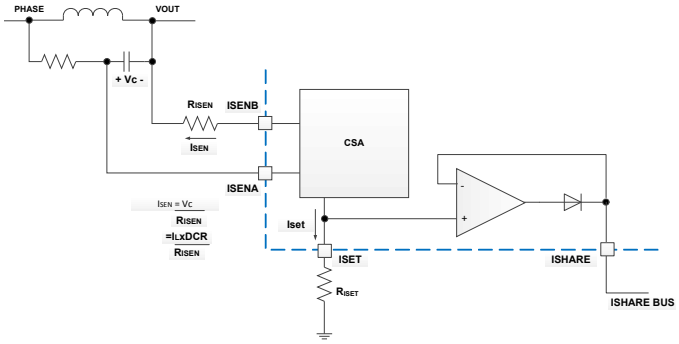


FIGURE 28. CURRENT SENSING BLOCK DIAGRAM

The voltage difference between ISHARE and ISET will create two correction currents (See Figure 29). One is Ish_corr1 which makes the COMP voltage increase and the other is Ish_corr2 which makes the RGND voltage increase. A resistor (typically 100Ω) connected between RGND and the output capacitor ground is required. The correction currents make the duty cycle increase thereby making the voltage at ISET track the voltage at ISHARE within 10mV of offset.

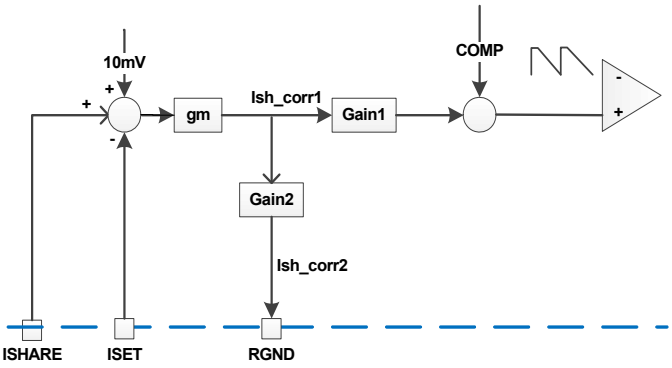


FIGURE 29. CURRENT SHARING BLOCK DIAGRAM

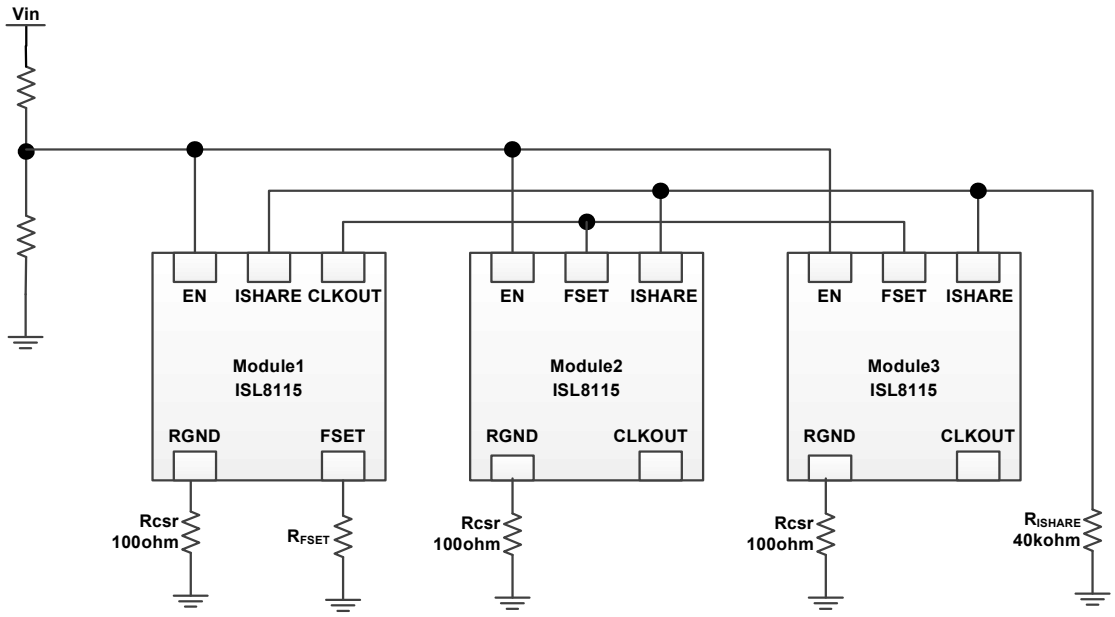


FIGURE 30. SIMPLIFIED MULTI-PHASE DIAGRAM

Figure 30 shows 3-phase operation. Device 1 is the master and the remaining devices are synchronized and phase shifted. The phase shift can be set using the CONF pin.

The ISHARE bus remains low until the PLL of all phases are locked. This assures that all phases start up at the same time, thereby preventing an overcurrent condition. A 40kΩ resistor is required between the ISHARE bus and ground.

Feedback Compensation

Figure 31 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the reference voltage level. The error amplifier output (V_{EA}) is compared with the oscillator (OSC) sawtooth waveform to provide a pulse-width modulated (PWM) signal with an amplitude of VIN at the PHASE node. The PWM signal is smoothed by the output filter (L_O and C_O).

This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

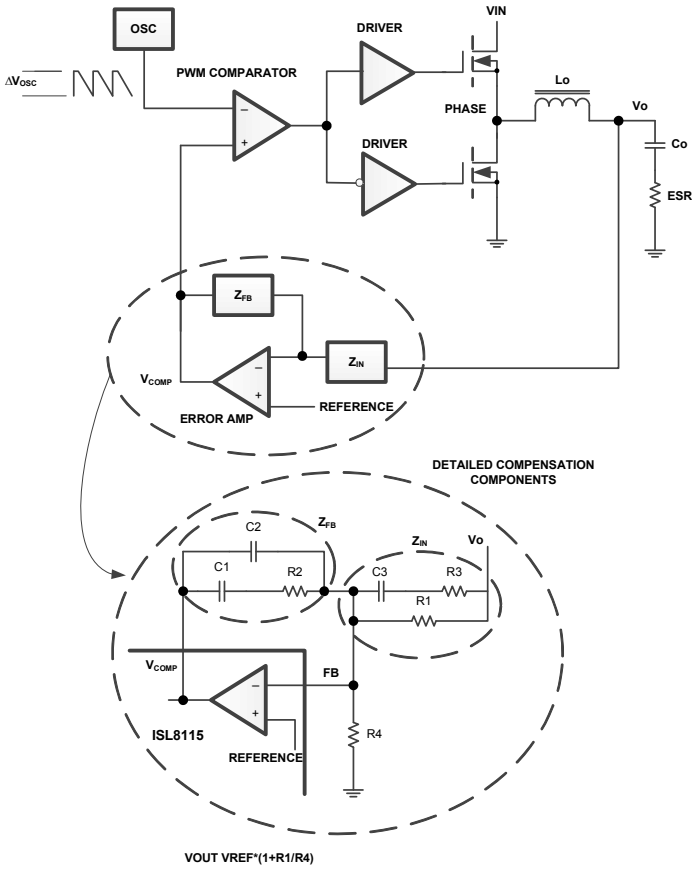


FIGURE 31. VOLTAGE- MODE BUCK CONVERTER COMPENSATION DESIGN

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \bullet \sqrt{L_O \bullet C_O}} \quad \text{(EQ. 15)}$$

$$F_{ESR} = \frac{1}{2\pi \bullet (ESR \bullet C_O)} \quad \text{(EQ. 16)}$$

The compensation network consists of the error amplifier (internal to the ISL8115) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180°. The following equations relate to the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 31. Use the following guidelines for locating the poles and zeros of the compensation network.

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \bullet R2 \bullet C1} \quad \text{(EQ. 17)}$$

$$F_{P1} = \frac{1}{2\pi \bullet R2 \bullet \left(\frac{C1 \bullet C2}{C1 + C2}\right)} \quad \text{(EQ. 18)}$$

$$F_{Z2} = \frac{1}{2\pi \bullet (R1 + R3) \bullet C3} \quad \text{(EQ. 19)}$$

$$F_{P2} = \frac{1}{2\pi \bullet R3 \bullet C3} \quad \text{(EQ. 20)}$$

1. Pick Gain (R2/R1) for desired converter bandwidth
2. Place 1ST Zero Below Filter's Double Pole (~75% F_{LC})
3. Place 2ND Zero at Filter's Double Pole
4. Place 1ST Pole at the ESR Zero
5. Place 2ND Pole at Half the Switching Frequency
6. Check Gain against Error Amplifier's Open-Loop Gain
7. Estimate Phase Margin - Repeat if Necessary

Figure 32 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 32. Using the previously mentioned guidelines should give a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The Loop Gain is constructed on the log-log graph of Figure 32 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

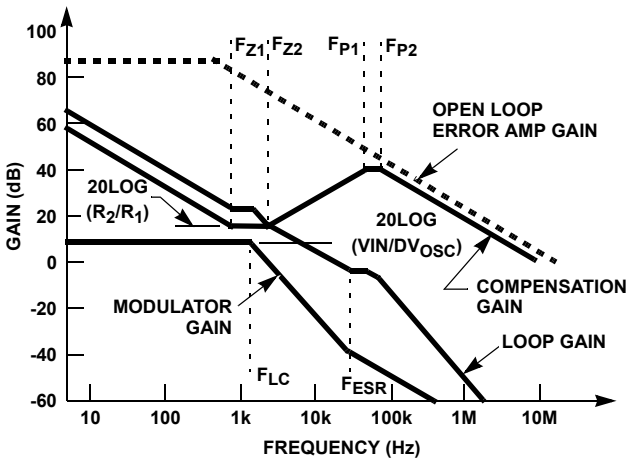


FIGURE 32. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin.

Component Selection Guidelines

OUTPUT CAPACITOR SELECTION

The output capacitors should be selected to meet the dynamic regulation requirements including ripple voltage and load transients. Selection of output capacitors is also dependent on the output inductor, thus some inductor analysis is required to select the output capacitors.

One of the parameters limiting the converter's response to a load transient is the time required for the inductor current to slew to its new level. The response time is the time interval required to slew the inductor current from an initial current value to the load current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). Minimizing the response time can minimize the output capacitance required. Also, if the load transient rise time is slower than the inductor response time, as in a hard drive or CD drive, it reduces the requirement on the output capacitor.

The maximum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is shown in Equation 21:

$$C_{OUT} = \frac{(L_O)(I_{TRAN})^2}{2(V_{IN} - V_O)(DV_{OUT})} \quad \text{(EQ. 21)}$$

where C_{OUT} is the output capacitor(s) required, L_O is the output inductor, I_{TRAN} is the transient load current step, V_{IN} is the input voltage, V_O is output voltage, and DV_{OUT} is the drop in output voltage allowed during the load transient.

High frequency capacitors initially supply the transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Equivalent Series Resistance) and voltage rating requirements as well as actual capacitance requirements.

The output voltage ripple is due to the inductor ripple current and the ESR of the output capacitors as defined by Equation 22:

$$V_{RIPPLE} = \Delta I_L(ESR) \quad \text{(EQ. 22)}$$

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load circuitry for specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. In most cases, multiple small-case electrolytic capacitors perform better than a single large-case capacitor.

OUTPUT INDUCTOR SELECTION

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current and output capacitor(s) ESR. The ripple current is approximated by Equation 23:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_S)(L_O)(V_{IN})} \quad \text{(EQ. 23)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient. Also, it always means more expensive and large size.

INPUT CAPACITOR SELECTION

The important parameters for the bulk input capacitor(s) are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25x greater than the maximum input voltage and 1.5x is a conservative guideline. The AC RMS Input current varies with the load. The total RMS current supplied by the input capacitance is given by Equation 24:

$$I_{RMSx} = \sqrt{I_O^2(D - D^2) + \frac{\Delta I_L^{\,2}}{12}D} \quad \text{(EQ. 24)}$$

where, D is duty cycle of the buck converter.

Use a mix of input bypass capacitors to control the voltage ripple across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

MOSFET SELECTION

The logic level MOSFETs are chosen for optimum efficiency given the potentially wide input voltage range and output power requirements, two N-Channel MOSFETs for the Buck converter. These MOSFETs should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

Compared with other components, MOSFETs contribute significant power loss to the converter. Power loss of high side FET includes switching losses, conduction losses and gate charge losses. Low side FET contributes conduction losses and gate charge losses too, also reverse recovery loss and loss of the body diode during dead time should be considered.

Power loss of high side MOSFET can be expressed as:

$$P_H = \left(I_o^2 + \frac{\Delta I_L^{\,2}}{12}\right) \cdot D \cdot R_{DS(on)} + V_{IN} I_o t_{sw} F_{sw} + V_{IN} Q_H F_{sw} \quad \text{(EQ. 25)}$$

where $t_{sw}$is switching interval includes on and off intervals. Q_H is gate charge of the high side MOSFET.

Power loss of low side MOSFET derived as:

$$P_L = \left(I_o^2 + \frac{\Delta I_L^{\,2}}{12}\right) \cdot (1 - D) \cdot R_{DS(on)} + V_{IN} Q_{rr} F_{sw} + V_{IN} Q_L F_{sw} \quad \text{(EQ. 26)}$$

where Q_{rr} is the total reverse recovery charge. Q_L is gate charge of the low side MOSFET.

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding.

Figure 33 shows the critical power components of the buck converter. To minimize the voltage overshoot the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in Figure 33 should be located as close together as possible. Please note that the capacitors C_{IN} and C_O each represent numerous physical capacitors. Locate the ISL8115 within 3 inches of the MOSFETs, Q_1 and Q_2. The circuit traces for the MOSFETs' gate and source connections from the ISL8115 must be sized to handle up to 4A peak current.

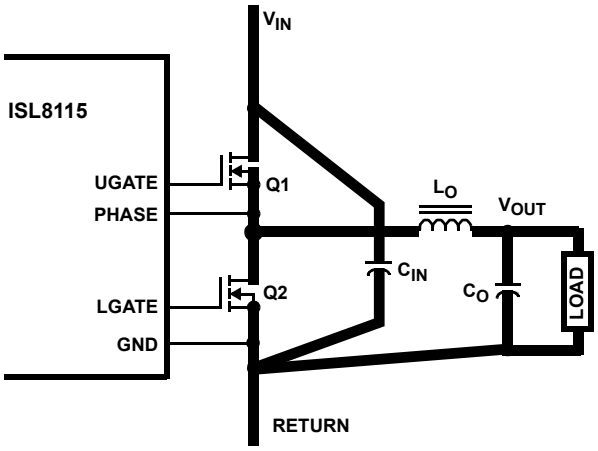


FIGURE 33. CRITICAL POWER TRAIN LOOP

Figure 34 shows the current sensing loop of the ISL8115 which is a sensitive analog loop needs “quiet and clean environment”. To minimize the coupling from switching nodes, using differential pair as the sensing route. R should be located close to the inductor; C and RISEN should be close to the IC.

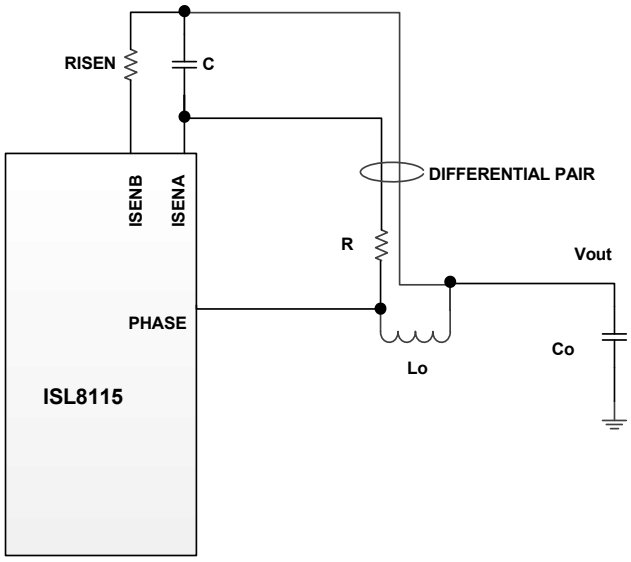


FIGURE 34. CURRENT SENSING LOOP

General PowerPAD Design Considerations

Figure 35 is an example of how to use vias to remove heat from the IC.

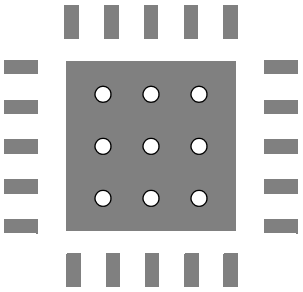


FIGURE 35. PCB VIA PATTERN

We recommend you fill the thermal pad area with vias. A typical via array would be to fill the thermal pad footprint with space, such that they are center on center 3x the radius apart from each other. Keep the Vias small but not so small that their inside diameter prevents solder wicking through the holes during reflow.

Connect all vias to the ground plane. It is important the vias have a low thermal resistance for efficient heat transfer. It is important to have a complete connection of the plated through-hole to each plane.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
September 23, 2013	FN8272.1	Initial Release.

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

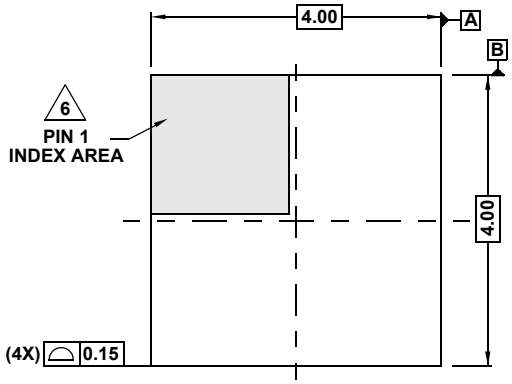
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

Package Outline Drawing

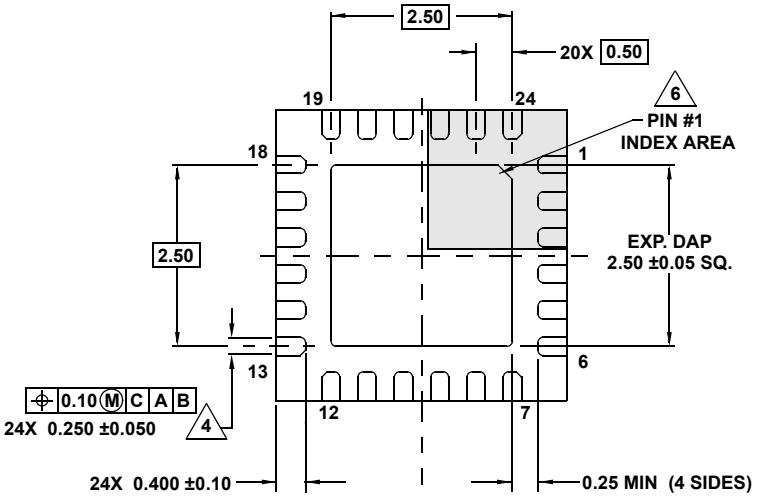
L24.4X4F

24 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

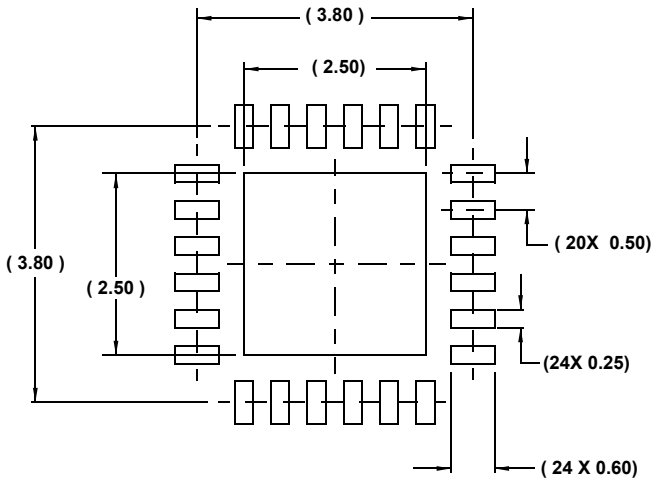
Rev 2, 1/11



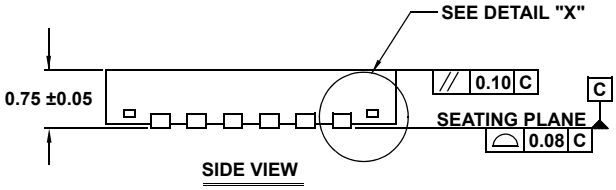
TOP VIEW



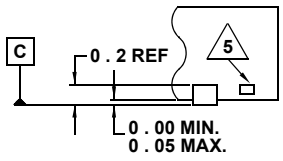
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-220 VGGD-8.