WAN PLL WITH SINGLE REFERENCE INPUT

IDT82V3001A

FEATURES

- Supports AT&T TR62411 and Telcordia GR-1244-CORE Stratum 4 Enhanced and Stratum 4 timing for DS1 interfaces
- Supports ETSI ETS 300 011, TBR 4, TBR 12 and TBR 13 timing for E1 interface
- Selectable input reference signal: 8 kHz, 1.544 MHz or 2.048 MHz
- Provides eight types of clock signals: C1.5o, **$\overline{\text{C3o}}$**, C2o, **$\overline{\text{C4o}}$**, C6o, C8o, **$\overline{\text{C16o}}$** and **$\overline{\text{C32o}}$**
- Provides six types of 8 kHz framing pulses: **$\overline{\text{F0o}}$**, F8o, **$\overline{\text{F16o}}$**, **$\overline{\text{F32o}}$**, RSP and TSP
- Holdover frequency accuracy of 0.025 ppm
- Phase slope of 5 ns/125 µs
- Attenuates wander from 2.1 Hz
- Fast Lock mode
- Provides Time Interval Error (TIE) correction
- MTIE of 600 ns
- JTAG boundary scan
- Holdover status indication
- Freerun status indication
- Normal status indication
- Lock status indication
- 3.3 V operation with 5 V tolerant I/O
- Package available: 56-pin SSOP (Green option available)

DESCRIPTION

The IDT82V3001A is a WAN PLL with single reference input. It contains a Digital Phase-Locked Loop (DPLL), which generates ST-BUS clocks and framing signals that are phase locked to a 2.048 MHz, 1.544 MHz or 8 kHz input reference.

The IDT82V3001A provides eight types of clock signals (C1.5o, $\overline{\text{C3o}}$, C6o, C2o, $\overline{\text{C4o}}$, C8o, $\overline{\text{C16o}}$, $\overline{\text{C32o}}$) and six types of framing signals ($\overline{\text{F0o}}$, F8o, $\overline{\text{F16o}}$, $\overline{\text{F32o}}$, RSP, TSP) for the multitrunk T1 and E1 primary rate transmission links.

The IDT82V3001A is compliant with AT&T TR62411, Telcordia GR-1244-CORE Stratum 4 Enhanced and Stratum 4, ETSI ETS 300 011. It meets the jitter/wander tolerance, jitter/wander transfer, intrinsic jitter/wander, frequency accuracy, capture range, phase change slope, holdover frequency accuracy and MTIE (Maximum Time Interval Error) requirements for these specifications.

The IDT82V3001A can be used in synchronization and timing control for T1 and E1 systems, or used as ST-BUS clock and frame pulse sources. It can also be used in access switch, access routers, ATM edge switches, wireless base station controllers, or IADs (Integrated Access Devices), PBXs and line cards.

FUNCTIONAL BLOCK DIAGRAM

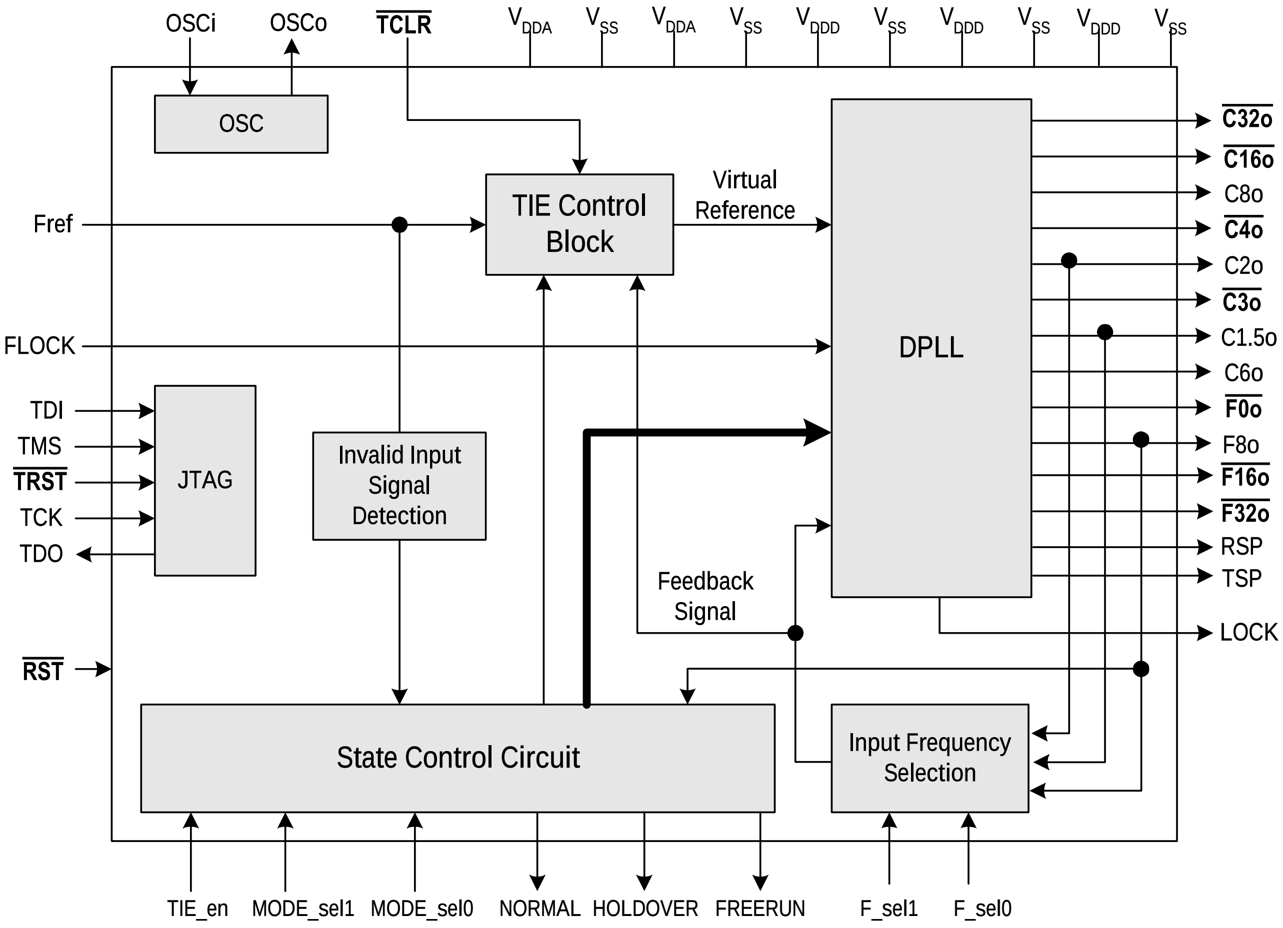


Figure - 1 Block Diagram

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 IDT82V3001A PIN CONFIGURATION

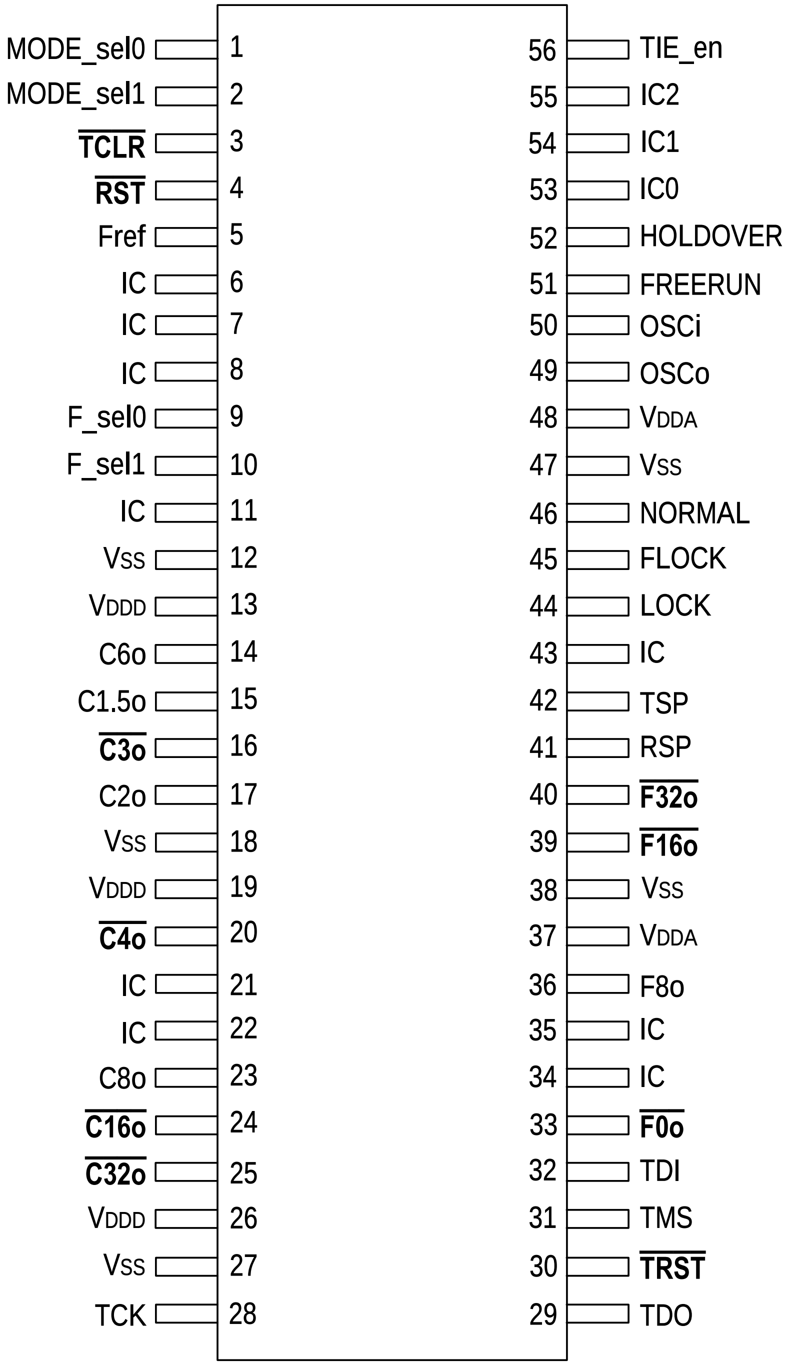


Figure - 2 IDT82V3001A SSOP56 Package Pin Assignment

2 PIN DESCRIPTION

Table - 1 Pin Description

Name	Type	Pin Number	Description
V_{SS}	Power	12, 18, 27, 38, 47	Ground. 0 V. All V_{SS} pins should be connected to the ground.
V_{DDA}	Power	37, 48	3.3 V Analog Power Supply. Refer to Chapter 3.9 Power Supply Filtering Techniques.
V_{DDD}	Power	13, 19, 26	3.3 V Digital Power Supply. Refer to Chapter 3.9 Power Supply Filtering Techniques.
OSCo	(CMOS) O	49	Oscillator Master Clock. This pin is left unconnected.
OSCi	(CMOS) I	50	Oscillator Master Clock. This pin is connected to a clock source.
Fref	I	5	Reference Input. This is the input reference source (falling edge) used for synchronization. One of three possible frequencies (8 kHz, 1.544 MHz, or 2.048 MHz) may be used. The Fref pin is internally pulled up to V_{DDD}.
F_sel1	I	10	Input Frequency Select 1. This input, in conjunction with F_sel0, determines which of three possible frequencies (8 kHz, 1.544 MHz, or 2.048 MHz) may be input to the Reference Input.
F_sel0	I	9	Input Frequency Select 0. See above.
MODE_sel1	I	2	Mode/Control Select 1. This input, in conjunction with MODE_sel0, determines the operation mode of the IDT82V3001A (Normal, Holdover or Freerun) . The logic level at this input is gated in by the rising edge of F8o. This pin is internally pulled down to V_{SS}. See Table - 2.
MODE_sel0	I	1	Mode/Control Select 0. See above. The logic level at this input is gated in by the rising edge of F8o. This pin is internally pulled down to V_{SS}.
$\overline{\mathrm{RST}}$	I	4	Reset Input. A logic low at this pin resets the IDT82V3001A. To ensure proper operation, the device must be reset after the frequency of the input reference is changed and power-up. The $\overline{\mathrm{RST}}$ pin should be held low for a minimum of 300 ns. While the $\overline{\mathrm{RST}}$ pin is low, all framing and clock outputs are at logic high.
$\overline{\mathrm{TCLR}}$	I	3	TIE Circuit Reset. Logic low at this input resets the TIE (Time Interval Error) control block, resulting in a realignment of output phase with input phase. The $\overline{\mathrm{TCLR}}$ pin should be held low for a minimum of 300 ns. This pin is internally pulled up to V_{DDD}.
TIE_en	I	56	TIE Enable. A logic high at this pin enables the TIE control block while a logic low at this pin disables the TIE control block. The logic level at this input is gated in by the rising edge of F8o. This pin is internally pulled down to V_{SS}.
FLOCK	I	45	Fast Lock Mode. Set high to allow the DPLL to quickly lock to the input reference (less than 500 ms locking time).
LOCK	(CMOS) O	44	Lock Indicator. This output goes high when the DPLL is frequency locked to the input reference.
HOLDOVER	(CMOS) O	52	Holdover Indicator. This output goes to a logic high whenever the DPLL goes into Holdover Mode.
NORMAL	(CMOS) O	46	Normal Indicator. This output goes to a logic high whenever the DPLL goes into Normal Mode.
FREERUN	(CMOS) O	51	Freerun Indicator. This output goes to a logic high whenever the DPLL goes into Freerun Mode.

Table - 1 Pin Description (Continued)

Name	Type	Pin Number	Description
$\overline{\text{C32o}}$	(CMOS) O	25	Clock 32.768 MHz. This output is a 32.768 MHz clock used for ST-BUS operation.
$\overline{\text{C16o}}$	(CMOS) O	24	Clock 16.384 MHz. This output is a 16.384 MHz clock used for ST-BUS operation.
C8o	(CMOS) O	23	Clock 8.192 MHz. This output is an 8.192 MHz clock used for ST-BUS operation.
$\overline{\text{C4o}}$	(CMOS) O	20	Clock 4.096 MHz. This output is a 4.096 MHz clock used for ST-BUS operation.
C2o	(CMOS) O	17	Clock 2.048 MHz. This output is a 2.048 MHz clock used for ST-BUS operation.
$\overline{\text{C3o}}$	(CMOS) O	16	Clock 3.088 MHz. This output is a 3.088 MHz clock used for T1 applications.
C1.5o	(CMOS) O	15	Clock 1.544 MHz. This output is a 1.544 MHz clock used for T1 applications.
C6o	(CMOS) O	14	Clock 6.312 MHz. This output is a 6.312 MHz clock used for DS2 applications.
$\overline{\text{F32o}}$	(CMOS) O	40	Frame Pulse ST-BUS 8.192 Mb/s. This is an 8 kHz 31 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 8.192 Mb/s.
$\overline{\text{F16o}}$	(CMOS) O	39	Frame Pulse ST-BUS 8.192 Mb/s. This is an 8 kHz 61 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 8.192 Mb/s.
F8o	(CMOS) O	36	Frame Pulse. This is an 8 kHz 122 ns active high framing pulse, which marks the beginning of a frame.
$\overline{\text{F0o}}$	(CMOS) O	33	Frame Pulse ST-BUS 2.048 Mb/s. This is an 8 kHz 244 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 2.048 Mb/s and 4.096 Mb/s.
RSP	(CMOS) O	41	Receive Sync Pulse. This is an 8 kHz 488 ns active high framing pulse, which marks the beginning of an ST-BUS frame. This is typically used to connect to Siemens MUNICH-32 device.
TSP	(CMOS) O	42	Transmit Sync Pulse. This is an 8 kHz 488 ns active high framing pulse, which marks the beginning of an ST-BUS frame. This is typically used to connect to Siemens MUNICH-32 device.
TDO	(CMOS) O	29	Test Serial Data Out. JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state if JTAG scan is not enabled.
TDI	I	32	Test Serial Data In. JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DDD}.
$\overline{\text{TRST}}$	I	30	Test Reset. Asynchronously initializes the JTAG TAP controller by putting it in Test-Logic-Reset state. This pin is internally pulled up to V_{DDD}. It is connected to the ground for normal applications.
TCK	I	28	Test Clock. Provides a clock to JTAG test logic.
TMS	I	31	Test Mode Select. JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DDD}.
IC0, IC1, IC2	-	53, 54, 55	Internal Connection. Internal Use. These pins should be connected to V_{SS} when in normal operation.

Table - 1 Pin Description (Continued)

Name	Type	Pin Number	Description
IC	-	6, 7, 8, 11, 21, 22, 34 35, 43	Internal Connection. Internal Use. These pins should be left open when in normal operation.

3 FUNCTIONAL DESCRIPTION

The IDT82V3001A is a WAN PLL with single reference input, providing timing (clock) and synchronization (framing) signals to interface circuits for T1 and E1 Primary Rate Digital Transmission links. See Figure - 1. The detail is described in the following sections.

3.1 STATE CONTROL CIRCUIT

The State Control Circuit is an important part of the IDT82V3001A. As shown in Figure - 3, the State Control Circuit outputs signals to enable/disable the TIE Control Block and control the operation mode of the DPLL Block based on MODE_sel0 and MODE_sel1 and TIE_en pins.

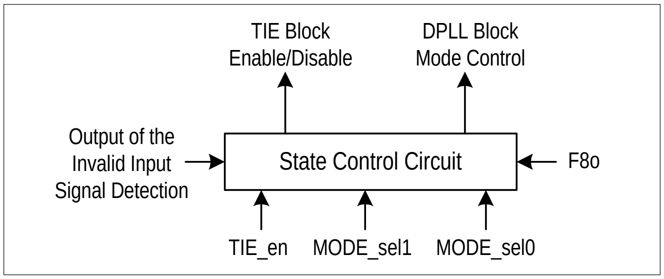


Figure - 3 State Control Block

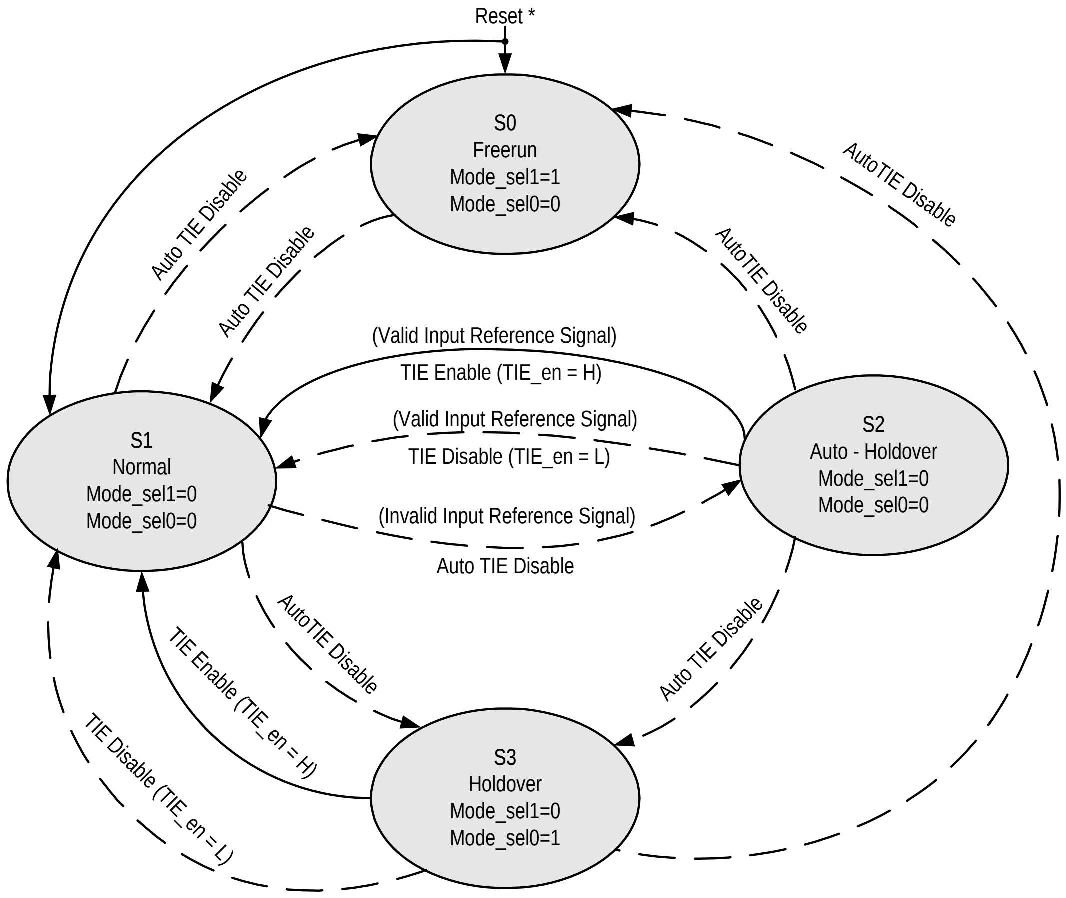
The IDT82V3001A has three possible modes of operation: Normal, Holdover and Freerun. The mode selection pins, MODE_sel1 and MODE_sel0 select the operation mode. See Table - 2.

Table - 2 Operating Modes and Status

MODE_sel1	MODE_sel0	Mode
0	0	Normal
0	1	Holdover
1	0	Freerun
1	1	Reserved

All state control changes occur synchronously on the rising edge of F8o. As shown in Figure - 4, the operating mode can be changed from one to another by the MODE_sel0 and MODE_sel1 pins, except the mode changes between Normal (S1) and Auto-Holdover (S2). The mode changes between Normal (S1) and Auto-Holdover (S2) are triggered by the Invalid Input Reference Detection Circuit and irrelative to the MODE_sel0 and MODE_sel1 pins. That is, at the stage of S1, the operating mode will be changed automatically from Normal (S1) to Auto-Holdover (S2) if an invalid input reference is detected (input reference is out of the capture range). If the input reference becomes valid (within the capture range), the operating mode will be changed back to Normal (S1) automatically.

When the operating mode is changed from one to another, the TIE control block will be disabled automatically as shown in Figure - 4, except the change from Holdover (S3) or Auto-Holdover (S2) to Normal (S1). In the case of changing from Holdover (S3) or Auto-Holdover (S2) to Normal (S1), the TIE control block can be manually enabled or disabled by the TIE_en pin, as required.



* Note: After reset, Mode_sel1 and Mode_sel0 should be initially set to '10' or '00'.

Figure - 4 State Control Diagram

3.1.1 NORMAL MODE

Normal Mode is typically used when a slave clock source synchronized to the network is required.

In this mode, the IDT82V3001A provides timing (C1.5o, $\overline{\text{C3o}}$, C2o, $\overline{\text{C4o}}$, C6o, C8o, $\overline{\text{C16o}}$ and $\overline{\text{C32o}}$) and synchronization ($\overline{\text{F0o}}$, F8o, $\overline{\text{F16o}}$, $\overline{\text{F32o}}$, TSP, RSP) signals, which are synchronous to the input reference. The input reference signal has a nominal frequency of 8 kHz, 2.048 MHz or 1.544 MHz.

From a reset condition, the IDT82V3001A will take 30 seconds at most to make the output signals synchronous (phase locked) to the input reference.

Whenever the IDT82V3001A enters Normal Mode, it will give an indication by setting the NORMAL pin to high.

3.1.2 FAST LOCK MODE

Fast Lock Mode is a submode of Normal Mode. It is used to allow the IDT82V3001A to lock to a reference more quickly than Normal Mode will do. Typically, the DPLL will lock to the input reference within 500 ms if the FLOCK pin is high.

3.1.3 HOLDOVER MODE

Holdover Mode is typically used for short duration (e.g., 2 seconds) while network synchronization is temporarily disrupted.

In Holdover Mode, the IDT82V3001A provides timing and synchronization signals, which are not locked to the external reference signal but based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to the external reference signal.

In Normal Mode, when the output signal is locked to the input reference signal, a numerical value corresponding to the output frequency is stored alternately in two memory locations every 30 ms. When the device is switched into Holdover Mode, the stored value in memory from between 30 ms and 60 ms is used to set the output frequency of the device.

The frequency accuracy in Holdover Mode is ±0.025 ppm, which corresponds to the worst case of 18 frame (125 µs per frame) slips in 24 hours. This meets AT&T TR62411 requirement of ±0.37 ppm (255 frame slips per 24 hours).

The HOLDOVER pin will be set to logic high whenever the IDT82V3001A goes into Holdover Mode.

3.1.4 FREERUN MODE

Freerun Mode is typically used when a master clock source is required, or a system is just powered up and the network synchronization has not been achieved.

In Freerun Mode, the IDT82V3001A provides timing and synchronization signals which are based on the master clock frequency (OSCi) only and not synchronized to the input reference signal.

The accuracy of the output clock is equal to the accuracy of the master clock (OSCi). So if a ±32 ppm output clock is required, the master clock must also be ±32 ppm. Refer to "OSC" section for more information.

The FREERUN pin will go high whenever the IDT82V3001A works in Freerun Mode.

3.2 FREQUENCY SELECT CIRCUIT

The IDT82V3001A accepts one reference input signal, Fref, and operates on its falling edge. The input reference can be 8 kHz, 1.544 MHz or 2.048 MHz. As shown in Table - 3, the F_sel1 and F_sel0 pins determine which of the three frequencies is selected. Every time the frequency is changed, the device must be reset to make the change effective.

Table - 3 Input Reference Frequency Selection

F_sel1	F_sel0	Input Frequency
0	0	Reserved
0	1	8 kHz
1	0	1.544 MHz
1	1	2.048 MHz

3.3 INVALID INPUT SIGNAL DETECTION

This circuit monitors the input reference signal into the IDT82V3001A. The IDT82V3001A will automatically enter Holdover Mode (Auto-Holdover) if the incoming reference signal is out of the capture range (See Table - 7), including a complete loss of input reference, or a large frequency shift in the input reference. When the input reference returns to normal, the DPLL will return to Normal Mode. In Holdover Mode, the output signal of the IDT82V3001A is based on the output signal 30 ms to 60 ms prior to entering Holdover Mode. The amount of phase drift in Holdover Mode is negligible because Holdover Mode is very accurate (e.g., 0.025 ppm). Consequently, the phase delay between the input and output after switching back to Normal Mode is preserved.

3.4 TIE CONTROL BLOCK

If the current reference is badly damaged or lost, it is necessary to use the reference generated by the storage techniques instead. But when switching the operation mode, a step change in phase on the input reference will occur. And a step change in phase at the input of the DPLL would lead to unacceptable phase changes in the output signals. The TIE control block, when enabled, prevents a step change in phase on the input reference signals from causing a step change in phase at the output of the DPLL block. Figure - 5 shows the TIE Control Block diagram.

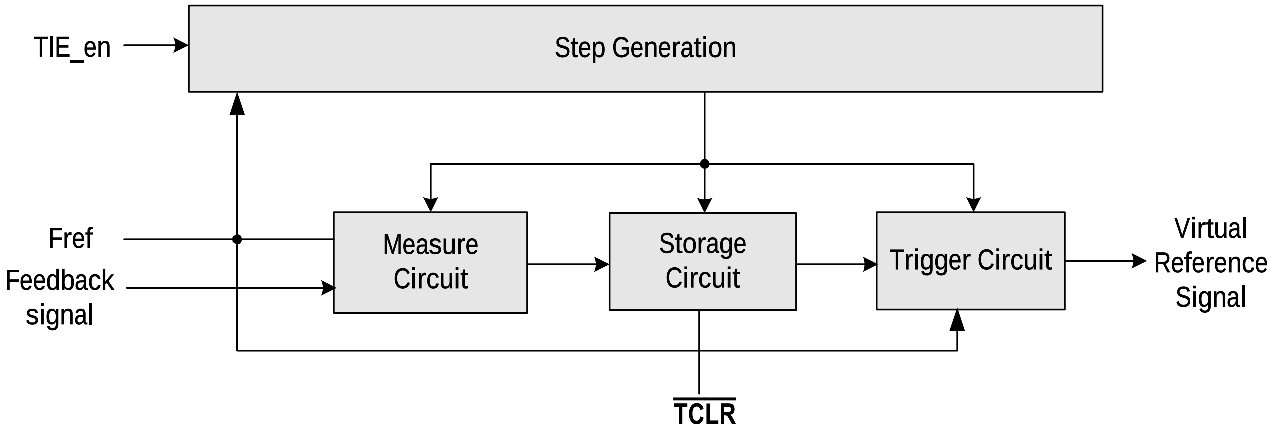


Figure - 5 TIE Control Circuit Diagram

The TIE Control Block will work under the control of the Step Generation circuit when it is enabled manually or automatically (by the TIE_en pin or TIE auto-enable logic generated by the State Control Circuit).

The input reference signal is compared with the feedback signal (current output feedback from the Frequency Select Circuit) by the Measure Circuit. The phase difference between the input reference and the feedback signal is sent to the Storage Circuit for TIE correction. The Trigger Circuit generates a virtual reference with the phase corrected to the same position as the previous reference according to the value stored in the Storage Circuit. With this TIE correction mechanism, the reference is switched without generating a step change in phase.

Figure - 6 shows the phase transient that would result if a state switch is performed with the TIE Control Block enabled.

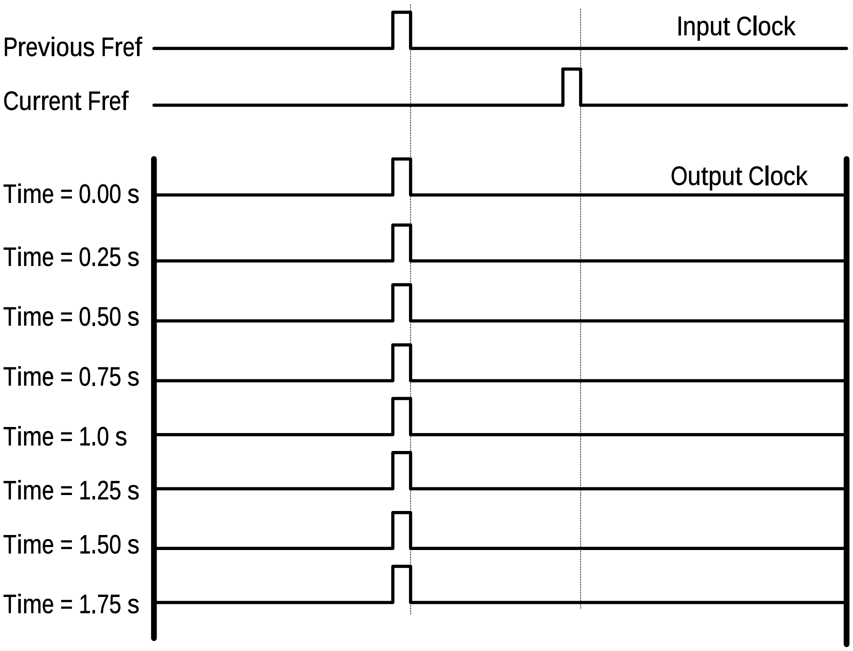


Figure - 6 State Switch with TIE Control Block Enabled

The phase difference in the Storage Circuit can be cleared by applying a logic low pulse to the $\overline{\text{TCLR}}$ pin. The reset pulse should be at least 300 ns.

When the IDT82V3001A primarily enters Holdover Mode for short time periods and then turns back to Normal Mode, the TIE Control Circuit should not be enabled. This will prevent undesired accumulated phase change between the input and output.

If the TIE Control Block is disabled manually or automatically during state switching, the phase of the output signal will align with that of the new reference. The phase slope limited to 5 ns per 125 µs. Figure - 7 shows the phase transient resulting from a state switch with the TIE Control Block disabled.

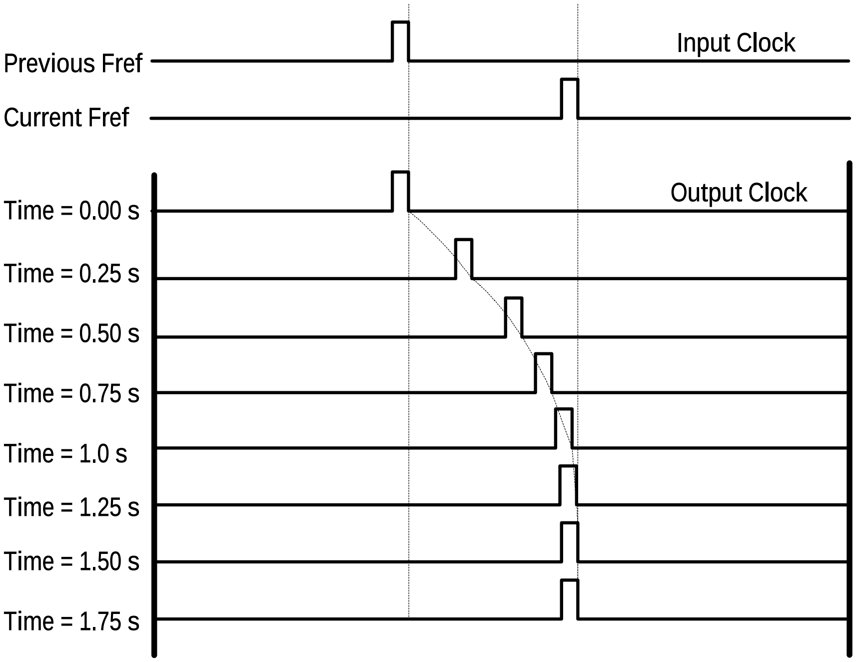


Figure - 7 State Switch with TIE Control Block Disabled

3.5 DPLL BLOCK

As shown in Figure - 8, the DPLL Block consists of a Phase Detector, a Limiter, a Loop Filter, a Digital Control Oscillator and Dividers.

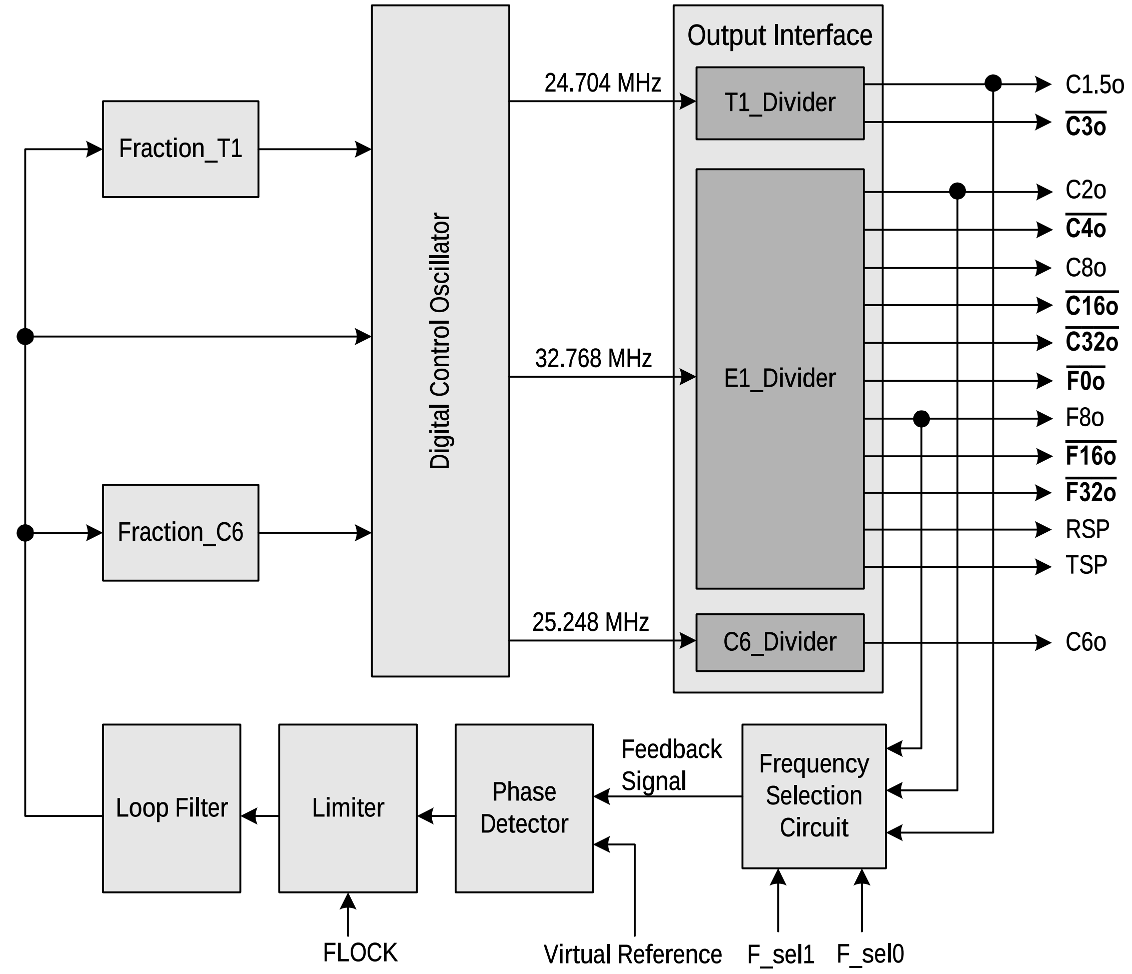


Figure - 8 DPLL Block Diagram

3.5.1 PHASE DETECTOR (PHD)

In Normal Mode, the Phase Detector compares the virtual reference signal from the TIE Control Circuit with the feedback signal from the Frequency Select Circuit, and outputs an error signal corresponding to the phase difference between the two. This error signal is then sent to the Limiter circuit for phase slope control.

The feedback signal can be 8 kHz, 2.048 MHz or 1.544 MHz, as selected by F_sel1 and F_sel0 pins. Refer to Table - 3 for details.

In Freerun or Holdover Mode, the Frequency Select Circuit, the Phase Detector and the Limiter are not active and the input reference signal is not used.

3.5.2 LIMITER

The Limiter is used to ensure that the DPLL responds to all input transient conditions with a maximum output phase slope of 5 ns per 125 µs. This well meets AT&T TR62411 and Telcordia GR-1244-CORE specifications, which specify the maximum phase slope of 7.6 ns per 125 µs and 81 ns per 1.326 ms respectively.

In Normal Mode, the Limiter receives the error signal from the Phase Detector, limits the phase slope within 5 ns per 125 µs and sends the limited signal to the Loop Filter.

The fast lock mode is a submode of Normal Mode. By setting the FLOCK pin to high, the device will enter fast lock mode. In this mode, the Limiter is disabled and the DPLL will lock to the incoming reference within 500 ms.

3.5.3 LOOP FILTER

The Loop Filter ensures that the jitter transfer meets ETS 300 011 and AT&T TR62411 requirements. This Loop Filter works similarly to a first order low pass filter with 2.1 Hz cutoff frequency for the three valid input reference signals (8 kHz, 2.048 MHz or 1.544 MHz).

The output of the Loop Filter goes to the Digital Control Oscillator directly or via the Fraction blocks, in which E1, T1 and C6 signals are generated.

3.5.4 FRACTION BLOCK

By applying some algorithms to the incoming E1 signal, the Fraction_C6 and Fraction_T1 blocks generate C6 and T1 signals respectively.

3.5.5 DIGITAL CONTROL OSCILLATOR (DCO)

In Normal Mode, the DCO receives three limited and filtered signals from Loop Filter or Fraction blocks. Based on the received signals, the DCO generates three digital outputs, 25.248 MHz, 32.768 MHz and 24.704 MHz for C6, E1 and T1 divider respectively.

In Holdover mode, the DCO is running at the same frequency which is generated by using the storage techniques.

In Freerun mode, the DCO is running at the same frequency as that of the master clock.

3.5.6 LOCK INDICATOR

In Normal Mode, the LOCK pin will be set to high only when the following equation is satisfied:

$$|f_{out} - f_{in}| \leq 0.4 \text{ ppm}$$

f_{out} = the average frequency of the output clock signal from the DPLL (within 2 seconds)

f_{in} = the average frequency of the input reference (within 2 seconds)

In other operation modes, the LOCK pin remains low.

3.5.7 OUTPUT INTERFACE

The Output Interface uses three output signals of the DCO to generate eight types of clock signals and six types of framing signals totally.

The 32.768 MHz signal is used by the E1_divider to generate five types of clock signals (C2o, $\overline{\text{C4o}}$, C8o, $\overline{\text{C16o}}$ and $\overline{\text{C32o}}$) with nominal 50% duty cycle and six types of framing signals (F0o, F8o, $\overline{\text{F16o}}$, $\overline{\text{F32o}}$, RSP and TSP).

The 24.704 MHz signal is used by the T1_divider to generate two types of T1 signals (C1.5o and $\overline{\text{C3o}}$) with nominal 50% duty cycle.

The 25.248 MHz signal is used by the C6_divider to generate a C6o signal with nominal 50% duty cycle.

All these output signals are synchronous to F8o.

3.6 OSC

The IDT82V3001A can use a clock as the master timing source.

In Freerun Mode, the frequency tolerance at the clock outputs is identical to that of the source at the OSCi pin. For applications not requiring an accurate Freerun Mode, the tolerance of the master timing source may be ±100 ppm. For applications requiring an accurate Freerun Mode, such as AT&T TR62411, the tolerance of the master timing source must be no greater than ±32 ppm.

The desired capture range should be taken into consideration when determining the accuracy of the master timing source. The sum of the accuracy of the master timing source and the capture range of the IDT82V3001A will always equal 230 ppm. For example, if the master timing source is 100 ppm, the capture range will be 130 ppm.

3.6.1 CLOCK OSCILLATOR

When selecting a clock oscillator, numerous parameters must be considered, including absolute frequency, frequency change over temperature, output rise and fall times, output levels and duty cycle.

For applications requiring ±32 ppm clock accuracy, the following clock oscillator module may be used.

FOX F7C-2E3-20.0 MHz

Frequency:	20 MHz
Tolerance:	25 ppm 0°C to 70°C
Rise & Fall Time:	10 ns (0.33 V 2.97 V 15 pF)
Duty Cycle:	40% to 60%

The output clock should be connected directly (not AC coupled) to the OSCi input of the IDT82V3001A, and the OSCo output should be left open as shown in Figure - 9.

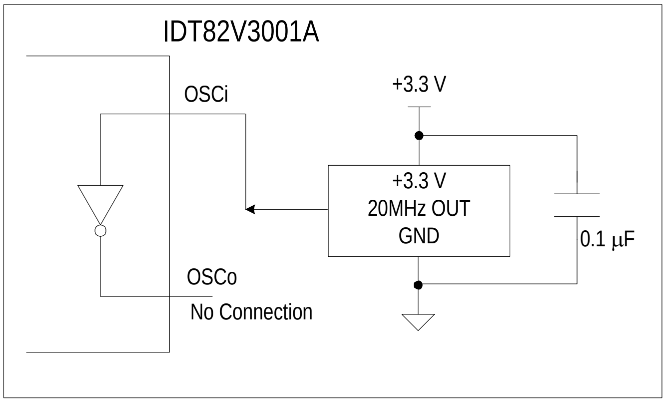


Figure - 9 Clock Oscillator Circuit

3.7 JTAG

The IDT82V3001A supports IEEE 1149.1 JTAG Scan.

3.8 RESET CIRCUIT

A simple power up reset circuit is shown in Figure - 10. Resistor Rp is used for protection only and limits current into the $\overline{\text{RST}}$ pin during power down conditions. The reset low time is not critical but should be greater than 300 ns. In Figure - 10, the reset low time is about 50 µs.

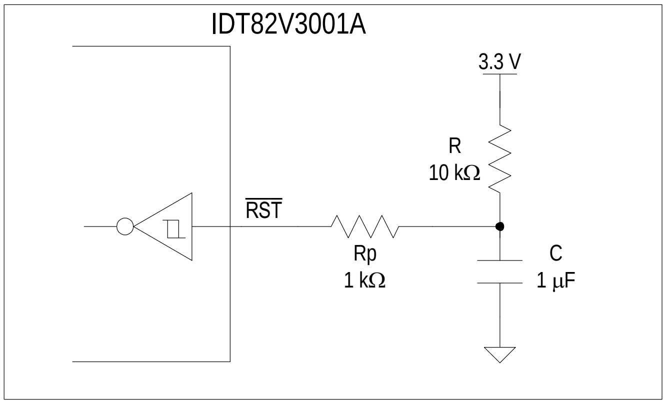


Figure - 10 Power-Up Reset Circuit

3.9 POWER SUPPLY FILTERING TECHNIQUES

To achieve optimum jitter performance, power supply filtering is required to minimize supply noise modulation of the output clocks. The common sources of power supply noise are switching power supplies and the high switching noise from the outputs to the internal PLL. The 82V3001A provides separate power pins: V_{DDA} and V_{DDD}. V_{DDA} pins are for the internal analog PLL, and V_{DDD} pins are for the core logic as well as I/O driver circuits.

To minimize switching power supply noise generated by the switching regulator, the power supply output should be filtered with sufficient bulk capacity to minimize ripple and 0.1 uF (0402 case size, ceramic) capacitors to filter out the switching transients.

For the 82V3001A, the decoupling for V_{DDA} and V_{DDD} are handled individually. V_{DDD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. Figure - 11 illustrates how bypass capacitor and ferrite bead should be connected to each power pin.

The analog power supply V_{DDA} should have low impedance. This can be achieved by using one 10 uF (1210 case size, ceramic) and at least two 0.1 uF (0402 case size, ceramic) capacitors in parallel. The 0.1 uF (0402 case size, ceramic) capacitors must be placed next to the V_{DDA} pins and as close as possible. Note that the 10 uF capacitor must be of 1210 case size, and it must be ceramic for lowest possible ESR (Effective Series Resistance). The 0.1 uF should be of case size 0402, which offers the lowest ESL (Effective Series Inductance) to achieve low impedance towards the high speed range.

For V_{DDD}, at least three 0.1 uF (0402 case size, ceramic) and one 10 uF (1210 case size, ceramic) capacitors are recommended. The 0.1 uF capacitors should be placed as close to the V_{DDD} pins as possible.

Please refer to evaluation board schematic for details.

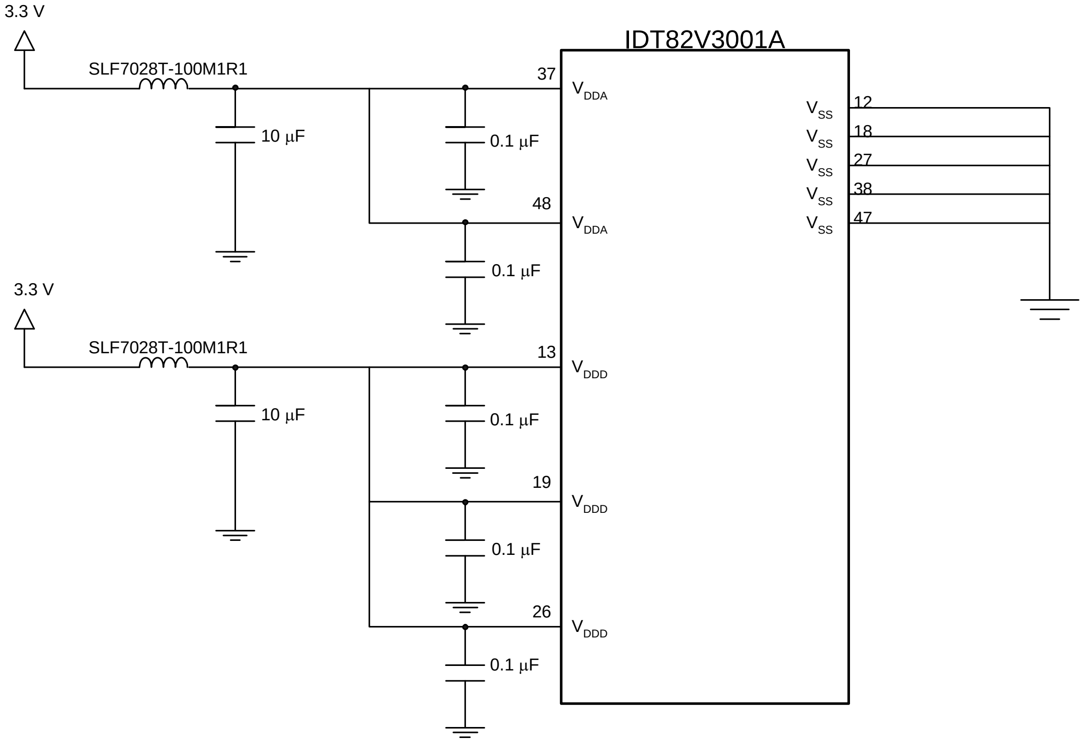


Figure - 11 IDT82V3001A Power Decoupling Scheme

4 MEASURES OF PERFORMANCE

The following are some synchronizer performance indicators and their corresponding definitions.

4.1 INTRINSIC JITTER

Intrinsic jitter is the jitter produced by the synchronizing circuit and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Intrinsic jitter may also be measured when the device is in a non-synchronizing mode, such as free running or holdover, by measuring the output jitter of the device. Intrinsic jitter is usually measured with various band limiting filters depending on the applicable standards. In the IDT82V3001A, the intrinsic Jitter is limited to less than 0.02 UI on the 2.048 MHz and 1.544 MHz clocks.

4.2 JITTER TOLERANCE

Jitter tolerance is a measure of the ability of a DPLL to operate properly (i.e., remain in lock and or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and jitter frequency depends on the applicable standards.

4.3 JITTER TRANSFER

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

For the IDT82V3001A, two internal elements determine the jitter attenuation. This includes the internal 2.1 Hz low pass loop filter and the phase slope limiter. The phase slope limiter limits the output phase slope to 5 ns/125 µs. Therefore, if the input signal exceeds this rate, such as for very large amplitude low frequency input jitter, the maximum output phase slope will be limited (i.e., attenuated) to 5 ns/125 µs.

The IDT82V3001A has fourteen outputs with three possible input frequencies for a total of 42 possible jitter transfer functions. Since all outputs are derived from the same signal, the jitter transfer values for three cases, 8 kHz to 8 kHz, 1.544 MHz to 1.544 MHz and 2.048 MHz to 2.048 MHz can be applied to all outputs.

It should be noted that 1 UI at 1.544 MHz is 644 ns, which is not equal to 1 UI at 2.048 MHz, which is 488 ns. Consequently, a transfer value using different input and output frequencies must be calculated in common units (e.g., seconds).

Using the above method, the jitter attenuation can be calculated for all combinations of input and outputs based on the three jitter transfer functions provided. Note that the resulting jitter transfer functions for all combinations of input (8 kHz, 1.544 MHz, 2.048 MHz) and outputs (8 kHz, 1.544 MHz, 3.088 MHz, 6.312 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz, 32.768 MHz) for a given input signal (jitter frequency and jitter amplitude) are the same.

Since intrinsic jitter is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g., 75% of the specified maximum jitter tolerance).

4.4 FREQUENCY ACCURACY

Frequency accuracy is defined as the absolute tolerance of an output clock signal when it is not locked to an external reference, but is operating in a free running mode. For the IDT82V3001A, the Freerun accuracy is equal to the Master Clock (OSCi) accuracy.

4.5 HOLDOVER ACCURACY

Holdover accuracy is defined as the absolute tolerance of an output clock signal, when it is not locked to an external reference signal, but is operating using storage techniques. For the IDT82V3001A, the storage value is determined while the device is in Normal Mode and locked to an external reference signal.

The absolute Master Clock (OSCi) accuracy of the IDT82V3001A does not affect Holdover accuracy, but the change in OSCi accuracy while in Holdover Mode does.

4.6 CAPTURE RANGE

Also referred to as pull-in range. This is the input frequency range over which the synchronizer must be able to pull into synchronization. The IDT82V3001A capture range is equal to ±230 ppm minus the accuracy of the master clock (OSCi). For example, a 32 ppm master clock results in a capture range of 198 ppm.

4.7 LOCK RANGE

This is the input frequency range over which the synchronizer must be able to maintain synchronization. The lock range is equal to the capture range for the IDT82V3001A.

4.8 PHASE SLOPE

Phase slope is measured in seconds per second and is the rate at which a given signal changes phase with respect to an ideal signal. The given signal is typically the output signal. The ideal signal is of constant frequency and is nominally equal to the value of the final output signal or final input signal.

4.9 TIME INTERVAL ERROR (TIE)

TIE is the time delay between a given timing signal and an ideal timing signal.

4.10 MAXIMUM TIME INTERVAL ERROR (MTIE)

MTIE is the maximum peak to peak delay between a given timing signal and an ideal timing signal within a particular observation period.

4.11 PHASE CONTINUITY

Phase continuity is the phase difference between a given timing signal and an ideal timing signal at the end of a particular observation period. Usually, the given timing signal and the ideal timing signal are of the same frequency. Phase continuity applies to the output of the synchronizer after a signal disturbance due to a mode change. The observation period is usually the time from the disturbance, to just after the synchronizer has settled to a steady state.

In the case of the IDT82V3001A, the output signal phase continuity is maintained to within ±5 ns at the instance (over one frame) of all mode changes. The total phase shift, depending on the type of mode change, may accumulate up to 200 ns over many frames. The rate of change of the 200 ns phase shift is limited to a maximum phase slope of approximately 5 ns/125 µs. This meets AT&T TR62411 maximum phase slope requirement of 7.6 ns/125 µs and Telcordia GR-1244-CORE (81 ns/1.326 ms).

4.12 PHASE LOCK TIME

This is the time it takes the synchronizer to phase lock to the input signal. Phase lock occurs when the input signal and output signal are not changing in phase with respect to each other (not including jitter).

Lock time is very difficult to determine because it is affected by many factors, which include:

i) Initial input to output phase difference
ii) Initial input to output frequency difference
iii) Synchronizer loop filter
iv) Synchronizer limiter

Although a short lock time is desirable, it is not always possible to achieve due to other synchronizer requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time. And better (smaller) phase slope performance (limiter) results in longer lock times. The IDT82V3001A loop filter and limiter were optimized to meet AT&T TR62411 jitter transfer and phase slope requirements. Consequently, phase lock time, which is not a standards requirement, may be longer than in other applications. See Table - 7 for Maximum Phase Lock Time.

The IDT82V3001A provides a fast lock pin (FLOCK), which enables the DPLL to lock to an incoming reference within approximately 500 ms when set high.

5 TEST SPECIFICATIONS

Table - 4 Absolute Maximum Ratings**

Rating	Min.	Max.	Unit
Power Supply Voltage	-0.5	5.0	V
Voltage on Any Pin with Respect to Ground	-0.5	V_{DDD} + 0.5	V
Package Power Dissipation		200	mW
Storage Temperature	-55	125	°C

Note:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table - 5 Recommended DC Operating Conditions**

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature	-40		+85	°C
Power Supply Voltage	3.0		3.6	V

Table - 6 DC Electrical Characteristics**

Parameter	Description	Min	Typ.	Max	Units	Test Conditions
I_{DDS}	Supply current with OSCi = 0 V			10	mA	Outputs unloaded
I_{DD}	Supply current with OSCi = Clock			60	mA	Outputs unloaded
V_{CIH}	CMOS high-level input voltage	$0.7V_{DDD}$			V	OSCi, Fref
V_{CIL}	CMOS low-level input voltage			$0.3V_{DDD}$	V	OSCi, Fref
V_{TIH}	TTL high-level input voltage	2.0			V	All input pins except for OSCi and Fref
V_{TIL}	TTL low-level input voltage			0.8	V	All input pins except for OSCi and Fref
I_{IL}	Input leakage current: Normal (low level) Normal (high level) Pull up (low level) Pull up (high level) Pull down (low level) Pull down (high level)	 -15 -15 -100 -15 -15 0		 15 15 0 15 15 100	µA	$V_I = V_{DDD}$ or 0 V
V_{OH}	High-level output voltage	2.4			V	I_{OH} = 8 mA
V_{OL}	Low-level output voltage			0.4	V	I_{OL} = 8 mA

5.1 AC ELECTRICAL CHARACTERISTICS**

Table - 7 Performance

Description	Min	Typ.	Max	Units	Test Conditions / Notes*
Freerun Mode accuracy with OSCi at : 0 ppm	-0		+0	ppm	3-6
Freerun Mode accuracy with OSCi at : ±32 ppm	-32		+32	ppm	3-6
Freerun Mode accuracy with OSCi at : ±100 ppm	-100		+100	ppm	3-6
Holdover Mode accuracy with OSCi at : 0 ppm	-0.025		+0.025	ppm	2, 4-6, 38, 39
Holdover Mode accuracy with OSCi at : ±32 ppm	-0.025		+0.025	ppm	2, 4-6, 38, 39
Holdover Mode accuracy with OSCi at : ±100 ppm	-0.025		+0.025	ppm	2, 4-6, 38, 39
Capture range with OSCi at : 0 ppm	-230		+230	ppm	1, 4-6
Capture range with OSCi at : ±32 ppm	-198		+198	ppm	1, 4-6
Capture range with OSCi at : ±100 ppm	-130		+130	ppm	1, 4-6
Phase lock time		50		s	1, 4-12, 40
Output phase continuity with mode switch to Normal			200	ns	2-12
Output phase continuity with mode switch to Freerun			200	ns	3-12
Output phase continuity with mode switch to Holdover			50	ns	1, 4-12
MTIE (maximum time interval error)			600	ns	1-12, 25
Output phase slope			40	µs/s	1-12, 25
Reference input for Auto-Holdover with 8 kHz	-18 k		+18 k	ppm	1, 4, 7-9
Reference input for Auto-Holdover with 1.544 MHz	-36 k		+36 k	ppm	1, 5, 7-9
Reference input for Auto-Holdover with 2.048 MHz	-36 k		+36 k	ppm	1, 6, 7-9

**Note:
Voltages are with respect to ground (V_{SS}) unless otherwise stated.

Table - 8 Intrinsic Jitter Unfiltered

Description	Min	Typ	Max	Units	Test Conditions / Notes*
Intrinsic jitter at F8o (8 kHz)			0.0001	UIpp	1-12, 19-22, 26
Intrinsic jitter at $\overline{\text{F0o}}$ (8 kHz)			0.0001	UIpp	1-12, 19-22, 26
Intrinsic jitter at $\overline{\text{F16o}}$ (8 kHz)			0.0001	UIpp	1-12, 19-22, 26
Intrinsic jitter at C1.5o (1.544 MHz)			0.015	UIpp	1-12, 19-22, 27
Intrinsic jitter at $\overline{\text{C3o}}$ (3.088 MHz)			0.03	UIpp	1-12, 19-22, 29
Intrinsic jitter at C2o (2.048 MHz)			0.01	UIpp	1-12, 19-22, 28
Intrinsic jitter at C6o (6.312 MHz)			0.06	UIpp	1-12, 19-22
Intrinsic jitter at $\overline{\text{C4o}}$ (4.096 MHz)			0.02	UIpp	1-12, 19-22, 30
Intrinsic jitter at C8o (8.192 MHz)			0.04	UIpp	1-12, 19-22, 31
Intrinsic jitter at $\overline{\text{C16o}}$ (16.834 MHz)			0.04	UIpp	1-12, 19-22, 32
Intrinsic jitter at TSP (8 kHz)			0.0001	UIpp	1-12, 19-22, 32
Intrinsic jitter at RSP (8 kHz)			0.0001	UIpp	1-12, 19-22, 32
Intrinsic jitter at $\overline{\text{C32o}}$ (32.768 MHz)			0.08	UIpp	1-12, 19-22, 33

Table - 9 C1.5o (1.544 MHz) Intrinsic Jitter Filtered

Description	Min	Typ	Max	Units	Test Conditions / Notes*
Intrinsic jitter (4 Hz to 100 kHz filter)			0.008	UIpp	1-12, 19-22, 27
Intrinsic jitter (10 Hz to 40 kHz filter)			0.006	UIpp	1-12, 19-22, 27
Intrinsic jitter (8 kHz to 40 kHz filter)			0.006	UIpp	1-12, 19-22, 27
Intrinsic jitter (10 Hz to 8 kHz filter)			0.003	UIpp	1-12, 19-22, 27

Table - 10 C2o (2.048 MHz) Intrinsic Jitter Filtered

Description	Min	Typ	Max	Units	Test Conditions / Notes*
Intrinsic jitter (4 Hz to 100 kHz filter)			0.005	UIpp	1-12, 19-22, 28
Intrinsic jitter (10 Hz to 40 kHz filter)			0.004	UIpp	1-12, 19-22, 28
Intrinsic jitter (8 kHz to 40 kHz filter)			0.003	UIpp	1-12, 19-22, 28
Intrinsic jitter (10 Hz to 8 kHz filter)			0.002	UIpp	1-12, 19-22, 28

Table - 11 8 kHz Input to 8 kHz Output Jitter Transfer

Description	Min	Typ	Max	Units	Test Conditions / Notes*
Jitter attenuation for 1 Hz@0.01 UIpp input	0		6	dB	1, 5, 7-12, 19-20, 22, 27, 33
Jitter attenuation for 1 Hz@0.54 UIpp input	6		16	dB	1, 5, 7-12, 19-20, 22, 27, 33
Jitter attenuation for 10 Hz@0.10 UIpp input	15		22	dB	1, 5, 7-12, 19-20, 22, 27, 33
Jitter attenuation for 60 Hz@0.10 UIpp input	32		38	dB	1, 5, 7-12, 19-20, 22, 27, 33
Jitter attenuation for 300 Hz@0.10 UIpp input	42			dB	1, 5, 7-12, 19-20, 22, 27, 33
Jitter attenuation for 3600 Hz@0.005 UIpp input	50			dB	1, 5, 7-12, 19-20, 22, 27, 33

Table - 12 1.544 MHz Input to 1.544 MHz Output Jitter Transfer

Description	Min	Typ	Max	Units	Test Conditions / Notes*
Jitter attenuation for 1 Hz@20 UIpp input	0		6	dB	1-3, 7, 9-14, 21-22, 24, 29, 35
Jitter attenuation for 1 Hz@104 UIpp input	6		16	dB	1-3, 7, 9-14, 21-22, 24, 29, 35
Jitter attenuation for 10 Hz@20 UIpp input	17		22	dB	1-3, 7, 9-14, 21-22, 24, 29, 35
Jitter attenuation for 60 Hz@20 UIpp input	33		38	dB	1-3, 7, 9-14, 21-22, 24, 29, 35
Jitter attenuation for 300 Hz@20 UIpp input	45			dB	1-3, 7, 9-14, 21-22, 24, 29, 35
Jitter attenuation for 10 kHz@0.3 UIpp input	48			dB	1-3, 7, 9-14, 21-22, 24, 29, 35
Jitter attenuation for 40 kHz@0.3 UIpp input	50			dB	1-3, 7, 9-14, 21-22, 24, 29, 35

Table - 13 2.048 MHz Input to 2.048 MHz Output Jitter Transfer

Description	Min	Typ	Max	Units	Test Conditions / Notes*
Jitter at output for 1 Hz@3.00 UIpp input			2.5	UIpp	1, 6, 7-12, 19-20, 22, 28, 33
Jitter at output for 1 Hz@3.00 UIpp input with 40 Hz to 100 Hz filter			0.07	UIpp	1, 6, 7-12, 19-20, 22, 28, 34
Jitter at output for 3 Hz@2.33 UIpp input			1.4	UIpp	1, 6, 7-12, 19-20, 22, 28, 33
Jitter at output for 3 Hz@2.33 UIpp input with 40 Hz to 100 Hz filter			0.10	UIpp	1, 6, 7-12, 19-20, 22, 28, 34
Jitter at output for 5 Hz@2.07 UIpp input			0.90	UIpp	1, 6, 7-12, 19-20, 22, 28, 33
Jitter at output for 5 Hz@2.07 UIpp input with 40 Hz to 100 Hz filter			0.10	UIpp	1, 6, 7-12, 19-20, 22, 28, 34
Jitter at output for 10 Hz@1.76 UIpp input			0.40	UIpp	1, 6, 7-12, 19-20, 22, 28, 33
Jitter at output for 10 Hz@1.76 UIpp input with 40 Hz to 100 Hz filter			0.10	UIpp	1, 6, 7-12, 19-20, 22, 28, 34
Jitter at output for 100 Hz@1.50 UIpp input			0.06	UIpp	1, 6, 7-12, 19-20, 22, 28, 33
Jitter at output for 100 Hz@1.50 UIpp input with 40 Hz to 100 Hz filter			0.05	UIpp	1, 6, 7-12, 19-20, 22, 28, 34
Jitter at output for 2400 Hz@1.50 UIpp input			0.04	UIpp	1, 6, 7-12, 19-20, 22, 28, 33
Jitter at output for 2400 Hz@1.50 UIpp input with 40 Hz to 100 Hz filter			0.03	UIpp	1, 6, 7-12, 19-20, 22, 28, 34
Jitter at output for 100 kHz@0.20 UIpp input			0.04	UIpp	1, 6, 7-12, 19-20, 22, 28, 33
Jitter at output for 100 kHz@0.20 UIpp input with 40 Hz to 100 Hz filter			0.02	UIpp	1, 6, 7-12, 19-20, 22, 28

Table - 14 8 kHz Input Jitter Tolerance

Description	Min	Typ	Max	Units	Test Conditions / Notes*
Jitter tolerance for 1 Hz input	0.80			UIpp	1, 4, 7-12, 19-20, 22-24, 26
Jitter tolerance for 5 Hz input	0.70			UIpp	1, 4, 7-12, 19-20, 22-24, 26
Jitter tolerance for 20 Hz input	0.60			UIpp	1, 4, 7-12, 19-20, 22-24, 26
Jitter tolerance for 300 Hz input	0.16			UIpp	1, 4, 7-12, 19-20, 22-24, 26
Jitter tolerance for 400 Hz input	0.14			UIpp	1, 4, 7-12, 19-20, 22-24, 26
Jitter tolerance for 700 Hz input	0.07			UIpp	1, 4, 7-12, 19-20, 22-24, 26
Jitter tolerance for 2400 Hz input	0.02			UIpp	1, 4, 7-12, 19-20, 22-24, 26
Jitter tolerance for 3600 Hz input	0.01			UIpp	1, 4, 7-12, 19-20, 22-24, 26

Table - 15 1.544 MHz Input Jitter Tolerance

Description	Min	Typ	Max	Units	Test Conditions / Notes*
Jitter tolerance for 1 Hz input	150			UIpp	1, 5, 7-12, 19-20, 22-24, 27
Jitter tolerance for 5 Hz input	140			UIpp	1, 5, 7-12, 19-20, 22-24, 27
Jitter tolerance for 20 Hz input	130			UIpp	1, 5, 7-12, 19-20, 22-24, 27
Jitter tolerance for 300 Hz input	38			UIpp	1, 5, 7-12, 19-20, 22-24, 27
Jitter tolerance for 400 Hz input	25			UIpp	1, 5, 7-12, 19-20, 22-24, 27
Jitter tolerance for 700 Hz input	15			UIpp	1, 5, 7-12, 19-20, 22-24, 27
Jitter tolerance for 2400 Hz input	5			UIpp	1, 5, 7-12, 19-20, 22-24, 27
Jitter tolerance for 10 kHz input	1.2			UIpp	1, 5, 7-12, 19-20, 22-24, 27
Jitter tolerance for 40 kHz input	0.5			UIpp	1, 5, 7-12, 19-20, 22-24, 27

Table - 16 2.048 MHz Input Jitter Tolerance

Description	Min	Typ	Max	Units	Test Conditions / Notes*
Jitter tolerance for 1 Hz input	150			UIpp	1, 6, 7-12, 19-20, 22-24, 28
Jitter tolerance for 5 Hz input	140			UIpp	1, 6, 7-12, 19-20, 22-24, 28
Jitter tolerance for 20 Hz input	130			UIpp	1, 6, 7-12, 19-20, 22-24, 28
Jitter tolerance for 300 Hz input	40			UIpp	1, 6, 7-12, 19-20, 22-24, 28
Jitter tolerance for 400 Hz input	33			UIpp	1, 6, 7-12, 19-20, 22-24, 28
Jitter tolerance for 700 Hz input	18			UIpp	1, 6, 7-12, 19-20, 22-24, 28
Jitter tolerance for 2400 Hz input	5.5			UIpp	1, 6, 7-12, 19-20, 22-24, 28
Jitter tolerance for 10 kHz input	1.3			UIpp	1, 6, 7-12, 19-20, 22-24, 28
Jitter tolerance for 100 kHz input	0.4			UIpp	1, 6, 7-12, 19-20, 22-24, 28

*Notes:

Voltages are with respect to ground (V_{SS}) unless otherwise stated.
Supply voltage and operating temperature are as per Recommended Operating Conditions.
Timing parameters are as per AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

1. Normal Mode selected.
2. Holdover Mode selected.
3. Freerun Mode selected.
4. 8 kHz Frequency Mode selected.
5. 1.544 MHz Frequency Mode selected.
6. 2.048 MHz Frequency Mode selected.
7. Master clock input OSCi at 20 MHz ±0 ppm.
8. Master clock input OSCi at 20 MHz ±32 ppm.
9. Master clock input OSCi at 20 MHz ±100 ppm.
10. Selected reference input at ±0 ppm.
11. Selected reference input at ±32 ppm.
12. Selected reference input at ±100 ppm.
13. For Freerun Mode of ±0 ppm.
14. For Freerun Mode of ±32 ppm.
15. For Freerun Mode of ±100 ppm.
16. For capture range of ±230 ppm.
17. For capture range of ±198 ppm.
18. For capture range of ±130 ppm.
19. 25 pF capacitive load.
20. OSCi Master Clock jitter is less than 2 nspp, or 0.04 UIpp where 1 UIpp = 1/20 MHz.
21. Jitter on reference input is obtained at slightly higher input jitter amplitudes.
22. Applied jitter is sinusoidal.
23. Minimum applied input jitter magnitude to regain synchronization.
24. Loss of synchronization is obtained at slightly higher input jitter amplitudes.
25. Within 10 ms of the state, reference or input change.
26. 1 UIpp = 125 µs for 8 kHz signals.
27. 1 UIpp = 648 ns for 1.544 MHz signals.
28. 1 UIpp = 488 ns for 2.048 MHz signals.
29. 1 UIpp = 323 ns for 3.088 MHz signals.
30. 1 UIpp = 244 ns for 4.096 MHz signals.
31. 1 UIpp = 122 ns for 8.192 MHz signals.
32. 1 UIpp = 61 ns for 16.484 MHz signals.
33. 1 UIpp = 30 ns for 32.968 MHz signals.
34. No filter.
35. 40 Hz to 100 kHz bandpass filter.
36. With respect to reference input signal frequency.
37. After chip reset or TIE reset.
38. Master clock duty 40% to 60%.
39. Prior to Holdover Mode, device as in Normal Mode and phase locked.
40. With input frequency offset of 100 ppm.

6 TIMING CHARACTERISTICS

Table - 17 Timing Parameter Measurement Voltage Levels

Parameter	Description	CMOS	Units
V_T	Threshold Voltage	$0.5V_{DDD}$	V
V_{HM}	Rise and Fall Threshold Voltage High	$0.7V_{DDD}$	V
V_{LM}	Rise and Fall Threshold Voltage Low	$0.3V_{DDD}$	V

Notes:

1. Voltages are with respect to ground (V_{SS}) unless otherwise stated.
2. Supply voltage and operating temperature are as per Recommended Operating Conditions.
3. Timing for input and output signals is based on the worst case result of the CMOS thresholds

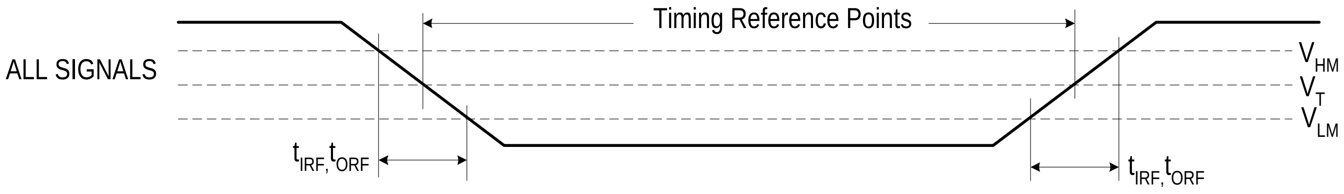


Table - 18 Input / Output Timing

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t_{RW}	Reference input pulse width high or low	51			ns	
t_{IRF}	Reference input rise or fall time			10	ns	
t_{R8D}	8 kHz reference input to F8o delay		8		ns	
t_{R15D}	1.544 MHz reference input to F8o delay		332		ns	
t_{R2D}	2.048 MHz reference input to F8o delay		253		ns	
t_{F0D}	F8o to $\overline{\text{F0o}}$ delay	118	121	124	ns	
t_{F16S}	$\overline{\text{F16o}}$ setup to $\overline{\text{C16o}}$ falling	25		40	ns	
t_{F16H}	$\overline{\text{F16o}}$ hold to $\overline{\text{C16o}}$ falling	25		40	ns	
t_{C15D}	F8o to C1.5o delay	-3	0	+3	ns	
t_{C3D}	F8o to $\overline{\text{C3o}}$ delay	-3	1.6	+3	ns	
t_{C6D}	F8o to C6o delay	-3	1.6	+3	ns	
t_{C2D}	F8o to C2o	-2	0	+2	ns	
t_{C4D}	F8o to $\overline{\text{C4o}}$	-2	0	+2	ns	
t_{C8D}	F8o to C8o delay	-2	0	+2	ns	
t_{C16D}	F8o to $\overline{\text{C16o}}$ delay	-2	0	+2	ns	
t_{C32D}	F8o to $\overline{\text{C32o}}$ delay	-2	2	+2	ns	
t_{TSPD}	F8o to TSP delay	-3	0	+3	ns	
t_{RSPD}	F8o to RSP delay	-3	0	+3	ns	
t_{C15W}	C1.5o pulse width high or low		323		ns	
t_{C3W}	$\overline{\text{C3o}}$ pulse width high or low		161		ns	
t_{C6W}	C6o pulse width high or low		82		ns	

Table - 18 Input / Output Timing (Continued)

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t_{C2W}	C2o pulse width high or low		244		ns	
t_{C4W}	$\overline{\text{C4o}}$ pulse width high or low		122		ns	
t_{C8W}	C8o pulse width high or low		61		ns	
t_{C16WL}	$\overline{\text{C16o}}$ pulse width high or low		30.5		ns	
t_{C32WH}	$\overline{\text{C32o}}$ pulse width high		14.4		ns	
t_{TSPW}	TSP pulse width high		486		ns	
t_{RSPW}	RSP pulse width high		490		ns	
t_{F0WL}	$\overline{\text{F0o}}$ pulse width low		243		ns	
t_{F8WH}	F8o pulse width high		123.6		ns	
t_{F16WL}	$\overline{\text{F16o}}$ pulse width low		60.9		ns	
t_{0RF}	Output clock and frame pulse rise or fall time		3		ns	
t_S	Input Controls Setup Time	100			ns	
t_H	Input Controls Hold Time	100			ns	
t_{F16D}	F8o to $\overline{\text{F16o}}$ delay	27.1	30.1	33.1	ns	
t_{F32D}	F8o to $\overline{\text{F32o}}$ delay	12	15.8	19	ns	
t_{F32S}	$\overline{\text{F32o}}$ setup to $\overline{\text{C32o}}$ falling	11			ns	
t_{F32H}	$\overline{\text{F32o}}$ hold to $\overline{\text{C32o}}$ falling	11			ns	
t_{F32WL}	$\overline{\text{F32o}}$ pulse width low		30.6		ns	

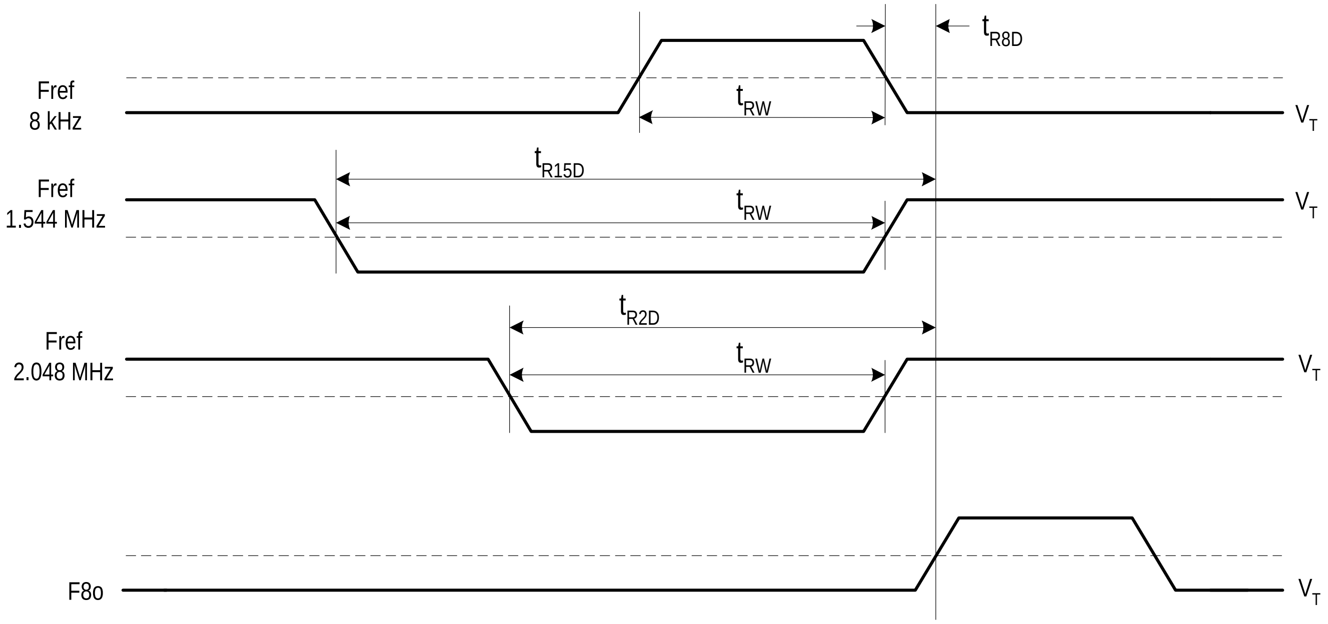


Figure - 12 Input to Output Timing (Normal Mode)

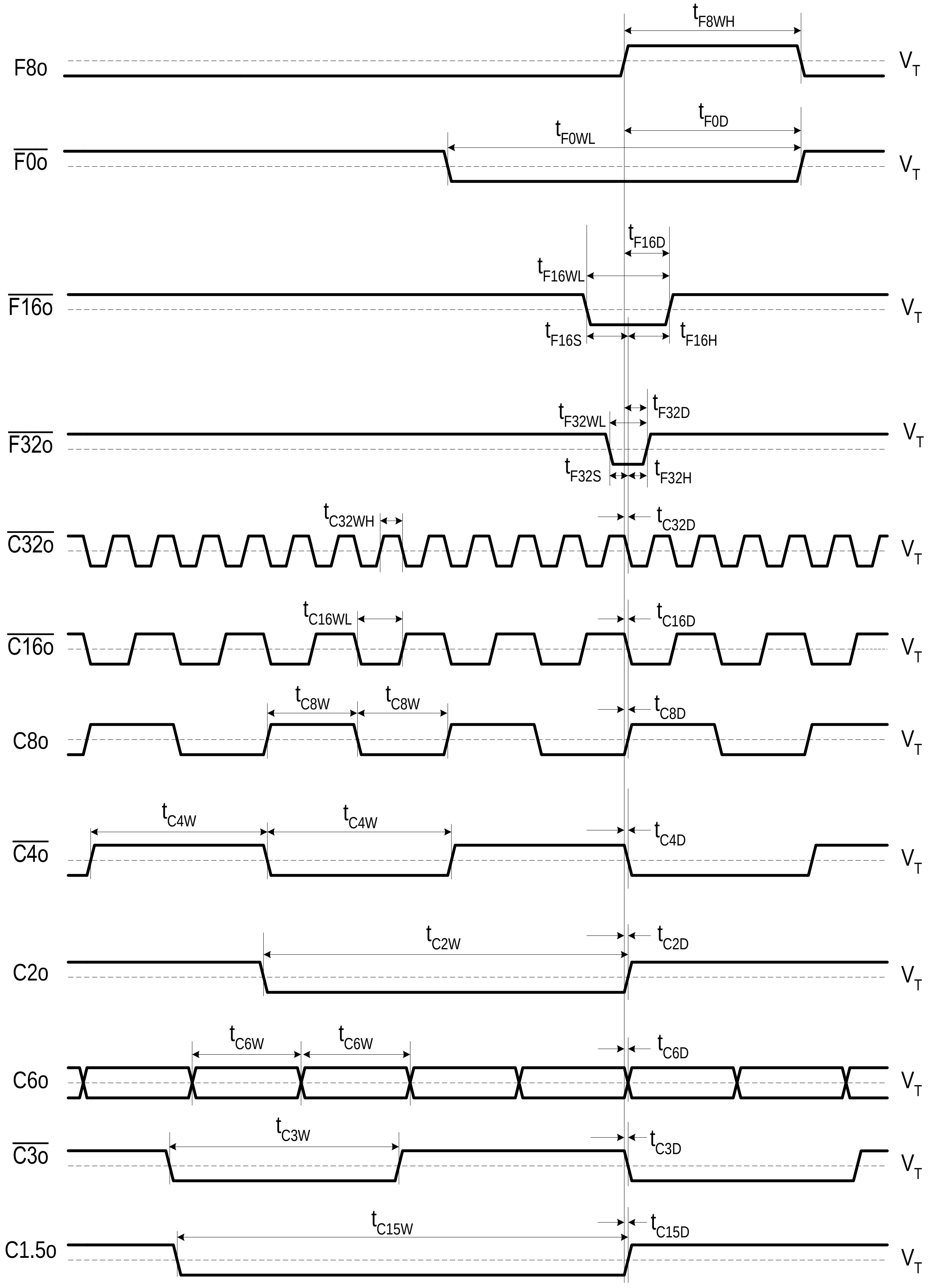


Figure - 13 Output Timing 1

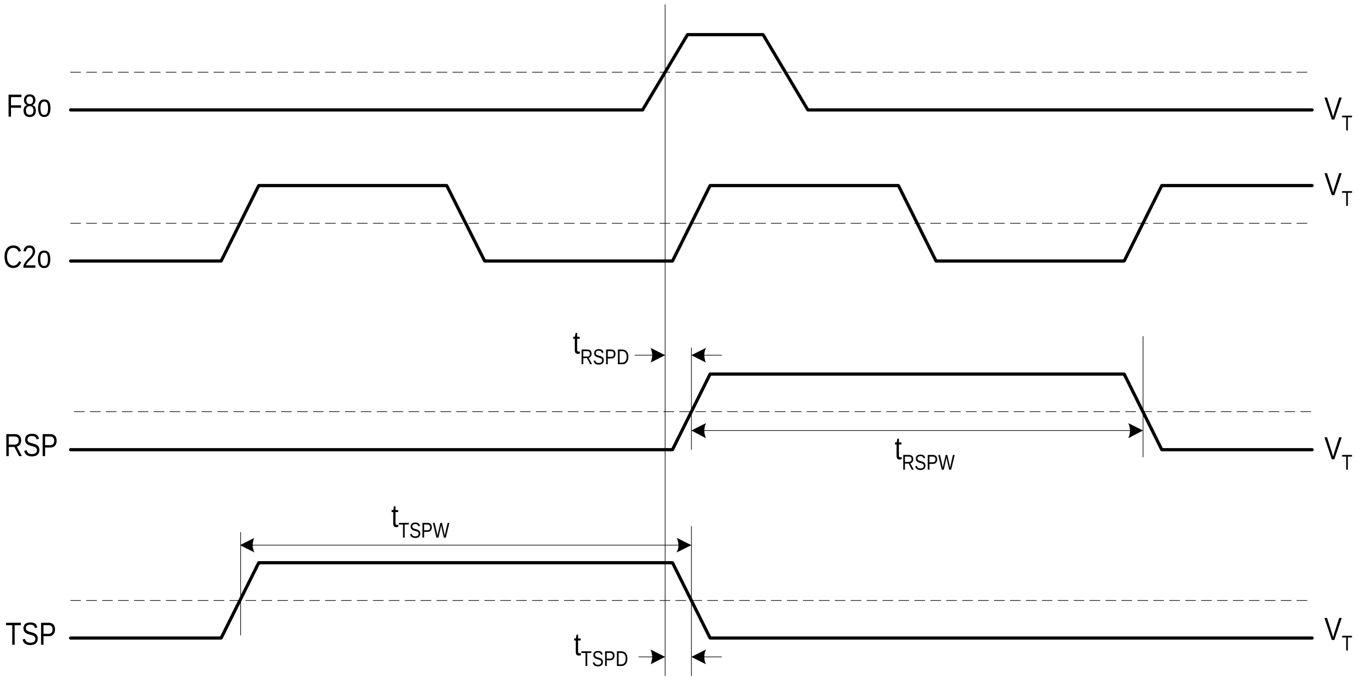


Figure - 14 Output Timing 2

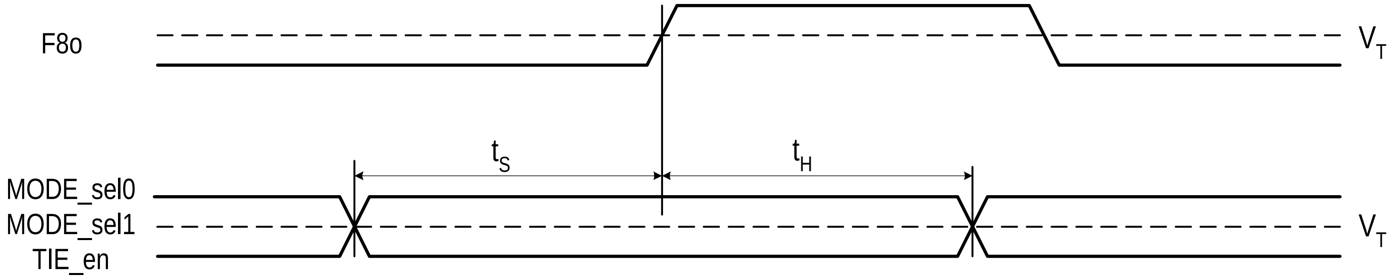
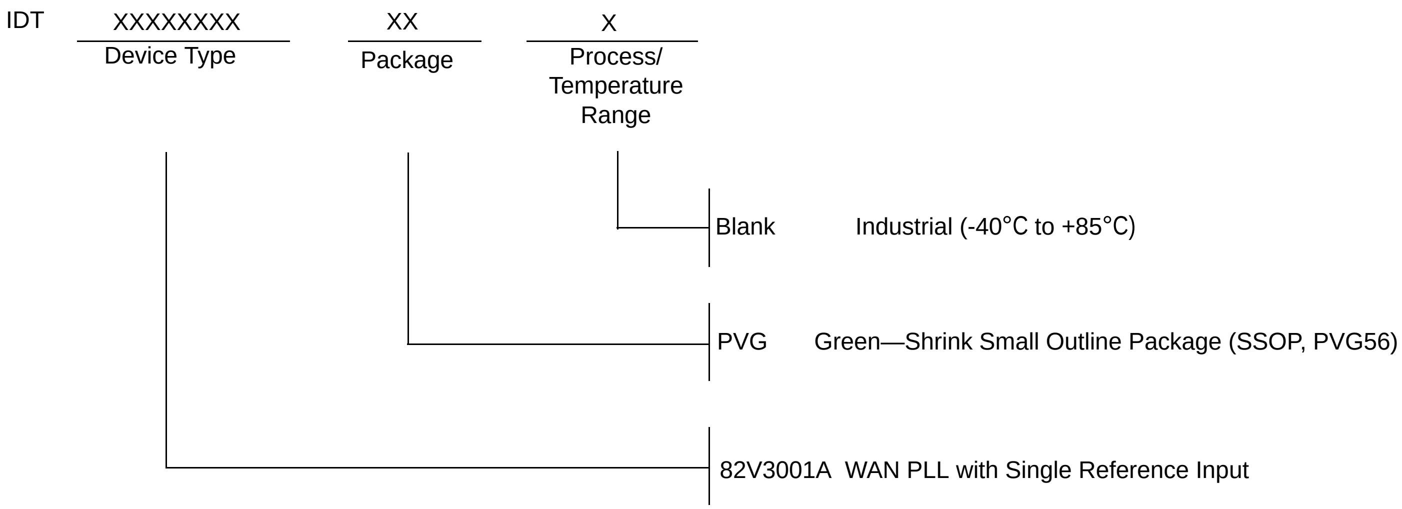


Figure - 15 Input Control Setup and Hold Timing

7 ORDERING INFORMATION



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