

74VHCT240AFT,74VHCT244AFT

1. Functional Description

- Octal Bus Buffer

74VHCT240AFT: INVERTED, 3-STATE OUTPUTS

74VHCT244AFT: NON-INVERTED, 3-STATE OUTPUTS

2. General

The 74VHCT240AFT and 74VHCT244AFT are advanced high speed CMOS OCTAL BUS BUFFERS fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The 74VHCT240AFT is an inverting 3-state buffer having two active-low output enables. The 74VHCT244AFT is a non-inverting 3-state buffer, and has two active-low output enables.

These devices are designed to be used with 3-state memory address drivers, etc.

The input voltage are compatible with TTL output voltage.

These devices may be used as a level converter for interfacing 3.3 V to 5 V system.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (Note) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

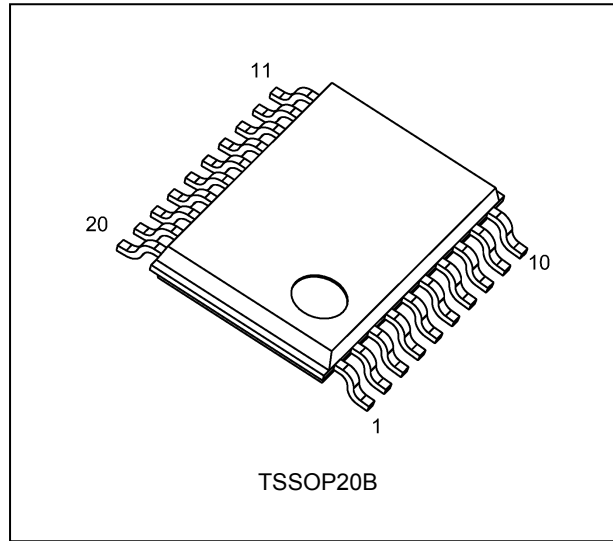
Note: Output in off-state

3. Features

- (1) AEC-Q100 (Rev. H) (Note 1)
- (2) Wide operating temperature range: $T_{opr} = -40$ to 125 °C
- (3) High speed: Propagation delay time = 6.1 ns (typ.) at $V_{CC} = 5.0$ V
- (4) Quiescent supply current: $I_{CC} = 4.0$ μ A (max) at $T_a = 25$ °C
- (5) Compatible with TTL input: $V_{IL} = 0.8$ V (max)
 $V_{IH} = 2.0$ V (min)
- (6) Power down protection is provided on all inputs and outputs.
- (7) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- (8) Low noise: $V_{OLP} = 1.0$ V (max)
- (9) Pin and function compatible with the 74 series
(ACT/HCT/AHCT etc.) 240/244 type.

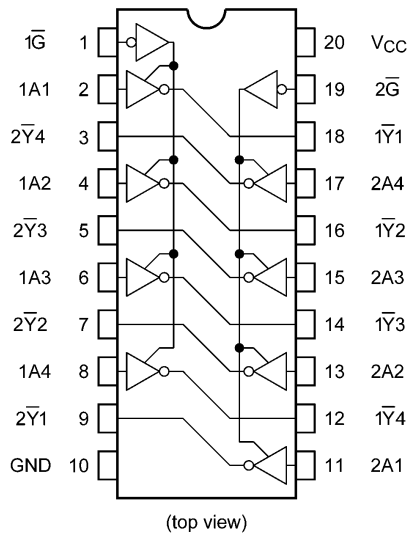
Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

4. Packaging

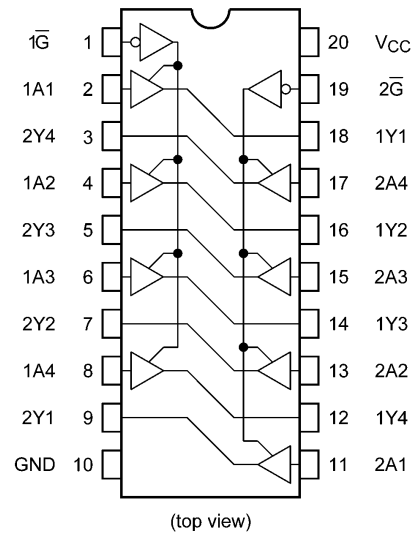


5. Pin Assignment

74VHCT240AFT

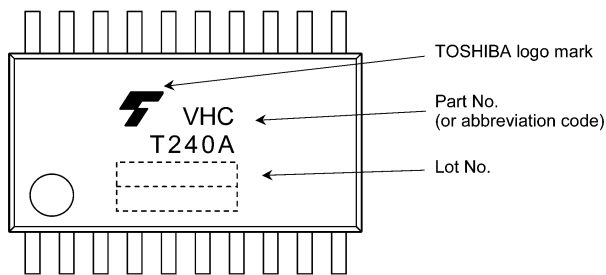


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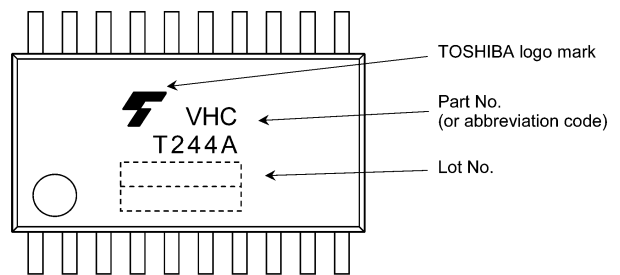


6. Marking

74VHCT240AFT

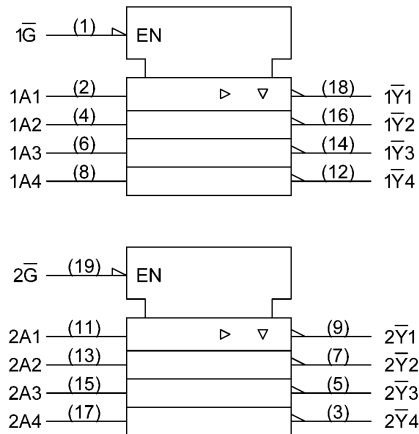


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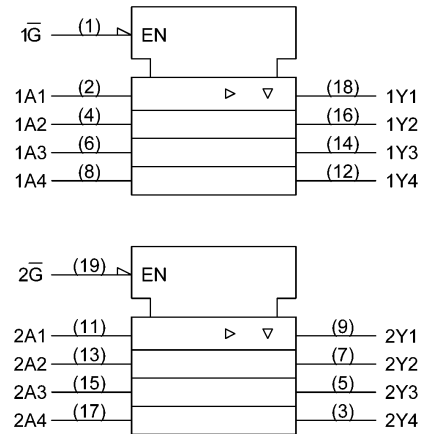


7. IEC Logic Symbol

74VHCT240AFT



74VHCT244AFT



8. Truth Table

Input \bar{G}	Input A_n	Output Y_n	Output \bar{Y}_n
L	L	L	H
L	H	H	L
H	X	Z	Z

- X: Don't care
- Z: High impedance
- Y_n : 74VHCT244AFT
- \bar{Y}_n : 74VHCT240AFT

9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to 7.0	V
Output voltage	V_{OUT}	(Note 1)	-0.5 to 7.0	V
		(Note 2)	-0.5 to $V_{CC} + 0.5$	
Input diode current	I_{IK}		-20	mA
Output diode current	I_{OK}	(Note 3)	± 20	mA
Output current	I_{OUT}		± 25	mA
V_{CC} /ground current	I_{CC}		± 75	mA
Power dissipation	P_D	(Note 4)	180	mW
Storage temperature	T_{stg}		-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Output in off-state.

Note 2: High (H) or Low (L) state. I_{OUT} absolute maximum rating must be observed.

Note 3: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Note 4: 180 mW in the range of $T_a = -40$ to $85^{\circ}C$. From $T_a = 85$ to $125^{\circ}C$ a derating factor of -3.25 mW/ $^{\circ}C$ shall be applied until 50 mW.

10. Operating Ranges (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		4.5 to 5.5	V
Input voltage	V_{IN}		0 to 5.5	V
Output voltage	V_{OUT}	(Note 1)	0 to 5.5	V
		(Note 2)	0 to V_{CC}	
Operating temperature	T_{opr}		-40 to 125	$^{\circ}C$
Input rise and fall times	dt/dv		0 to 20	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either V_{CC} or GND.

Note 1: Output in OFF state.

Note 2: High (H) or Low (L) state.

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit	
High-level input voltage	V_{IH}	—	4.5 to 5.5	2.0	—	—	V	
Low-level input voltage	V_{IL}	—	4.5 to 5.5	—	—	0.8	V	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	4.5	4.4	4.5	—	V
			$I_{OH} = -8\text{ mA}$	4.5	3.94	—	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	4.5	—	0.0	0.1	V
			$I_{OL} = 8\text{ mA}$	4.5	—	—	0.36	
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	—	—	± 0.25	μA	
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	—	± 0.1	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	μA	
	I_{CCT}	Per input : $V_{IN} = 3.4\text{ V}$ Other input: V_{CC} or GND	5.5	—	—	1.35	mA	
Output leakage current (Power-OFF)	I_{OPD}	$V_{OUT} = 5.5\text{ V}$	0	—	—	0.5	μA	

11.2. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $85\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit	
High-level input voltage	V_{IH}	—	4.5 to 5.5	2.0	—	V	
Low-level input voltage	V_{IL}	—	4.5 to 5.5	—	0.8	V	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	4.5	4.4	—	V
			$I_{OH} = -8\text{ mA}$	4.5	3.80	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	4.5	—	0.1	V
			$I_{OL} = 8\text{ mA}$	4.5	—	0.44	
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	—	± 2.50	μA	
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	± 1.0	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	40.0	μA	
Quiescent supply current	I_{CCT}	Per input: $V_{IN} = 3.4\text{ V}$ Other input: V_{CC} or GND	5.5	—	1.50	mA	
Output leakage current (Power-OFF)	I_{OPD}	$V_{OUT} = 5.5\text{ V}$	0	—	5.0	μA	

11.3. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $125\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit	
High-level input voltage	V_{IH}	—	4.5 to 5.5	2.0	—	V	
Low-level input voltage	V_{IL}	—	4.5 to 5.5	—	0.8	V	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	4.5	4.4	—	V
			$I_{OH} = -8\text{ mA}$	4.5	3.70	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	4.5	—	0.1	V
			$I_{OL} = 8\text{ mA}$	4.5	—	0.55	
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	—	± 10.0	μA	
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	± 2.0	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	80.0	μA	
Quiescent supply current	I_{CCT}	Per input: $V_{IN} = 3.4\text{ V}$ Other input: V_{CC} or GND	5.5	—	1.50	mA	
Output leakage current (Power-OFF)	I_{OPD}	$V_{OUT} = 5.5\text{ V}$	0	—	20.0	μA	

11.4. AC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Part Number	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Propagation delay time	74VHCT240AFT	t_{PLH}, t_{PHL}		—	5.0 ± 0.5	15	—	5.6	7.8	ns
						50	—	6.1	8.8	
	74VHCT244AFT	t_{PLH}, t_{PHL}		—	5.0 ± 0.5	15	—	5.4	7.4	ns
						50	—	5.9	8.4	
3-state output enable time		t_{PZL}, t_{PZH}		$R_L = 1\text{ k}\Omega$	5.0 ± 0.5	15	—	7.7	10.4	ns
						50	—	8.2	11.4	
3-state output disable time		t_{PLZ}, t_{PHZ}		$R_L = 1\text{ k}\Omega$	5.0 ± 0.5	50	—	8.8	11.4	ns
Output skew		$t_{oS LH}, t_{oS HL}$	(Note 1)	—	5.0 ± 0.5	50	—	—	1.0	ns
Input capacitance		C_{IN}		—			—	4	10	pF
Output capacitance		C_{OUT}		—			—	9	—	pF
Power dissipation capacitance	74VHCT240AFT	C_{PD}	(Note 2)	—			—	19	—	pF
	74VHCT244AFT	C_{PD}	(Note 2)	—			—	18	—	

Note 1: Parameter guaranteed by design. ($t_{oS LH} = |t_{PLHm} - t_{PLHn}|$, $t_{oS HL} = |t_{PHLm} - t_{PHLn}|$)

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8 \text{ (per bit)}$$

11.5. AC Characteristics (Unless otherwise specified, $T_a = -40\text{ to }85\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Part Number	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time	74VHCT240AFT	t_{PLH}, t_{PHL}		—	5.0 ± 0.5	15	1.0	9.0	ns
						50	1.0	10.0	
	74VHCT244AFT	t_{PLH}, t_{PHL}		—	5.0 ± 0.5	15	1.0	8.5	ns
						50	1.0	9.5	
3-state output enable time		t_{PZL}, t_{PZH}		$R_L = 1\text{ k}\Omega$	5.0 ± 0.5	15	1.0	12.0	ns
						50	1.0	13.0	
3-state output disable time		t_{PLZ}, t_{PHZ}		$R_L = 1\text{ k}\Omega$	5.0 ± 0.5	50	1.0	13.0	ns
Output skew		$t_{oS LH}, t_{oS HL}$	(Note 1)	—	5.0 ± 0.5	50	—	1.0	ns
Input capacitance		C_{IN}		—			—	10	pF

Note 1: Parameter guaranteed by design. ($t_{oS LH} = |t_{PLHm} - t_{PLHn}|$, $t_{oS HL} = |t_{PHLm} - t_{PHLn}|$)

11.6. AC Characteristics (Unless otherwise specified, $T_a = -40\text{ to }125\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Part Number	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time	74VHCT240AFT	t_{PLH}, t_{PHL}		—	5.0 ± 0.5	15	1.0	10.0	ns
						50	1.0	11.0	
Propagation delay time	74VHCT244AFT	t_{PLH}, t_{PHL}		—	5.0 ± 0.5	15	1.0	9.5	ns
						50	1.0	10.5	
3-state output enable time		t_{PZL}, t_{PZH}		$R_L = 1\text{ k}\Omega$	5.0 ± 0.5	15	1.0	13.0	ns
						50	1.0	14.5	
3-state output disable time		t_{PLZ}, t_{PHZ}		$R_L = 1\text{ k}\Omega$	5.0 ± 0.5	50	1.0	14.5	ns
Output skew		$t_{oS LH}, t_{oS HL}$	(Note 1)	—	5.0 ± 0.5	50	—	1.0	ns
Input capacitance		C_{IN}		—			—	10	pF

Note 1: Parameter guaranteed by design. ($t_{oS LH} = |t_{PLHm} - t_{PLHn}|$, $t_{oS HL} = |t_{PHLm} - t_{PHLn}|$)

11.7. Noise Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Limit	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	$C_L = 50\text{ pF}$	5.0	0.8	1.0	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	$C_L = 50\text{ pF}$	5.0	-0.8	-1.0	
Minimum high-level dynamic input voltage	V_{IHD}	$C_L = 50\text{ pF}$	5.0	—	2.0	
Maximum low-level dynamic input voltage	V_{ILD}	$C_L = 50\text{ pF}$	5.0	—	0.8	

Package Dimensions

Unit: mm



Weight: 0.071 g (typ.)

Package Name(s)
Nickname: TSSOP20B

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