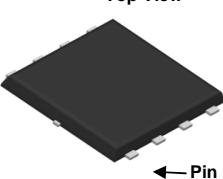
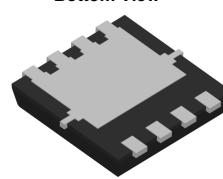
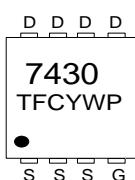
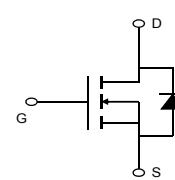


<p>30V N-Channel MOSFET</p> <p>PRODUCT SUMMARY</p> <p> V_{DS} (V) = 30V I_D = 34A (V_{GS} = 10V) $R_{DS(ON)}$ < 8.5mΩ (V_{GS} = 10V) $R_{DS(ON)}$ < 15mΩ (V_{GS} = 4.5V) </p> <p>100% UIS Tested 100% R_g Tested</p> <ul style="list-style-type: none"> • Trench Power αMOS Technology • Low $R_{DS(ON)}$ • Low Gate Charge • High Current Capability • RoHS and Halogen-Free Compliant <p>Applications</p> <ul style="list-style-type: none"> • DC/DC Converters in Computing • Isolated DC/DC Converters in Telecom and Industrial 	<p>DFN 3x3_EP</p> <p>Top View</p>  <p>Bottom View</p> 
	<p>Top View</p>  <p>Equivalent Circuit</p> 

Y :year code W :week code

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
7430	7430	PDFN3x3-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted				
Parameter	Symbol	Maximum	Units	
Drain-Source Voltage	V_{DS}	30	V	
Gate-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current ^A	I_D	34	A	
Pulsed Drain Current ^C	I_{DM}	80		
Continuous Drain Current ^A	I_{DSM}	13	A	
Avalanche Current ^C	I_{AR}	22		
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	24	mJ	
Power Dissipation ^B	P_D	23		
Power Dissipation ^A	P_{DSM}	3.1	W	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10\text{s}$	$R_{\theta JA}$	30	°C/W
Maximum Junction-to-Ambient ^A	Steady-State		60	°C/W
Maximum Junction-to-Case ^B	Steady-State	$R_{\theta JC}$	4.5	°C/W
			5.4	



SHENZHEN TUOFENG SEMICONDUCTOR TECHNOLOGY CO.,LTD

N-Channel Enhancement Mode Power MOSFET

7430

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$			1	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			100	nA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.5	1.9	2.5	V
$I_{\text{D(ON)}}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	80			A
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=20\text{A}$		6.5	8.5	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=20\text{A}$		13	15	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=20\text{A}$		45		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				25	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$	610	760	910	pF
C_{oss}	Output Capacitance		88	125	160	pF
C_{rss}	Reverse Transfer Capacitance		40	70	100	pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$	0.8	1.6	2.4	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, I_D=20\text{A}$	11	14	17	nC
$Q_g(4.5\text{V})$	Total Gate Charge		5	6.6	8	nC
Q_{gs}	Gate Source Charge		1.9	2.4	2.9	nC
Q_{gd}	Gate Drain Charge		1.8	3	4.2	nC
$t_{\text{D(on)}}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, R_L=0.75\Omega, R_{\text{GEN}}=3\Omega$		4.4		ns
t_r	Turn-On Rise Time			9		ns
$t_{\text{D(off)}}$	Turn-Off DelayTime			17		ns
t_f	Turn-Off Fall Time			6		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}, dI/dt=500\text{A}/\mu\text{s}$	5.6	7	8	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}, dI/dt=500\text{A}/\mu\text{s}$	6.4	8	9.6	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ $t \leq 10\text{s}$ value and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(\text{MAX})}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(\text{MAX})}=150^\circ\text{C}$.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

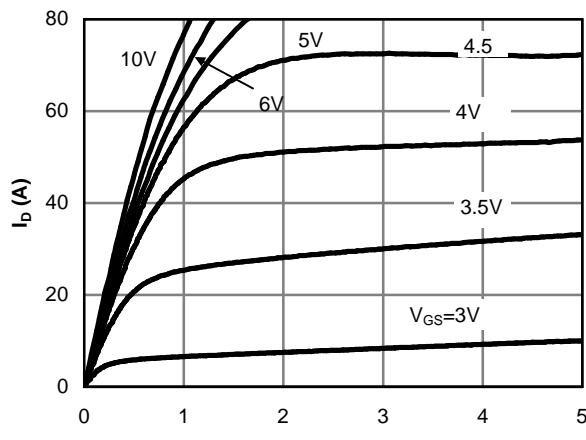


Fig 1: On-Region Characteristics

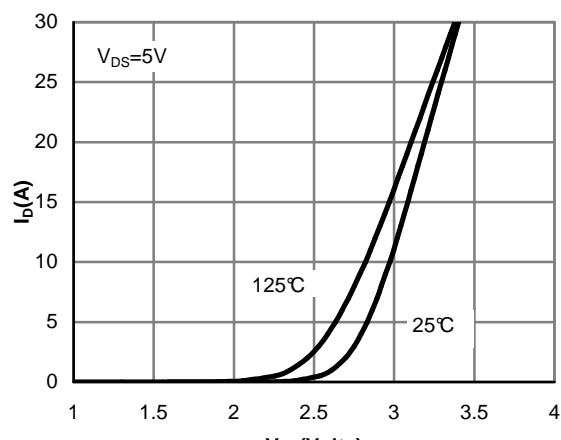


Figure 2: Transfer Characteristics

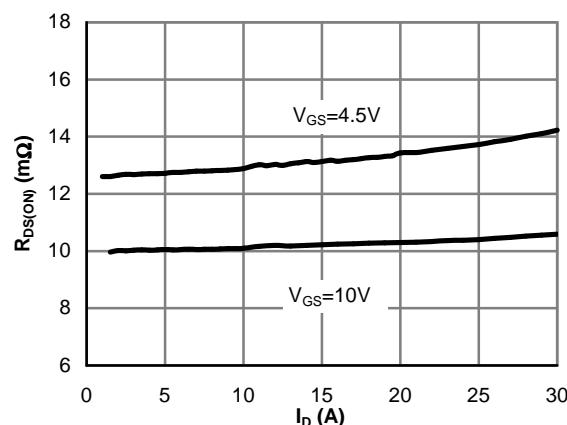


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

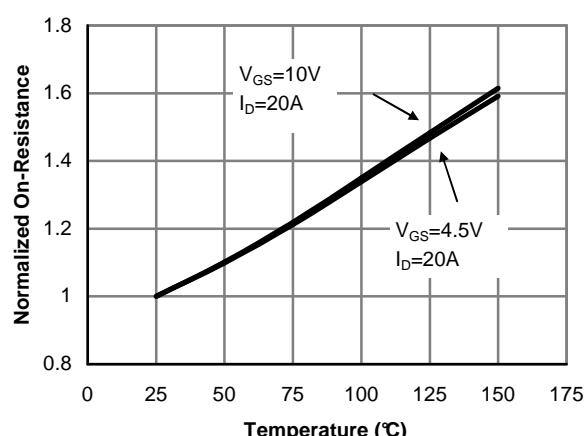


Figure 4: On-Resistance vs. Junction Temperature

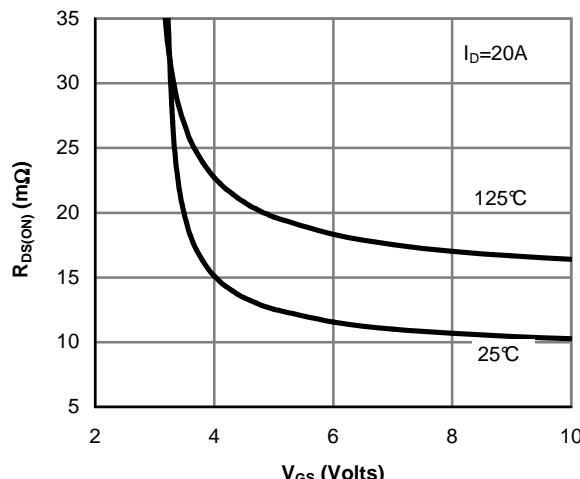


Figure 5: On-Resistance vs. Gate-Source Voltage

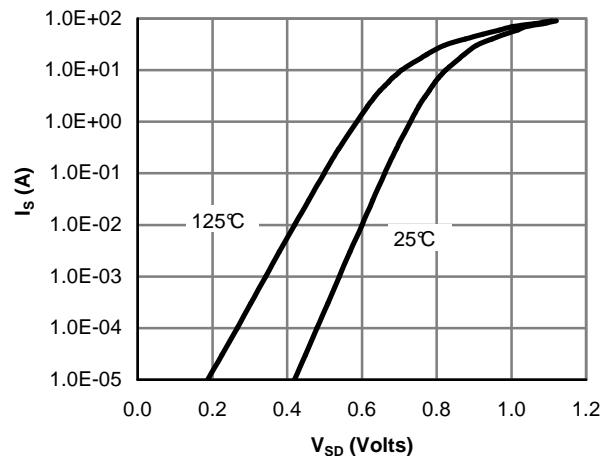


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

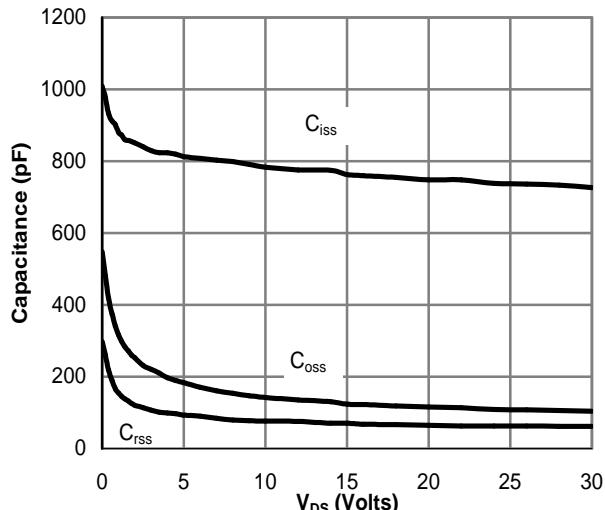
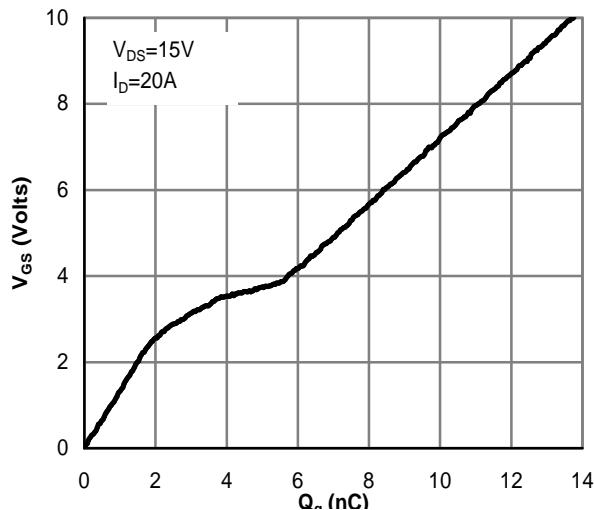


Figure 8: Capacitance Characteristics

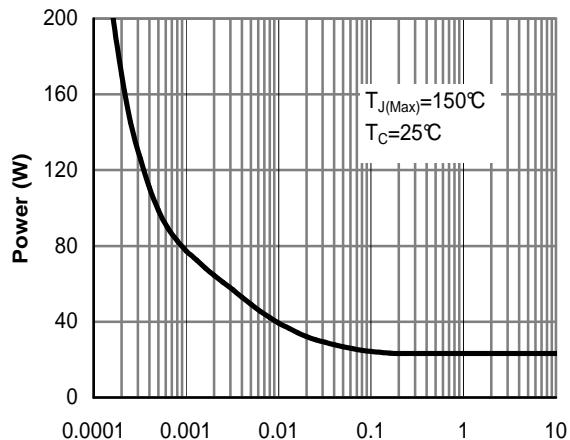
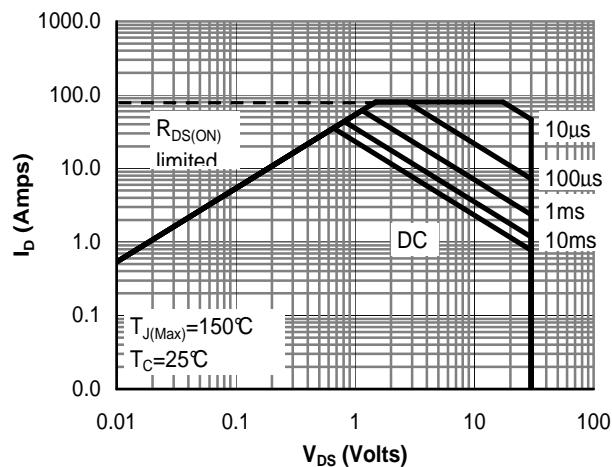


Figure 9: Maximum Forward Biased
Safe Operating Area (Note F)

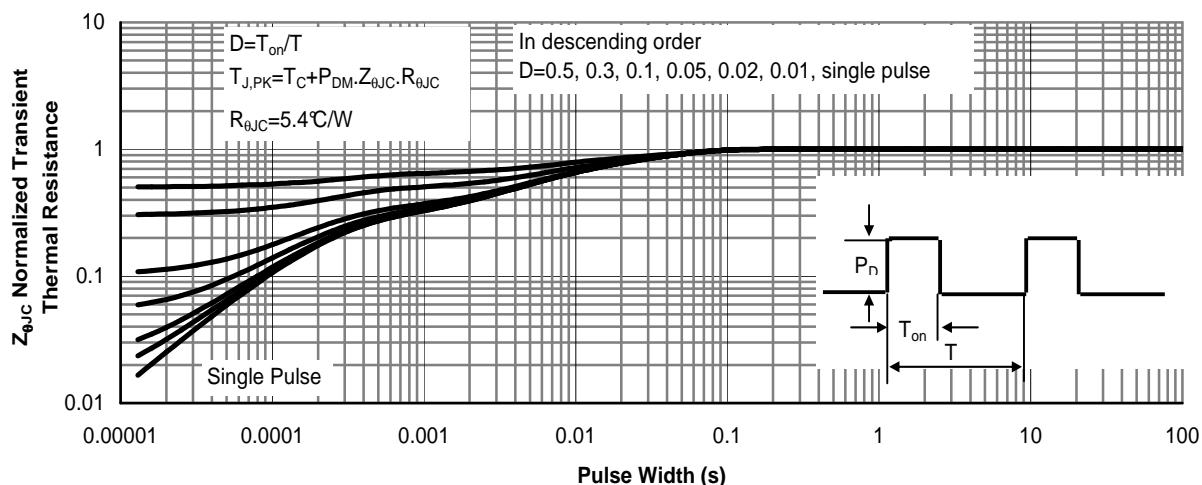


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

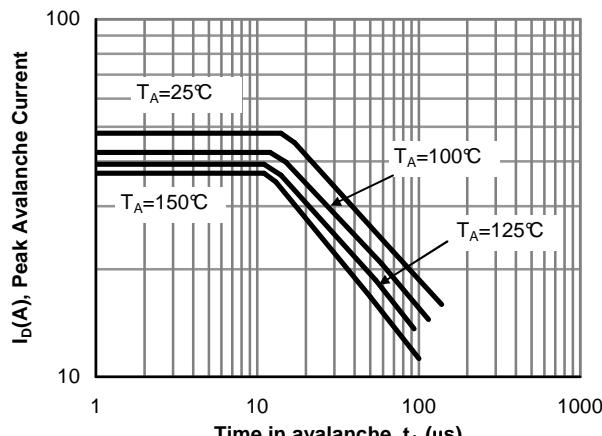


Figure 12: Single Pulse Avalanche capability
(Note C)

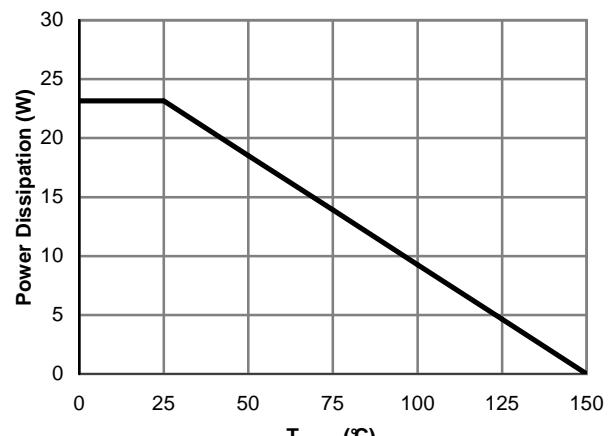


Figure 13: Power De-rating (Note F)

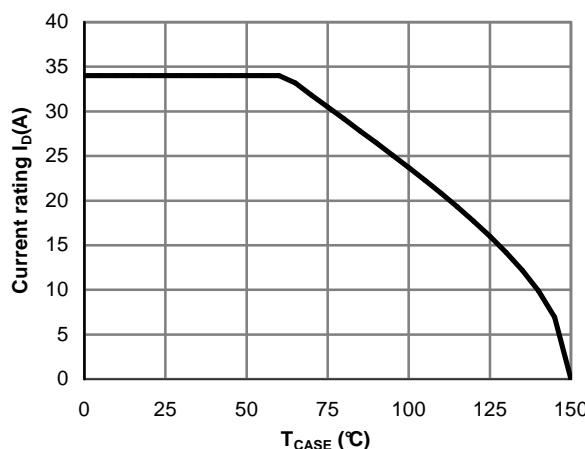


Figure 14: Current De-rating (Note F)

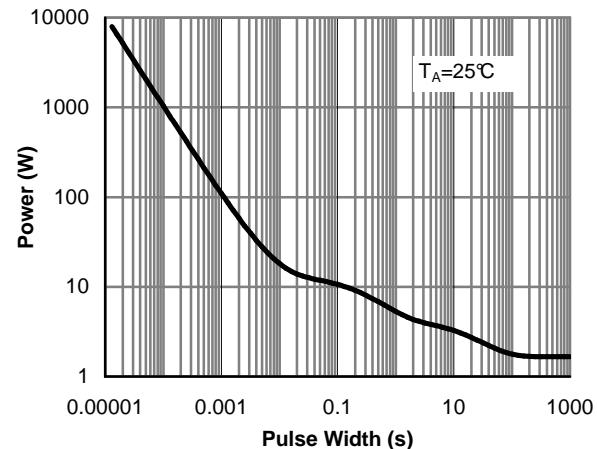


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

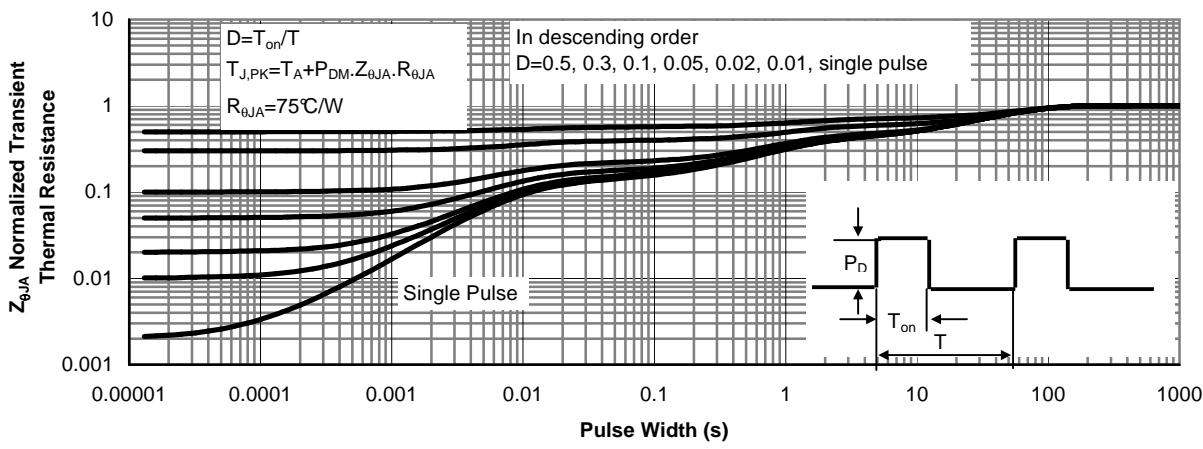
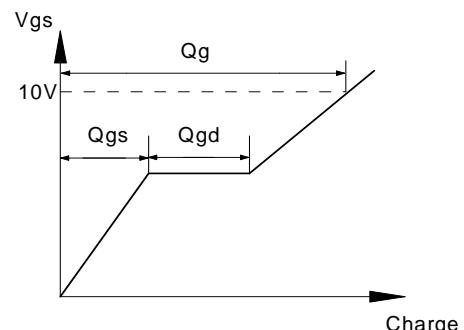
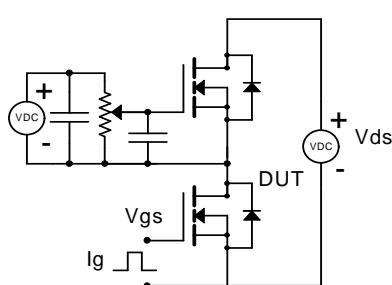
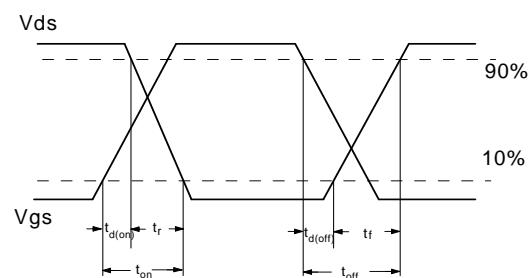
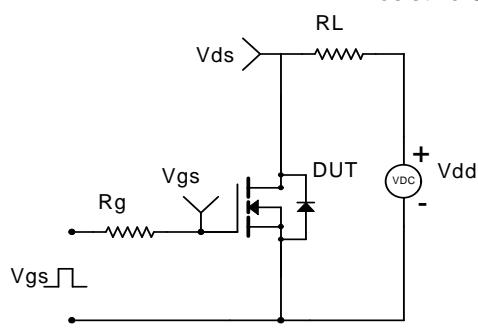


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

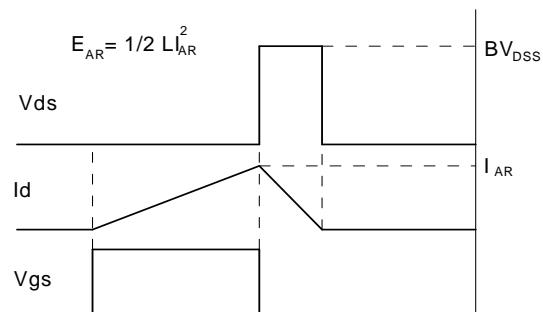
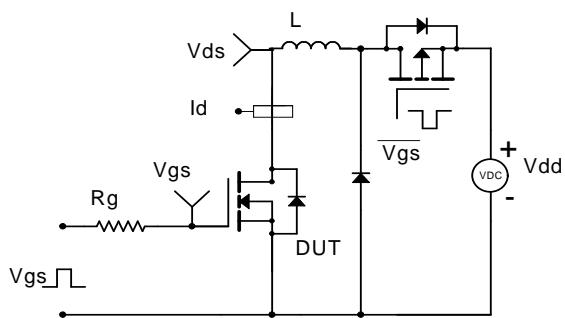
Gate Charge Test Circuit & Waveform



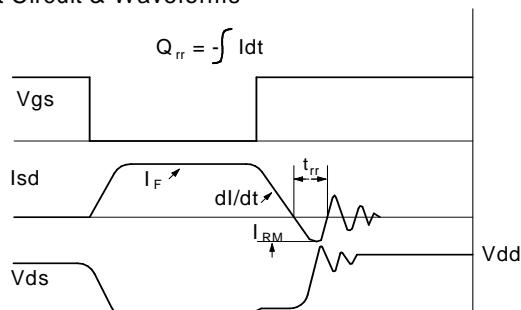
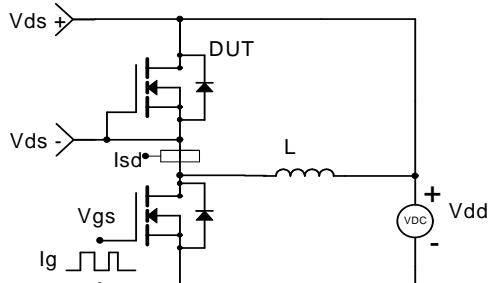
Resistive Switching Test Circuit & Waveforms



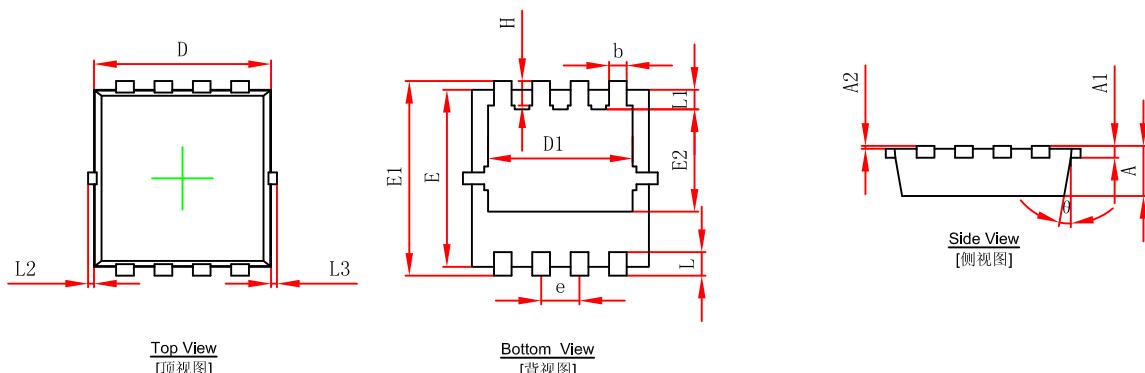
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

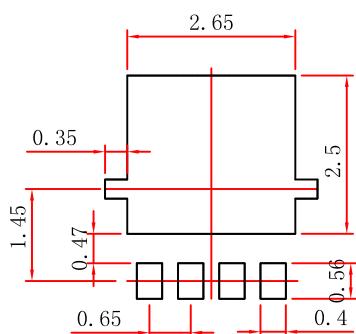


PDFNWB3.3x3.3-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

PDFNWB3.3x3.3-8L Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.