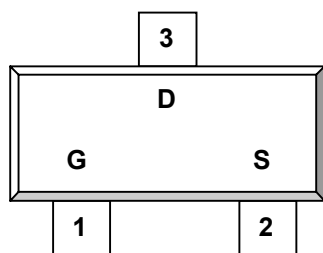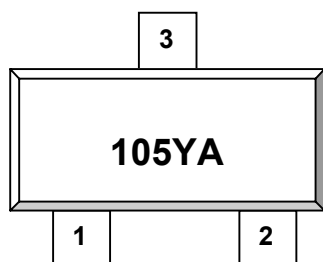## DESCRIPTION

ST1005SRG is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.
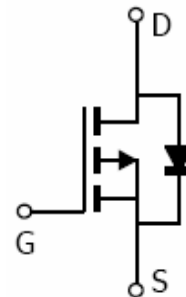
PIN CONFIGURATION
SOT-23

1.Gate   2.Source   3.Drain

PART MARKING
SOT-23

105YA

Y: Year Code   A: Process Code

FEATURE

- -100V/-0.8.0A, $R_{DS(ON)}$ = 650m-ohm (Typ.)
  @VGS = -10V
- -60V/-0.4A, $R_{DS(ON)}$ = 700m-ohm
  @VGS = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain CurrentTJ=150℃）	TA=25℃ TA=70℃	I_D	-0.8 -0.4	A
Pulsed Drain Current		I_{DM}	-4	A
Continuous Source Current (Diode Conduction)		I_S	-1.0	A
Power Dissipation	TA=25℃ TA=70℃	P_D	1.25 0.8	W
Operation Junction Temperature		T_J	150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	85	℃/W

ST1005SRG

P Channel Enhancement Mode MOSFET

-0.8A

ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-10uA	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=VGS,I_D=-250uA	-1.0		-2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-80V,V_{GS}=0V			-1	uA
		V_{DS}=-80V,V_{GS}=0V T_J=55℃			-5	
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-0.8A V_{GS}=-4.5V,I_D=-0.4A		0.640 0.690	0.650 0.700	Ω
Forward Transconductance	g_{fs}	V_{DS}=-5,I_D=-0.8		2.0		S
Diode Forward Voltage	V_{SD}	I_S=-1.0A,V_{GS}=0V			-0.8	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-50V V_{GS}=-10V $I_D≡$-0.5A		16		nC
Gate-Source Charge	Q_{gs}			9		
Gate-Drain Charge	Q_{gd}			1.23		
Input Capacitance	C_{iss}	V_{DS}=-15V V_{GS}=0V F=1MHz			600	pF
Output Capacitance	C_{oss}			550		
Reverse Transfer Capacitance	C_{rss}			20		
Turn-On Time	$t_{d(on)}$ tr	V_{DD}=-50V I_D=-0.5A V_{GS}=-10V R_G=2.5Ω		2		nS
				19		
Turn-Off Time	$t_{d(off)}$ tf			18.5		
				20		

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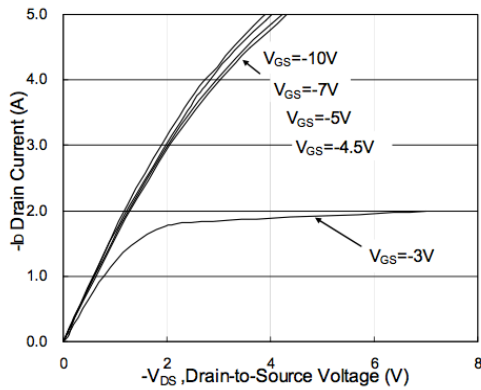
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TYPICAL CHARACTERISTICS

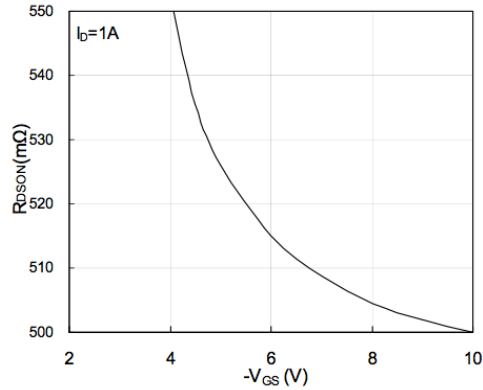**Fig.1 Typical Output Characteristics**
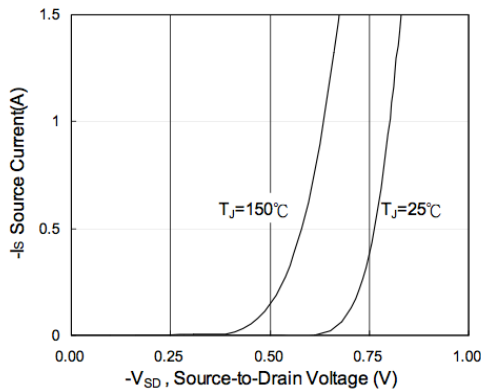

Fig.2 On-Resistance vs. Gate-Source
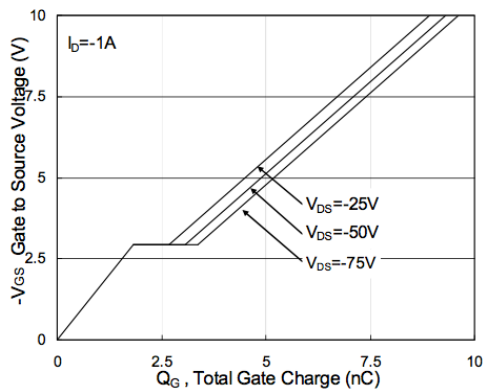

Fig.3 Forward Characteristics Of Reverse

Fig.4 Gate-Charge Characteristics

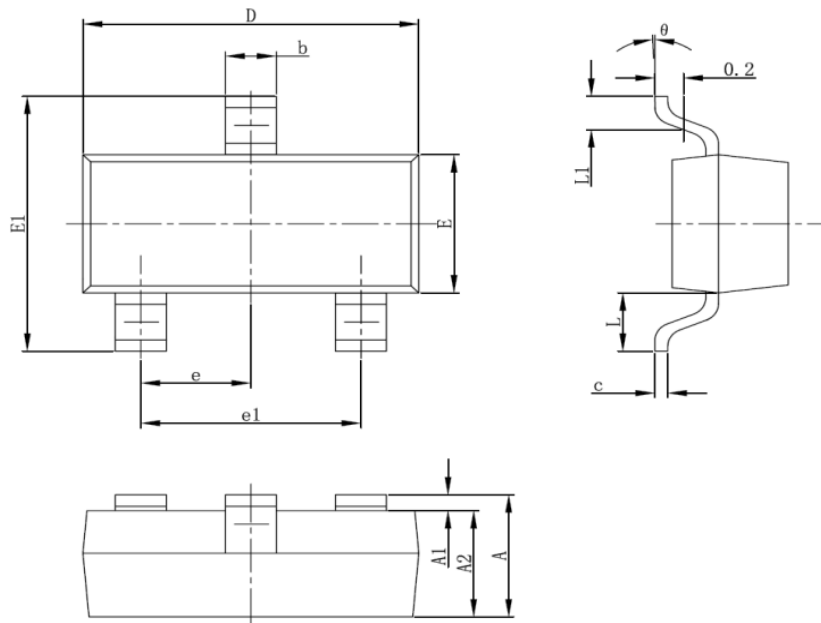**Fig.5 Normalized $V_{GS(th)}$ vs. T_J**

Fig.6 Normalized R_{DSON} vs. T_J

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120 Bentley Square, Mountain View, Ca 94040 USA
www.stansontech.com

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SOT-23 PACKAGE OUTLINE

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

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