HCNW4502/3 HCPL-0452/0453/4502/4503 Single Channel, High Speed Optocouplers



Data Sheet



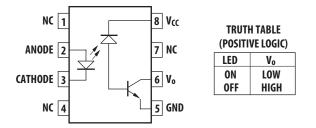
Description

These diode-transistor optocouplers use an insulating layer between a LED and an integrated photodetector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output-transistor collector increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

These single channel optocouplers are available in 8-Pin DIP, SO-8 and Widebody package configurations.

The HCPL-4502/4503 and HCNW4502/4503 are designed for high speed TTL/TTL applications. A standard 16 mATTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 k Ω pull-up resistor. CTR for these devices is 19% minimum at I_e = 16 mA.

Functional Diagram



A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

Features

- 15 kV/ μ s minimum common mode transient immunity at V_{CM} = 1500 V
- High speed: 1 Mb/s
- TTL compatible
- Available in 8-Pin DIP, SO-8, widebody packages
- Open collector output
- Guaranteed performance from temperature: 0°C to 70°C
- Safety approval UL Recognized – 3750 V_{rms} for 1 minute (5000 V_{rms} for 1 minute for HCNW and Option 020 devices) per UL1577 CSA Approved IEC/EN/DIN EN 60747-5-5 Approved
 - $-V_{IORM} = 630 \text{ V peak for HCPL-4503#060}$
 - $-V_{IORM} = 1414 \text{ V} \text{ peak for HCNW devices}$
- Dual channel version available (4534/0534)
- MIL-PRF-38534 hermetic version available (55XX/65XX/4N55)

Applications

- High voltage insulation
- Video signal isolation
- Power transistor isolation in motor drives
- Line receivers
- Feedback element in switched mode power supplies
- High speed logic ground isolation – TTL/TTL, TTL/CMOS, TTL/LSTTL
- Replaces pulse transformers
- Replaces slow phototransistor isolators
- Analog signal ground isolation

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.