ZD53D16GA062FA

16Gb -3200

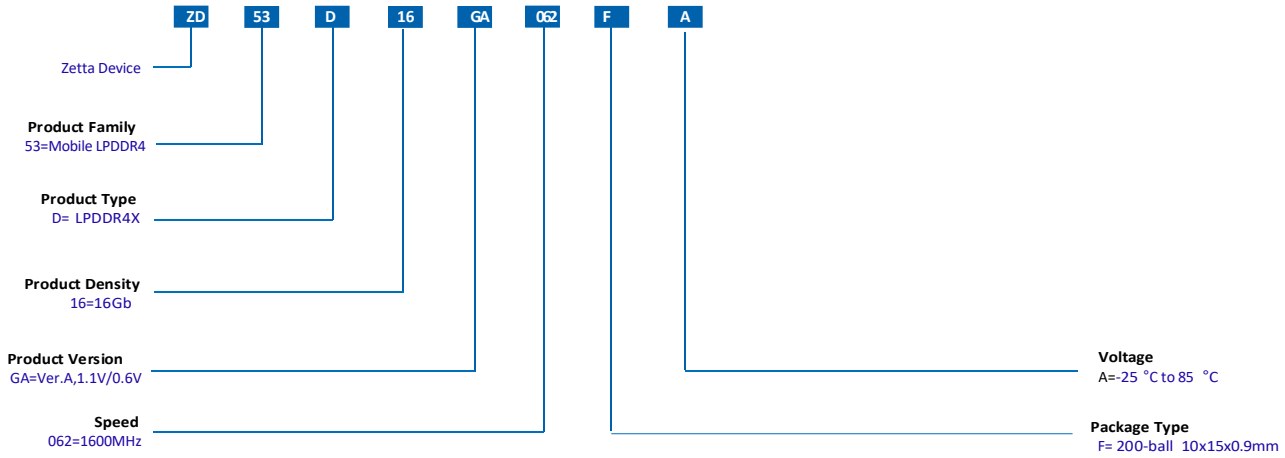
LPDDR4X SDRAM Datasheet

1. Core Specifications

1.1 *Ordering* Part *Number*

Table 1-1 LPDDR4X Device Ordering Information

Part Number	Density	Organization	Data Rate	Package
ZD53D16GA062FA	16Gb	2CH x32	-062 / 3200 Mbps	200-Ball (10mmx15mm)



1.2 Address Table

Table 1-2 Die Addressing Table

Die Configuration	512Mb x16
Bank Address	BA0~BA2
Row Address	A0~A15
Column Address	A0~A9

2. Physical Specifications

2.1 200-Ball x32 Discrete Package Dimension

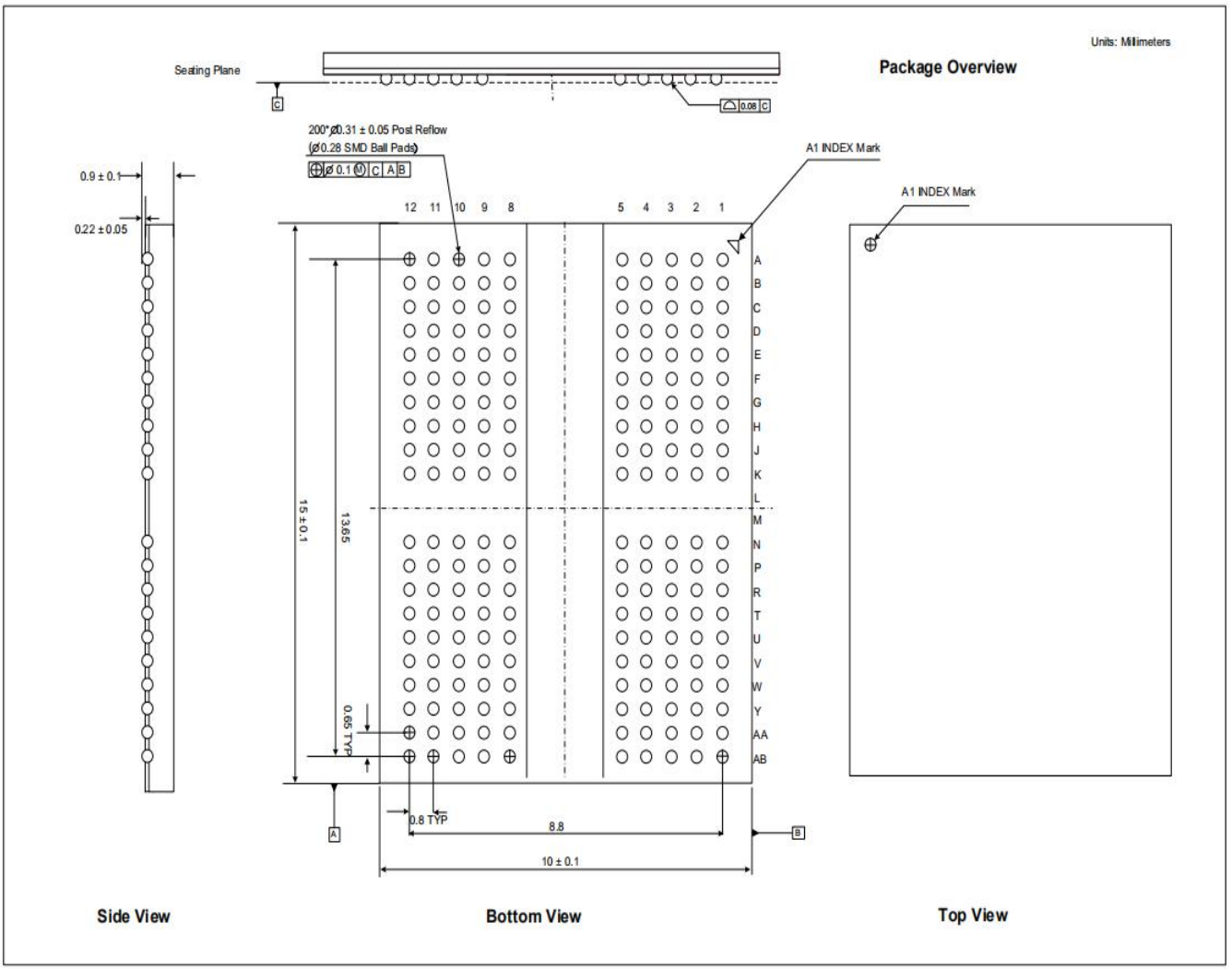


Figure 2-1 200-Ball x32 Discrete FBGA Package Dimension

2.2 x32 Discrete Package Ballout

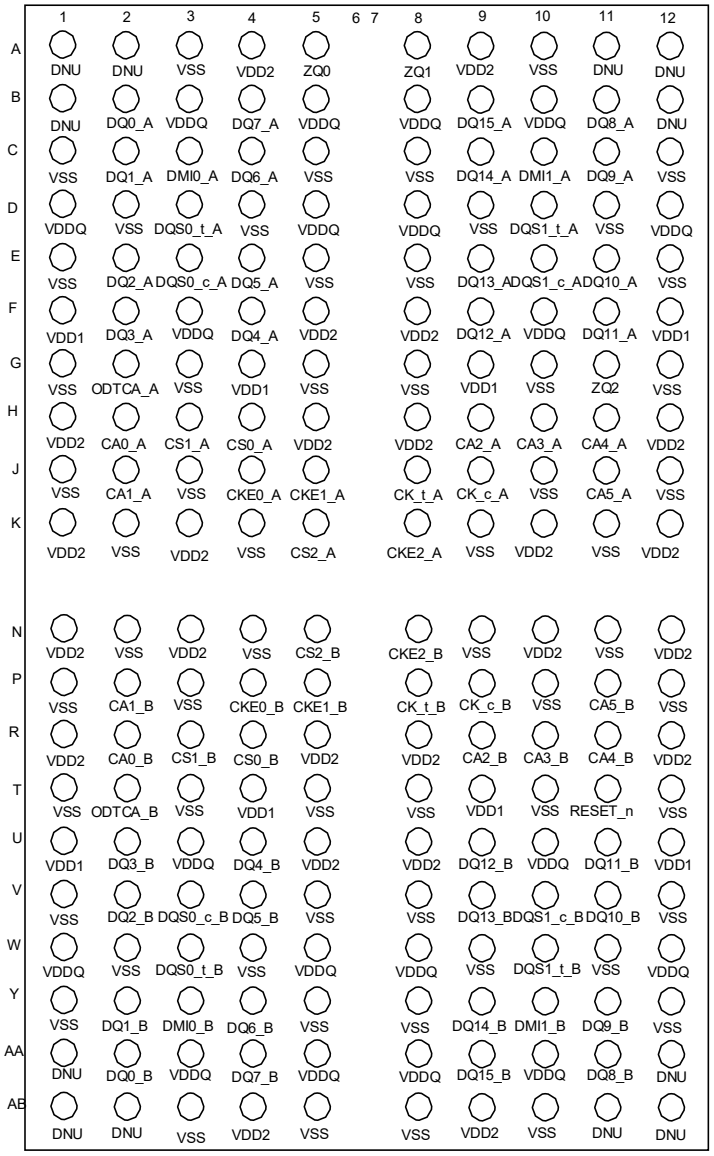


Figure 2-2 x32 Discrete Package Ballout

Note:

1 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows using MO-311 0.80mm Pitch

2 Top View, A1 in top left corner. CS1_A/B, CE1_A/B, ZQ1 is floating for 2GB package.

3 ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.

4 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3-rank package. For 1-rank and 2-rank package those balls are NC.

5 Die pad VSS and VSSQ signals are combined to VSS package balls.

6 Package requires dual channel die or functional equivalent of single channel die-stack.

2.3 Pad Definition

"_A" and "_B" indicate DRAM channels. "_A" pads are present in all devices while "_B" pads are present in dual channel SDRAM devices only.

LPDDR4X pad definitions are the same as LPDDR4, except ODT_CA pins as described in Table 2-1.

Table 2-3 Pad Definition

Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.
CKE_A, CKE_B	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS_A, CS_B	Input	**Chip Select:** CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A, CA[5:0]_B	Input	**Command/Address Inputs:** CA signals provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals.
DQ[15:0]_A, DQ[15:0]_B	I/O	**Data Input/Output:** Bi-direction data bus.
DQS[1:0]_t_A,DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	**Data Strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	**Data Mask Inversion:** DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.

Symbol	Type	Description
ZQ	Reference	**Calibration Reference:** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ± 1% resistor.
VDDQ,VDD1,VDD2	Supply	**Power Supplies:** Isolated on the die for improved noise immunity.
VSS, VSSQ	GND	**Ground Reference:** Power supply ground reference
RESET_n	Input	**RESET:** When asserted LOW, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die.
ODT_CA_A ,ODT_CA_B	Input	**CA ODT Control:** **LPDDR4:** The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins. **LPDDR4X:**The ODT_CA pin is ignored by LPDDR4X devices. ODT_CS/CA/CK Function is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to either VDD2 or Vss.

3. Absolute Maximum DC Ratings

Table 3-1 Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit
VDD1 supply voltage relative to VSS[1]	VDD1	-0.4	2.1	V
VDD2 supply voltage relative to VSS[1]	VDD2	-0.4	1.5	
VDDQ supply voltage relative to VSSQ[1]	VDDQ			
Voltage on any ball except VDD1 relative to VSS	V_{IN}, V_{OUT}			
Storage Temperature[2]	T_{STG}	-55	125	°C

Note:

1 See “Power-Ramp” for relationships between power supplies.

2 Storage temperature is the case surface temperature on the center/top side of the LPDDR4X device. For the measurement conditions, please refer to JESD51-2.

4. AC and DC Operating Conditions

4.1 Recommended DC Operating Conditions for Low Voltage

Table 4-1(a) LPDDR4 Recommended DC Operating Conditions

DRAM	Symbol	Min	Typ	Max	Unit	Note
Core 1 Power	VDD1	1.7	1.8	1.95	V	1,2
Core 1 Power/Input Buffer Power	VDD2	1.06	1.1	1.17	V	1,2,3
I/O Buffer Power	VDDQ	1.06	1.1	1.17	V	2,3

Note:

1 VDD1 uses significantly less current than VDD2.

2 The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.

3 VdIVW and TdIVW limits described elsewhere in this document apply for voltage noise on supply voltages of up to 45 mV (peak-to-peak) from DC to 20MHz.

Table 4-1(b) LPDDR4X Recommended DC Operating Conditions

DRAM	Symbol	Min	Typ	Max	Unit	Note
Core 1 Power	VDD1	1.7	1.8	1.95	V	1,2
Core 1 Power/Input Buffer Power	VDD2	1.06	1.1	1.17	V	1,2,3
I/O Buffer Power	VDDQ	0.57	0.6	0.65	V	2,3,4,5

Note:

1 VDD1 uses significantly less current than VDD2.

2 The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.

3 The voltage noise tolerance from DC to 20 MHz exceeding a pk-pk tolerance of 45 mV at the DRAM ball is not included in the TdIVW.

4 VDDQ(max) may be extended to 0.67 V as an option in case the operating clock frequency is equal or less than 800 Mhz.

5 Pull up, pull down and ZQ calibration tolerance spec is valid only in normal VDDQ tolerance range (0.57 V - 0.65 V).

4.2 Input Leakage Current

Table 4-2 Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit
Input Leakage current[1,2]	I_L	-4	4	uA

Note:

1 For CK_t, CK_c, CKE, CS, CA, ODT_CA and RESET_n. Any input 0V ≤ VIN ≤ VDD2 (All other pins not under test = 0V).

2 CA ODT is disabled for CK_t, CK_c, CS, and CA.

4.3 Input/Output Leakage Current

Table 4-3 Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit
Input/Output Leakage current[1,2]	I_{OZ}	-5	5	uA

Note:

1 For DQ, DQS_t, DQS_c and DMI. Any I/O 0V ≤ VOUT ≤ VDDQ.

2 I/Os status are disabled: High Impedance and ODT Off.

4.4 Operating Temperature Range

Table 4-4 Operating Temperature Range

Parameter/Condition	Parameter/Condition	Min	Max	Unit
Standard	T_{OPER}	-25	85	°C
Elevated		85	105	°C

Note:

1 Operating Temperature is the case surface temperature on the center-top side of the LPDDR4 device. For the measurement conditions, please refer to JESD51-2.

2 Some applications require operation of LPDDR4 in the maximum temperature conditions in the Elevated Temperature Range between 85 °C and 105 °C case temperature. For LPDDR4 devices, derating may be necessary to operate in this range. See MR4.

3 Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing derating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Elevated Temperature Ranges. For example, T_{CASE} may be above 85 °C when the temperature sensor indicates a temperature of less than 85 °C.

4.5 IDD Test Conditions and Specifications

Table 4.5-1 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Note
Operating one bank active-precharge current: tCK = tCKmin; tRC = tRCmin;CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable ,ODT disabled	IDD01	VDD1	
	IDD02	VDD2	
	IDD0Q	VDDQ	3
Idle power-down standby current: tCK = tCKmin;CKE is LOW;CS is LOW;All banks are idle;CA bus inputs are switching;Data bus inputs are stable,ODT disabled	IDD2P1	VDD1	
	IDD2P2	VDD2	
	IDD2PQ	VDDQ	3
Idle power-down standby current with clock stop:CK_t =LOW, CK_c =HIGH;CKE is LOW;CS is LOW;All banks are idle;CA bus inputs are stable;Data bus inputs are stable,ODT disabled	IDD2PS1	VDD1	
	IDD2PS2	VDD2	
	IDD2PSQ	VDDQ	3
Idle non power-down standby current:tCK = tCKmin;CKE is HIGH; CS is LOW;All banks are idle;CA bus inputs are switching;Data bus inputs are stable,ODT disabled	IDD2N1	VDD1	
	IDD2N2	VDD2	
	IDD2NQ	VDDQ	3
Idle non power-down standby current with clock stopped:CK_t=LOW; CK_c=HIGH;CKE is HIGH;CS is LOW;All banks are idle;CA bus inputs are stable;Data bus inputs are stable, ODT disabled	IDD2NS1	VDD1	
	IDD2NS2	VDD2	
	IDD2NSQ	VDDQ	3
Active power-down standby current:tCK = tCKmin;CKE is LOW;CS is LOW;One bank is active;CA bus inputs are switching;Data bus inputs are stable, ODT disabled	IDD3P1	VDD1	
	IDD3P2	VDD2	
	IDD3PQ	VDDQ	3
Active power-down standby current with clock stop:CK_t=LOW, CK_c=HIGH;CKE is LOW;CS is LOW;One bank is active;CA bus inputs are stable;Data bus inputs are stable,ODT disabled	IDD3PS1	VDD1	
	IDD3PS2	VDD2	
	IDD3PSQ	VDDQ	4
Active non-power-down standby current:tCK = tCKmin;CKE is HIGH;CS is LOW;One bank is active;CA bus inputs are switching; Data bus inputs are stable,ODT disabled	IDD3N1	VDD1	
	IDD3N2	VDD2	
	IDD3NQ	VDDQ	4
Active non-power-down standby current with clock stopped:CK_t=LOW, CK_c=HIGH;CKE is HIGH;CS is LOW; One bank is active;CA bus inputs are stable;Data bus inputs are stable,ODT disabled	IDD3NS1	VDD1	
	IDD3NS2	VDD2	
	IDD3NSQ	VDDQ	4
Operating burst READ current:tCK = tCKmin;CS is LOW between valid commands;One bank is active;BL = 16 or 32; RL = RL(MIN);CA bus inputs are switching;50% data change each burst transfer ODT disabled	IDD4R1	VDD1	
	IDD4R2	VDD2	
	IDD4RQ	VDDQ	5
Operating burst WRITE current:tCK = tCKmin;CS is LOW between valid commands;One bank is active;BL = 16 or 32; WL = WLmin;CA bus inputs are switching;50% data change each burst transfer ODT disabled	IDD4W1	VDD1	
	IDD4W2	VDD2	
	IDD4WQ	VDDQ	4
All bank REFRESH Burst current:tCK = tCKmin;CKE is HIGH between valid commands;tRC = tRFCabmin;Burst refresh;CA bus inputs are switching; Data bus inputs are stable;ODT disabled	IDD51	VDD1	
	IDD52	VDD2	
	IDD5Q	VDDQ	4
All bank REFRESH Average current:tCK = tCKmin;CKE is HIGH between valid commands;tRC = tREFI;CA bus inputs are switching;Data bus inputs are stable;ODT disabled	IDD5AB1	VDD1	
	IDD5AB2	VDD2	
	IDD5ABQ	VDDQ	4
Per bank REFRESH Average current:tCK = tCKmin; CKE is HIGH between valid commands;tRC = tREFI/8;CA bus inputs are switching;Data bus inputs are stable;ODT disabled	IDD5PB1	VDD1	
	IDD5PB2	VDD2	
	IDD5PBQ	VDDQ	4

Parameter/Condition	Symbol	Power Supply	Note
Power Down Self Refresh current (-25 ° C to +85 ° C):CK_t=LOW, CK_c=HIGH;CKE is LOW;CA bus inputs are stable;Data bus inputs are stable;Maximum 1x Self Refresh Rate;ODT disabled	IDD61	VDD1	6,7,8,10
	IDD62	VDD2	6,7,8,10
	IDD6Q	VDDQ	4,6,7,8,10
Power Down Self Refresh current (+85 ° C to +105 ° C): CK_t=LOW, CK_c=HIGH;CKE is LOW;CA bus inputs are stable; Data bus inputs are stable;Maximum 1x Self Refresh Rate;ODT disabled	IDD6ET1	VDD1	7,8,11
	IDD6ET2	VDD2	7,8,11
	IDD6ETQ	VDDQ	4,7,8,11

Note:

1 DBI Published IDD values are the maximum of the distribution of the arithmetic mean.

2 ODT disabled: MR11[2:0] = 000B.

3 IDD current specifications are tested after the device is properly initialized.

4 Measured currents are the summation of VDDQ and VDD2.

5 Guaranteed by design with output load = 5pF and RON = 40 Ω.

6 The 1x Self Refresh Rate is the rate at which the LPDDR4 device is refreshed internally during Self Refresh, before going into the elevated Temperature range.

7 This is the general definition that applies to full array Self Refresh.

8 Supplier datasheets may contain additional Self Refresh IDD values for temperature subranges within the Standard or elevated Temperature Ranges.

9 For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.

10 IDD6 85 °C is guaranteed, IDD6 45 °C is typical of the distribution of the arithmetic mean.

11 IDD6ET is a typical value, is sampled only, and is not tested.

12 Dual Channel devices are specified in dual channel operation (both channels operating together).

4.6 LPDDR4X IDD Parameters - Single Die

VDD2 = 1.06 ~ 1.17V, VDDQ = 0.57 ~ 0.65V; VDD1 = 1.70 ~ 1.95V; T_C = –25°C ~ +85°C

Symbol	Supply	3200 Mbps	Unit
$IDD0_1$	VDD1	3.5	mA
$IDD0_2$	VDD2	54.0	
IDD0Q	VDDQ	1.5	
$IDD2P_1$	VDD1	0.4	mA
$IDD2P_2$	VDD2	1.6	
IDD2PQ	VDDQ	1.5	
$IDD2PS_1$	VDD1	0.4	mA
$IDD2PS_2$	VDD2	1.6	
IDD2PSQ	VDDQ	1.5	
$IDD2N_1$	VDD1	0.4	mA
$IDD2N_2$	VDD2	22.4	
IDD2NQ	VDDQ	1.5	
$IDD2NS_1$	VDD1	0.4	mA
$IDD2NS_2$	VDD2	15.1	
IDD2NSQ	VDDQ	1.5	
$IDD3P_1$	VDD1	0.8	mA
$IDD3P_2$	VDD2	4.3	
IDD3PQ	VDDQ	1.5	
$IDD3PS_1$	VDD1	0.8	mA
$IDD3PS_2$	VDD2	4.2	
IDD3PSQ	VDDQ	1.5	
$IDD3N_1$	VDD1	1.7	mA
$IDD3N_2$	VDD2	26.4	
IDD3NQ	VDDQ	1.5	
$IDD3NS_1$	VDD1	1.7	mA
$IDD3NS_2$	VDD2	19.1	
IDD3NSQ	VDDQ	1.5	
$IDD4R_1$	VDD1	4.6	mA
$IDD4R_2$	VDD2	378	
IDD4RQ	VDDQ	85.8	
$IDD4W_1$	VDD1	2.0	mA
$IDD4W_2$	VDD2	300	
IDD4WQ	VDDQ	1.5	

Symbol	Supply	3200 Mbps	Unit
$IDD5_1$	VDD1	14.3	mA
$IDD5_2$	VDD2	147.1	
IDD5Q	VDDQ	1.5	
$IDD5AB_1$	VDD1	1.6	mA
$IDD5AB_2$	VDD2	32.4	
IDD5ABQ	VDDQ	1.5	
$IDD5PB_1$	VDD1	1.7	mA
$IDD5PB_2$	VDD2	32.9	
IDD5PBQ	VDDQ	1.5	

4.7 LPDDR4X IDD6 Parameters - Single Die

VDD2 = 1.06 ~ 1.17V, VDDQ = 0.57 ~ 0.65V; VDD1 = 1.70 ~ 1.95V; T_C = –25°C ~ +85°C

Temperature	Symbol	Supply	Full-Array Self Refresh Current	Unit
25°C	$IDD6_1$	VDD1	0.53	mA
	$IDD6_2$	VDD2	1.95	
	IDD6Q	VDDQ	0.15	
85°C	$IDD6_1$	VDD1	1.43	mA
	$IDD6_2$	VDD2	9.68	
	IDD6Q	VDDQ	0.15	

5. Electrical Characteristics and AC Timing

5.1 Clock Timing

Table 5-1 Clock AC Timings

Parameter	Symbol	1600/2400/3200		Unit
		Min	Max	
Clock Timing				
Average High pulse width	tCH(avg)	0.46	0.54	tCK(avg)
Average Low pulse width	tCL(avg)	0.46	0.54	tCK(avg)
Absolute clock period	tCK(abs)	tCK(avg)MIN +tJIT(per)MIN	-	ns
Absolute High clock pulse width	tCH(abs)	0.43	0.57	tCK(avg)
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	tCK(avg)

Parameter	Symbol	1600		2400		3200		Unit
		Min	Max	Min	Max	Min	Max	
Clock Timing								
Average clock period	tCK(avg)	1.25	100	0.833	100	0.625	100	ns
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40	ps
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	140	-	100	-	80	ps

5.2 DRAM Data Timing

Table 5-2 Read Output Timings

Unit UI = tCK(avg)min/2

Symbol	Parameter	DQ-1600/1867		DQ-2133/2400		DQ-3200		Unit	Note
		Min	Max	Min	Max	Min	Max		
Data Timing									
tDQSQ	DQS_t,DQS_c to DQ Skew total, per group, per access (DBIDisabled)	-	0.18	-	0.18	-	0.18	UI	
tQH	DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	UI	
tQW_total	DQ output window time total, per pin (DBI-Disabled)	0.75	-	0.73	-	0.7	-	UI	3
tQW_dj	DQ output window time deterministic, per pin (DBIDisabled)	TBD	-	TBD	-	TBD	-	UI	2,3
tDQSQ_DBI	DQS_t,DQS_c to DQ Skew total,per group, per access (DBI-Enabled)	-	0.18	-	0.18	-	0.18	UI	6
tQH_DBI	DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	Min (tQSH_DBI,tQSL_DBI)	-	Min (tQSH_DBI,tQSL_DBI)	-	Min (tQSH_DBI,tQSL_DBI)	TBD	UI	
tQW_total_DBI	DQ output window time total, per pin (DBI-Enabled)	0.75	-	0.73	-	0.7	-	UI	3
Data Strobe Timing									
tQSL	DQS, DQS# differential output low time (DBI-Disabled)	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCK(avg)	3,4
tQSH	DQS, DQS# differential output high time (DBI-Disabled)	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCL(abs) -0.05	-	tCK(avg)	3,5
tQSL_DBI	DQS, DQS# differential output low time (DBI-Enabled)	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCK(avg)	4,6
tQSH_DBI	DQS, DQS# differential output high time (DBI-Enabled)	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCK(avg)	5,6

a. The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies.

Note:

1 The deterministic component of the total timing. Measurement method tbd.

2 This parameter will be characterized and guaranteed by design.

3 This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

4 tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.

5 tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.

6 This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

5.3 DQ Rx Voltage and Timing

Table 5-3 DRAM DQs in Receive Mode

* UI=tCK(avg)min/2

Symbol	Parameter	DQ-1600/1867[a]/2133/2400		DQ-3200		Unit	Note
		Min	Max	Min	Max		
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	140	mV	1,2,3,4
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.22	-	0.25	UI	1,2,4
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	UI	1,2,4,12
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	UI	5,13
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45		0.45		UI	6
tDQS2DQ	DQ to DQS offset	200	800	200	800	ps	7
tDQ2DQ	DQ to DQ offset	-	30	-	30	ps	8
tQSL	tDQS2DQ_temp DQ to DQS offset temperature variation	-	0.6	-	0.6	ps/°C	9
tDQS2DQ_volt	DQ to DQS offset voltage variation	-	33	-	33	ps/50 mV	10
SRIN_dIVW	Input Slew Rate over VdIVW_total	1	7	1	7	V/ns	11
tDQS2DQ_rank2rank	DQ to DQS offset rank to rank variation	-	200	-	200	ps	14,15,16

a. The Rx voltage and absolute timing requirements apply for all DQ operating frequencies at or below 1600 for all speed bins. For example TdIVW_total(ps) = 137.5ps at or below 1600 operating frequencies

Note:

1 The Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20 MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.

2 The design specification is a BER <TBD. The BER will be characterized and extrapolated if necessary using a dual dirac method.

3 Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).

4 Vcent_DQ must be within the adjustment range of the DQ internal Vref.

5 DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ.

6 DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).

7 DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.

8 DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.

9 TDQS2DQ max delay variation as a function of temperature.

10 TDQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD2. It includes the VDDQ and VDD2 AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. For tester measurement VDDQ = VDD2 is assumed.

11 Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).

12 Rx mask defined for a one pin toggling with other DQ signals in a steady state.

13 VIHL_AC does not have to be met when no transitions are occurring.

14 The same voltage and temperature are applied to tDQS2DQ_rank2rank.

15 tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

16 tDQS2DQ_rabk2rank support was added to JESD209-4B, some older devices designed to support JESD209-4 and JESD209-4A may not support this parameter. Refer to vendor datasheet.

6. AC Timing Parameters

6.1 Read AC Timing

Table 6-1 Read AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
Core Parameters			533/1066/1600/2133/2667/3200	
READ preamble	tRPRE	MIN	1.8	tCK(avg)
0.5 tCK READ postamble	tRPST	MIN	0.4	tCK(avg)
1.5 tCK READ postamble	tRPST	MIN	1.4	tCK(avg)
DQ low-impedance time from CK_t, CK_c	tLZ(DQ)	MIN	(RL x tCK) + tDQSCK(Min) - 200ps	ps
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	MAX	(RL x tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2 x tCK) - 100ps	ps
DQS_c low-impedance time from CK_t, CK_c	tLZ(DQS)	MIN	(RL x tCK) + tDQSCK(Min) - (tRPRE(Max) x tCK) - 200ps	ps
DQS_c high impedance time from CK_t, CK_c	tHZ(DQS)	MAX	(RL x tCK) + tDQSCK(Max) +(BL/2 x tCK) + (RPST(Max) x tCK) - 100ps	ps
DQS-DQ skew	tDQSQ	MAX	0.18	UI

6.2 tDQSCK Timing

Table 6.2-1 tDQSCK Timing Table

Parameter	Symbol	Min	Max	Unit	Note
DQS Output Access Time from CK_t/CK_c	tDQSCK	1.5	3.5	ns	1
DQS Output Access Time from CK_t/CK_c -Temperature Variation	tDQSCK_temp	-	4	ps/°C	2
DQS Output Access Time from CK_t/CK_c -Voltage Variation	tDQSCK_volt	-	7	ps/mV	3

Note:

1 Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies > 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.

2 tDQSCK_temp max delay variation as a function of Temperature.

3 tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. tDQSCK_volt should be used to calculate timing variation due to VDDQ and VDD2 noise < 20 MHz. Host controller do not need to account for any variation due to VDDQ and VDD2 noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1-tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}]/abs{V1-V2}. For tester measurement VDDQ = VDD2 is assumed.

Table 6.2-2 CK to DQS Rank to Rank Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
Read Timing			1600/1866/2133/2667/3200		
CK to DQS Rank to Rank variation	tDQSCK_rank2rank	Max	1.0	ns	1,2

Note:

1 The same voltage and temperature are applied to tDQS2CK_rank2rank.
2 tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

6.3 Write AC Timing

Table 6-3 Write AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
Write Timing			**533/1066/1600/2133/2667/3200**	
Write command to 1st DQS latching	tDQSS	Min	0.75	tCK(avg)
		Max	1.25	
DQS input high-level	tDQSH	Min	0.4	tCK(avg)
DQS input low-level width	tDQSL	Min	0.4	tCK(avg)
DQS falling edge to CK setup time	tDSS	Min	0.2	tCK(avg)
DQS falling edge hold time from CK	tDSH	Min	0.2	tCK(avg)
Write preamble	tWPRE	Min	1.8	tCK(avg)
0.5 tCK Write postamble	tWPST[1]	Min	0.4	tCK(avg)
1.5 tCK Write postamble	tWPST[1]	Min	1.4	tCK(avg)

Note:

The length of Write Postamble depends on MR3 OP1 setting.

6.4 Self Refresh Timing

Table 6-4 Self Refresh AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
			533/1066/1600/2133/2667/3200		
Self Refresh Timing					
Delay from SRE command to CKE Input low	tESCKE	Min	Max(1.75ns, 3tCK)	ns	1
Minimum Self Refresh Time	tSR	Min	Max(15ns, 3tCK)	ns	1
Exit Self Refresh to Valid commands	tXSR	Min	Max(tRFCab +7.5ns,2tCK)	ns	2

Note:

Delay time has to satisfy both analog time(ns) and clock count(tCK). It means that tESCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired.

6.5 Mode Register Read/Write AC Timing

Table 6-5 Mode Register Read/Write AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
Mode Register Read/Write Timing				
Additional time after tXP has expired until MRR command may be issued	tMRRI	Min	tRCD + 3nCK	-
MODE REGISTER READ command period	tMRR	Min	8	nCK
MODE REGISTER WRITE command period	tMRW	Min	MAX(10ns,10nCK)	-
Mode register set command delay	tMRD	Min	max(14ns,10nCK)	-

6.6 VRCG Enable/Disable Timing

Table 6-6 VRCG Enable/Disable Timing Table

Speed		533/1066/1600/2133/2667/3200		Unit
Parameter	Symbol	Min	Max	
VREF high current mode enable time	tVRCG_ENABLE	-	200	ns
VREF high current mode disable time	tVRCG_DISABLE	-	100	

6.7 Command Bus Training AC Timing

Table 6.7-1 Command Bus Training AC Timing Table

Parameter	Symbol	Min/Max	Data Rate 533/1066/1600/2133/2667/3200	Unit
Command Bus Training Timing				
Valid Clock Requirement after CKE Input low	tCKELCK	Min	Max(5ns, 5nCK)	-
Data Setup for VREF Training Mode	tDStrain	Min	2	ns
Data Hold for VREF Training Mode	tDHtrain	Min	2	ns
Asynchronous Data Read	tADR	Max	20	ns
CA Bus Training Command to CA Bus Training Command Delay	tCACD[2]	Min	RU(tADR/tCK)	tCK
Valid Strobe Requirement before CKE Low	tDQSCKE[1]	Min	10	ns
First CA Bus Training Command Following CKE Low	tCAENT	Min	250	ns
VREF Step Time– multiple steps	tVREFCA_LONG	Max	250	ns
VREF Step Time– one step	tVREFCA_SHORT	Max	80	ns
Valid Clock Requirement before CS High	tCKPRECS	Min	2tck + tXP (tXP = max(7.5ns, 5nCK))	-
Valid Clock Requirement after CS High	tCKPSTCS	Min	max(7.5ns, 5nCK))	-
Minimum delay from CS to DQS toggle in command bus training	tCS_VREF	Min	2	tCK
Minimum delay from CKE High to Strobe High Impedance	tCKEHDQS	Min	10	ns
Valid Clock Requirement before CKE Input High	tCKCKEH	Min	Max(1.75ns, 3nCK)	-
CA Bus Training CKE High to DQ Tri-state	tMRZ	Min	1.5	ns
ODT turn-on Latency from CKE	tCKELODTon	Min	20	ns
ODT turn-off Latency from CKE	tCKELODToff	Min	20	ns
Exit Command Bus Training Mode to next valid command delay[3]	tXCBT_Short	Min	Max(5nCK, 200ns)	-
	tXCBT_Middle	Min	Max(5nCK, 200ns)	-
	tXCBT_Long	Min	Max(5nCK, 250ns)	-

Note:

1 DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.

2 If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.

3 Exit Command Bus Training Mode to next valid command delay Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in Table 61. Additionally exit Command Bus Training Mode to next valid command delay Time may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.

Table 6.7-2 Command Bus Training AC Timing Table for Mode 1

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
			533/1066/1600/2133/2667/3200		
Command Bus Training Timing					
Clock and Command Valid after CKE Low	tCKELCK	Min	max(7.5ns, 3nCK)	tCK	
Asynchronous Data Read	tADR	Max	20	ns	
CA Bus Training Command to CA Bus Training Command Delay	tCACD	Min	RU(tADR/tCK)	tCK	1
First CA Bus Training Command Following CKE Low	tCAENT	Min	250	ns	
Valid Clock Requirement before CS High	tCKPRECS	Min	2tCK + tXP (tXP = max(7.5ns, 5nCK))		
Valid Clock Requirement after CS High	tCKPSTCS	Min	max(7.5ns, 5nCK))		
Clock and Command Valid before CKE High	tCKCKEH	Min	2	tCK	
CA Bus Training CKE High to DQ Tri-state	tMRZ	Min	1.5	ns	
ODT turn-on Latency from CKE	tCKELODTon	Min	20	ns	
ODT turn-off Latency from CKE	tCKELODToff	Min	20	ns	
Exit Command Bus Training Mode to next valid command delay	tXCBT_Short	Min	Max(5nCK, 200ns)		2
	tXCBT_Middle	Min	Max(5nCK, 200ns)		2
	tXCBT_Long	Min	Max(5nCK, 250ns)		2

Note:

1 If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.

2 Exit Command Bus Training Mode to next valid command delay Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. Additionally exit Command Bus Training Mode to next valid command delay Time may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.

Table 6.7-3 Command Bus Training AC Timing Table for Mode 2

Parameter	Symbol	Min/Max	Data Rate 533/1066/1600/2133/2667/3200	Unit	Note
Command Bus Training Timing					
Valid Clock Requirement after CKE Input low	tCKELCK	Min	Max(5ns,5nCK)	ns	
Valid Clock Requirement before CS High	tCKPRECS	Min	2tCK + tXP (tXP = max(7.5ns, 5nCK))	-	
Valid Clock Requirement after CS High	tCKPSTCS	Min	max(7.5ns, 5nCK))	-	
Valid Strobe Requirement before CKE Low	tDQSCKE	Min	10	ns	1
First CA Bus Training Command Following CKE Low	tCAENT	Min	250	ns	
VREF Step Time - Long	tVREFCA_Long	Max	250	ns	2
VREF Step Time - Middle	tVREFCA_Middle	Max	200	ns	3
VREF Step Time - Short	tVREFCA_Short	Max	100	ns	4
Data Setup for Vref Training Mode	tDStrain	Min	2	ns	
Data Hold for Vref Training Mode	tDHtrain	Min	2	ns	
Asynchronous Data Read Valid Window	tADVW	Min	16	ns	
		Max	80	ns	
DQS Input period at CBT mode	tDQSICYC	Min	5	ns	
		Max	100	ns	
Asynchronous Data Read	tADR	Max	20	ns	
DQS_c high impedance time from CS High	tHZCBT	Min	0	ns	
Asynchronous Data Read to DQ7 toggle	tAD2DQ7	Min	3	ns	
		Max	10	ns	
DQ7sample hold time	tDQ7SH	Min	10	ns	
		Max	60	ns	
Asynchronous Data Read Pulse Width	tADSPW	Min	3	ns	
		Max	10	ns	
Hi-Z to asynchronous Vref-CA valid data	tHZ2VREF	Min	Max(10ns, 5nCK)	-	
Read to Write Delay at CBT mode	tCBTRTW	Min	2	ns	
CA Bus Training Command to CA Bus Training Command Delay	tCACD	Min	Max(110ns, 4nCK)		
Minimum delay from CKE High to Strobe High Impedance	tCKEHDQS	Min	10	ns	
Clock and Command Valid before CKE High	tCKCKEH	Min	Max(1.75ns,3nCK)		
ODT turn-on Latency from CKE	tCKELODTon	Max	20	ns	
ODT turn-off Latency from CKE for ODT_CA	tCKELODToff	Max	20	ns	

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
			533/1066/1600/2133/2667/3200		
ODT turn-off Latency from CKE for ODT_DQ and DQS	tCKEHODToff	Max	20	ns	
ODT_DQ turn-off Latency from CS high during CB Training	tODToffCBT	Max	20	ns	
ODT_DQ turn-on Latency from the end of Valid Data out	tODTonCBT	Max	Max(10ns, 5nCK)		
Exit Command Bus Training Mode to next valid command delay	tXCBT_Short	Min	Max(5nCK, 200ns)		5
	tXCBT_Middle	Min	Max(5nCK, 200ns)		5
	tXCBT_Long	Min	Max(5nCK, 250ns)		5

Note:

1 DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.

2 VREFCA_Long is the time including up to VREFmin to VREFmax or VREFmax to VREFmin change across the VREFDQ Range in VREF voltage.

3 VREF_Middle is at least 2 stepsizes increment/decrement change within the same VREFDQ range in VREF voltage.

4 VREF_Short is for a single stepsize increment/decrement change in VREF voltage.

5 Exit Command Bus Training Mode to next valid command delay Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1.

6.8 Frequency Set Point Timing

Table 6-8 Frequency Set Point Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
			533/1066/1600/2133/2667/3200	
Frequency Set Point parameters				
Frequency Set Point Switching Time	tFC_Short[1]	Min	200	ns
Minimum Self Refresh Time	tFC_Middle[1]	Min	200	ns
Exit Self Refresh to Valid commands	tFC_Long[1]	Min	250	ns
Valid Clock Requirement after Entering FSP Change	tCKFSPE	Min	max(7.5ns, 4nCK)	-
Valid Clock Requirement before 1st Valid Command after FSP change	tCKFSPX	Min	max(7.5ns, 4nCK)	-

Note:

Frequency Set Point Switching Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. Additionally change of Frequency Set Point may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.

6.9 Write Leveling Timing

Table 6.9-1 Write Leveling Timing Table

Parameter	Symbol	Min/Max	Value	Unit
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSEN	Min	20	tCK
		Max	-	
Write preamble for Write Leveling	tWLWPRE	Min	20	tCK
		Max	-	
First DQS_t/DQS_c edge after write leveling mode is programmed	tWLMRD	Min	40	tCK
		Max	-	
Write leveling output delay	tWLO	Min	0	ns
		Max	20	
Mode register set command delay	tMRD	Min	max(14ns, 10nCK)	ns
		Max	-	
Valid Clock Requirement before DQS Toggle	tCKPRDQS	Min	max(7.5ns, 4nCK)	-
		Max	-	
Valid Clock Requirement after DQS Toggle	tCKPSTDQS	Min	max(7.5ns, 4nCK)	-
		Max	-	

Table 6.9-2 Write Leveling Setup and Hold Time

Parameter	Symbol	Min/Max	Data Rate			Unit
			1600	2400	3200	
Write Leveling Parameters						
Parameters Write leveling hold time	tWLH	Min	150	100	75	ps
Write leveling setup time	tWLS	Min	150	100	75	ps
Write leveling input valid window	tWLIVW	Min	240	160	120	ps

6.10 MPC [Write FIFO] AC Timing

Table 6.10 MPC [Write FIFO] AC Timing Table

Parameter	Symbol	Min/Max	Data Rate
			533/1066/1600/2133/2667/3200
MPC Write FIFO Timing			
Additional time after tXP has expired until MPC [Write FIFO] command may be issued	tMPCWR	Min	tRCD + 3nCK

6-11 DQS Interval Oscillator AC Timing

Table 6-11 DQS Interval Oscillator AC Timing Table

Parameter	Symbol	Min/Max	Value	Unit
Delay time from OSC stop to Mode Register Readout	tOSCO	Min	Max(40ns,8nCK)	ns

Note:

Start DQS OSC command is prohibited until tOSCO(Min) is satisfied.

6.12 Read Preamble Training Timing

Table 6-12 Read Preamble Training Timing Table

Parameter	Symbol	Min	Max
Delay from MRW command to DQS Driven	tSDO	-	Min(12nCK, 20ns)

6.13 ZQ Calibration Timing

Table 6-13 ZQCal Timing Table

Parameter	Symbol	Min /Max	Value	Unit
ZQ Calibration Time	tZQCAL	Min	1	us
ZQ Calibration Latch Time	tZQLAT	Min	max(30ns,8nCK)	ns
ZQ Calibration Reset Time	tZQRESET	Min	max(50ns,3nCK)	ns

6.14 ODT CA AC Timing

Table 6-14 ODT CA AC Timing Table

Speed		600/1866/2133/2400/3200	
Parameter	Symbol	MIN	MAX
ODT CA Value Update Time	tODTUP	RU(TBDns/tCK(avg))	-

6-15 Power-Down AC Timing

Table 6-15 Power-Down AC Timing

Parameter	Symbol	Min/Max	Data Rate 533/1066/1600/2133 /2667/3200	Unit	Note
Power Down Timing					
CKE minimum pulse width (HIGH and LOW pulse width) tCKE	tCKE	Min	Max(7.5ns,4nCK)	-	
Delay from valid command to CKE input LOW	tCMDCKE	Min	Max(1.75ns,3nCK)	ns	1
Valid Clock Requirement after CKE Input low	tCKELCK	Min	Max(5ns,5nCK)	ns	1
Valid CS Requirement before CKE Input Low	tCSCKE	Min	1.75	ns	
Valid CS Requirement after CKE Input low	tCKELCS	Min	Max(5ns,5nCK)	ns	
Valid Clock Requirement before CKE Input High	tCKCKEH	Min	Max(1.75ns,3nCK)	ns	1
Exit power- down to next valid command delay	tXP	Min	Max(7.5ns,5nCK)	ns	1
Valid CS Requirement before CKE Input High	tCSCKEH	Min	1.75	ns	
Valid CS Requirement after CKE Input High	tCKEHCS	Min	Max(7.5ns,5nCK)	ns	
Valid Clock and CS Requirement after CKE Input low after MRW Command	tMRWCKEL	Min	Max(14ns,10nCK)	ns	1
Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command	tZQCKE	Min	Max(1.75ns,3nCK)	ns	1

Note:

Delay time has to satisfy both analog time(ns) and clock count(nCK).