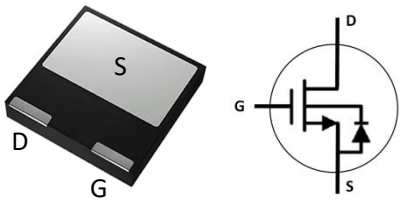
650V GaN Power Transistor (FET)

Features

- Easy to use, compatible with standard gate drivers
- Low Q_{rr}, no free-wheeling diode required
- Excellent Q_g x $R_{DS(on)}$ product (FOM)
- Low switching loss
- RoHS compliant and Halogen-free

Product Summary		
V_{DSS}	650	V
$R_{DS(on),\ typ}$	120	mΩ
$Q_{G,\ typ}$	12	nC
$Q_{RR,\ typ}$	80	nC



Applications

- Power adapters
- Telecom and datacom
- Automotive
- Servo motors

Packaging

Part Number	Package	Packaging	Base QTY
XG65T125HS1B	DFN 8*8mm	Tape and Reel	2500

Maximum ratings, at T_C=25 °C, unless otherwise specified

Symbol	Parameter		Limit Value	Unit
I_D	Continuous drain current @T_C=25°C		18	A
	Continuous drain current @T_C=100°C		11.5	A
I_{DM}	Pulsed drain current @T_C=25°C (pulse width: 10us)		82	A
	Pulsed drain current @T_C=150°C (pulse width: 10us)		62	A
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)		650	V
V_{GSS}	Gate to source voltage		±20	V
P_D	Maximum power dissipation @T_C=25°C		67.5	W
T_C	Operating temperature	Case	-55 to 150	°C
T_J		Junction	-55 to 150	°C
T_S	Storage temperature		-55 to 150	°C
T_{CSOLD}	Soldering peak temperature		260	°C

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	1.85	°C/W
$R_{\Theta JA}$	Junction-to-ambient [a]	50	°C/W

Notes:

a. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm^2 copper area and 70μm thickness)

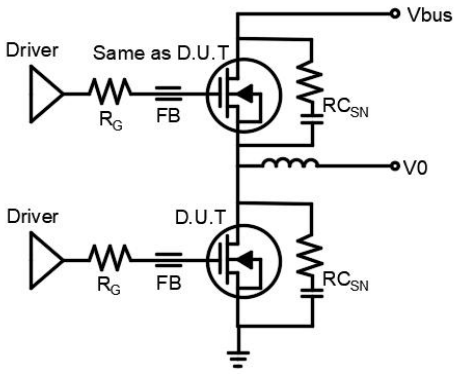
Electrical Parameters, at T_J=25 °C, unless otherwise specified

Symbol	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics					
$V_{DSS-MAX}$	650	-	-	V	V_{GS}=0V
BV_{DSS}	-	1700	-	V	V_{GS}=0V, I_{DSS}=250μA
$V_{GS(th)}$	-	1.82	-	V	V_{DS}=V_{GS}, I_D=500μA
$R_{DS(on)}$[a]	-	120	145	mΩ	V_{GS}=8V, I_D=4A, T_J=25°C
	-	240	-		V_{GS}=8V, I_D=4A, T_J=150°C
I_{DSS}	-	8	20	μA	V_{DS}=700V, V_{GS}=0V, T_J=25°C
	-	70	-	μA	V_{DS}=700V, V_{GS}=0V, T_J=150°C
I_{GSS}	-	-	150	nA	V_{GS}=20V
	-	-	-150	nA	V_{GS}=-20V
C_{ISS}	-	500	-	pF	V_{GS}=0V, V_{DS}=650V, f=1MHz
C_{OSS}	-	50	-	pF	
C_{RSS}	-	4	-	pF	
$C_{O(er)}$	-	60	-	pF	V_{GS}=0V, V_{DS}=0 to 650V
$C_{O(tr)}$	-	100	-	pF	
Q_G	-	12	-	nC	V_{DS}=400V, V_{GS}=0V to 8V, I_D=10A
Q_{GS}	-	3.7	-		
Q_{GD}	-	2.2	-		
$t_{D(on)}$	-	24	-	nS	V_{DS}=400V, V_{GS}=0V to 12V, I_D=10A, R_G=20Ω
t_R	-	14	-		
$t_{D(off)}$	-	100	-		
t_F	-	8	-		
Reverse Device Characteristics					
V_{SD}	-	1.4	-	V	V_{GS}=0V, I_S=5A, T_J=25°C
	-	2.2	-		V_{GS}=0V, I_S=10A, T_J=25°C
	-	3.2	-		V_{GS}=0V, I_S=10A, T_J=150°C
t_{RR}	-	12	-	ns	I_S=10A, V_{GS}=0V, d_i/d_t=2300A/us, V_{DD}=400V
Q_{RR}	-	80	-	nC	

Notes:

a. Dynamic on-resistance; see Fig. 15 and 16 for test circuit and conditions

Circuit Implementation



Recommended Drive Circuit

Recommended gate drive: (0 V, 12 V) with $R_{G(tot)}$ = 21 Ω, where $R_{G(tot)} = R_G + R_{Driver}$

Gate Ferrite Bead (FB)	Gate Resistance1 (R_G)	RC Snubber (RC_{SN})
MPZ1608S471ATA00	20 Ω	47 pF + 15 Ω

Notes:

a. RCsn should be placed as close as possible to the drain pin

b. The layout and wiring of the drive circuit should be as short as possible

Typical Characteristics, at T_C=25 °C, unless otherwise specified

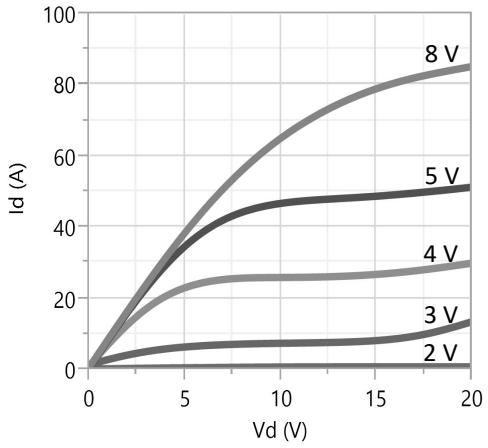


Figure 1. Typical Output Characteristics T_J=25°C

Parameter: V_{GS}

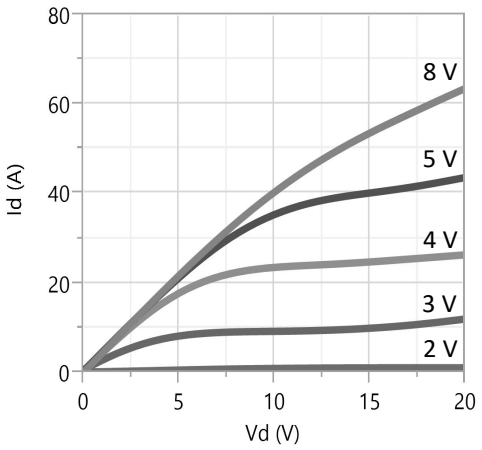


Figure 2. Typical Output Characteristics T_J=150°C

Parameter: V_{GS}

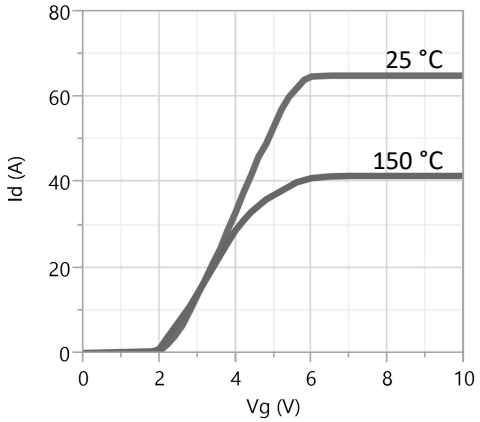


Figure 3. Typical Transfer Characteristics

V_{DS}=10V, Parameter: T_J

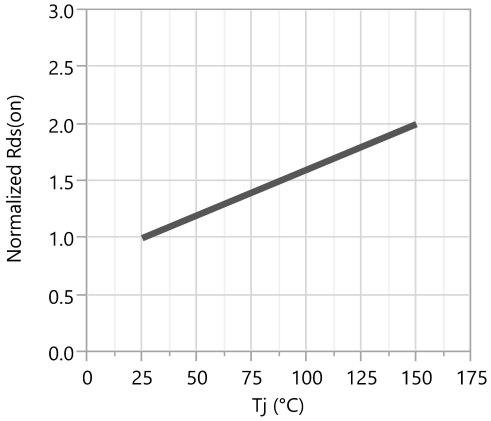


Figure 4. Normalized On-resistance

I_D=4A, V_{GS}=8V

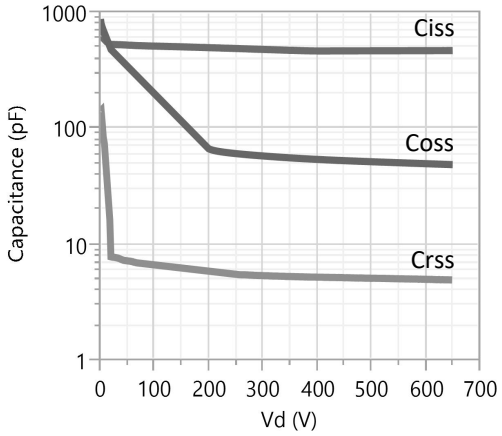


Figure 5. Typical Capacitance

V_{GS}=0V, f=1MHZ

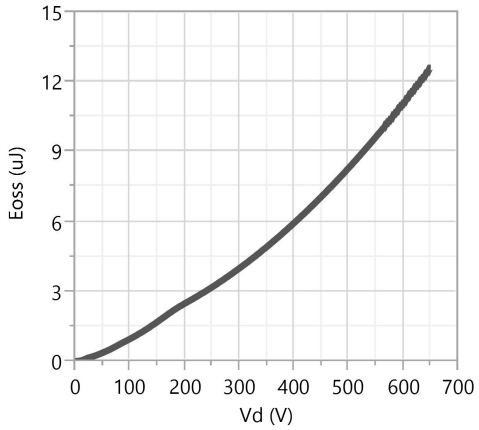


Figure 6. Typical Coss Stored Energy

Typical Characteristics, at T_C=25 °C, unless otherwise specified

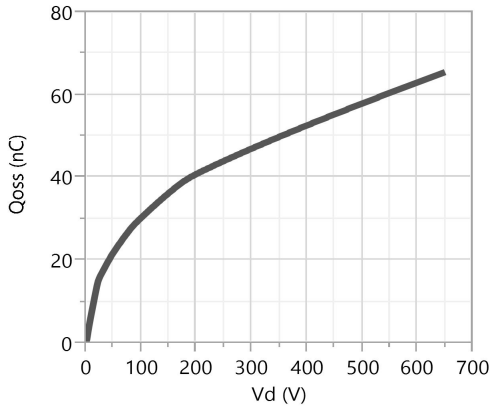


Figure 7. Typical Qoss

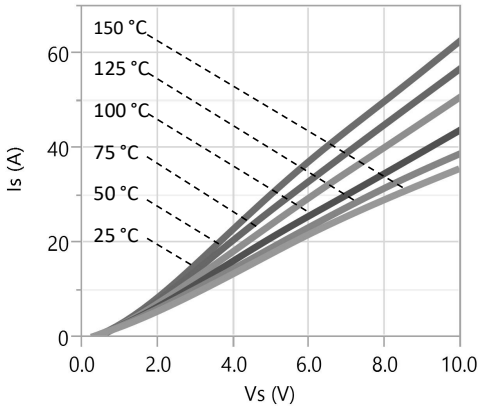


Figure 8. Forward Characteristic of Rev. Diode

Is=f(V_S), Parameter T_J

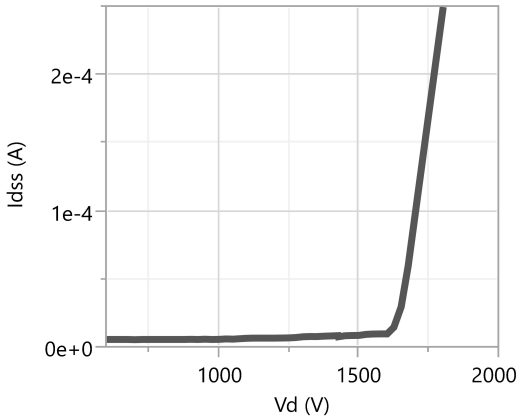


Figure 9. Drain-Source Breakdown Voltage

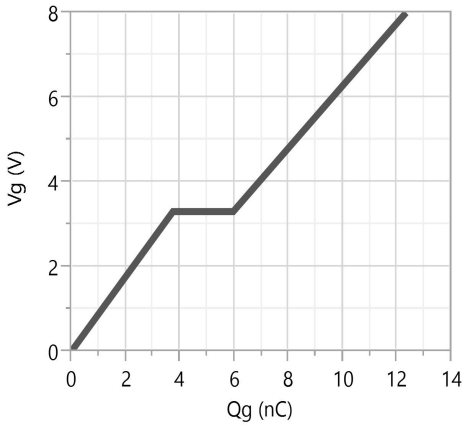


Figure 10. Typical Gate Charge

I_{DS}=10A, V_{DS}=400V

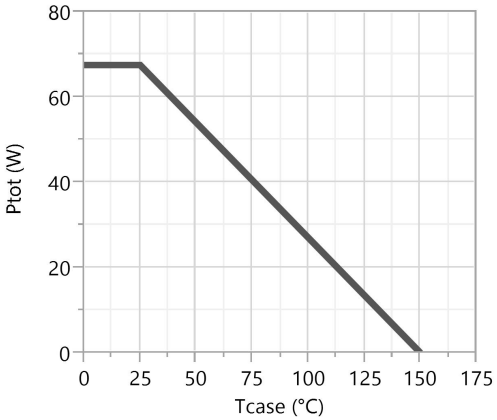


Figure 11. Power Dissipation

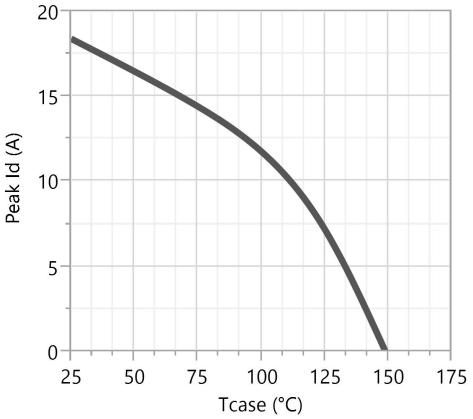


Figure 12. Current Derating

Test Circuits and Waveforms

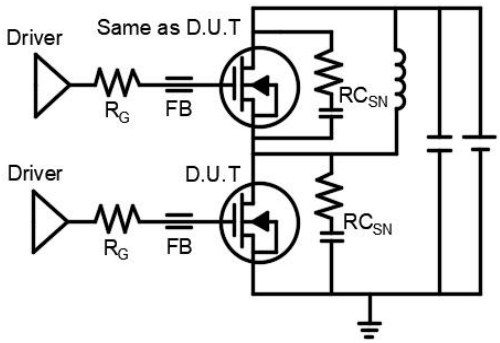


Figure 13. Switching Time Test Circuit

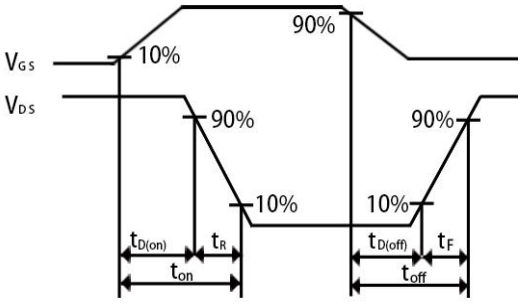


Figure 14. Switching Time Waveform

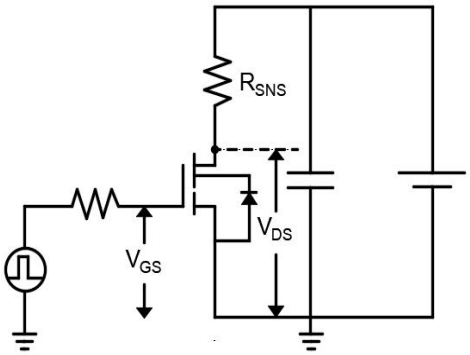


Figure 15. Dynamic $R_{DS(on)}$ Test Circuit

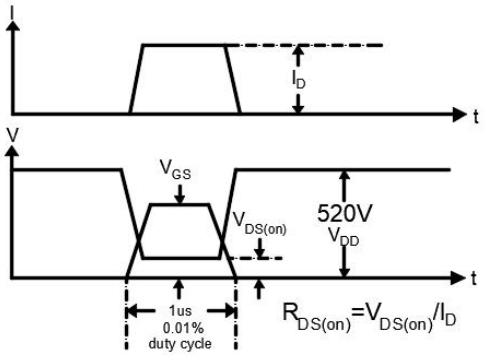


Figure 16. Dynamic $R_{DS(on)}$ Waveform

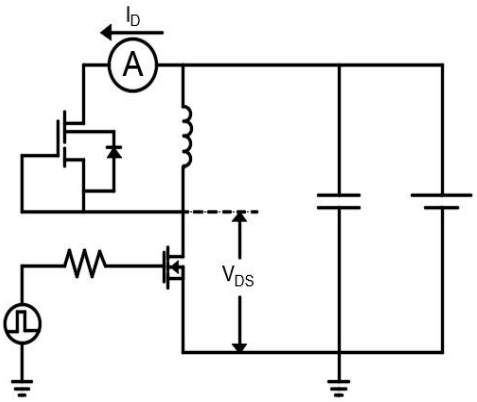


Figure 17. Diode Characteristic Test Circuit

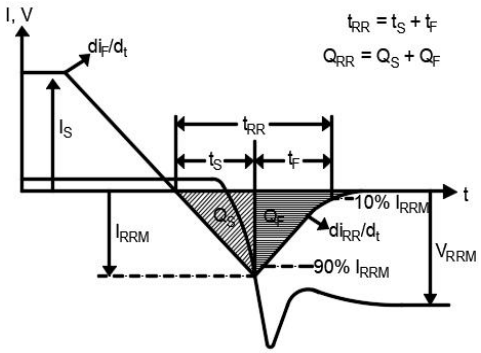


Figure 22. Diode Recovery Waveform

Design Considerations

Fast switching GaN device can reduce power conversion losses, and thus enable high frequency operations. Certain PCB design rules and instructions, however, need to be followed to take full advantages of fast switching GaN devices.

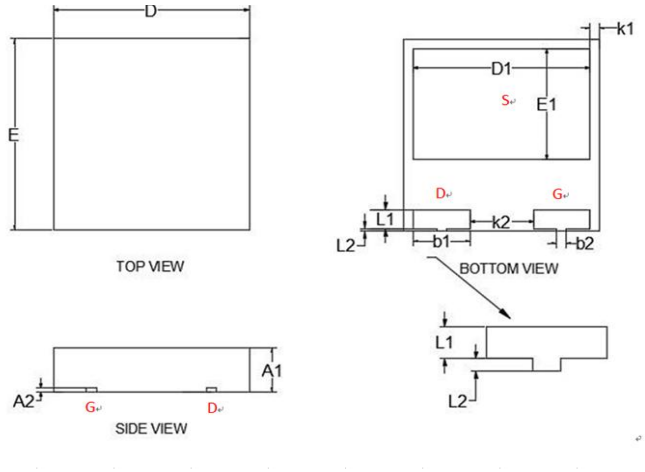
Before evaluating Xinguan's GaN devices, please refer to the table below which provides some practical rules that should be followed during the evaluation.

When Evaluating Xinguan's GaN Devices:

DO	DO NOT
Make sure the traces are as short as possible for both drive and power loops to minimize parasitic inductance	Using Xinguan's devices in GDS board layouts
Use the test tool with the shortest inductive loop, and make sure test points should be placed close enough	Use differential mode probe or probe ground clip with long wires
Minimize the lead length of TO packages when installing them to PCB	Use long traces in drive circuit, or long lead length of the devices

Mechanical

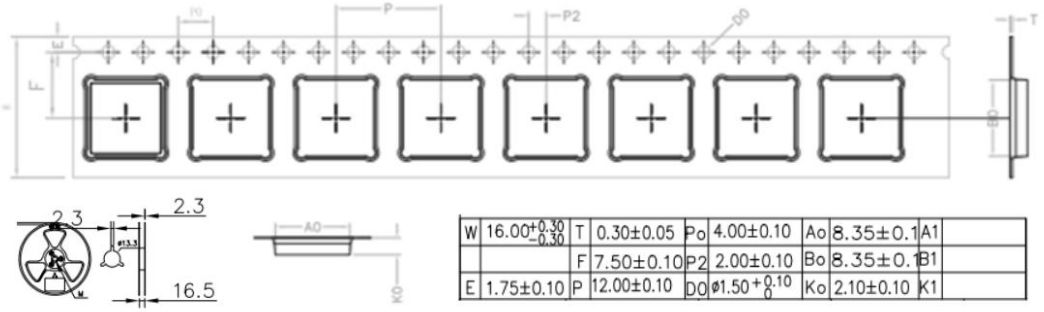
DFN 8*8 (HS) Package



Symbol	Dimensions in Millimeters		
	MIN	NOM	MAX
A1	1.825	1.850	1.875
A2	0.195	0.203	0.211
D	7.950	8.000	8.050
E	7.950	8.000	8.050
D1	7.150	7.200	7.250
E1	4.550	4.600	4.650
K1	0.375	0.400	0.425
K2	2.575	2.600	2.625
b1	2.275	2.300	2.325
b2	0.375	0.400	0.425
L1	0.775	0.800	0.825
L2	0.075	0.100	0.125

Package Outlines

Dimensions are show in millimeters



W	16.00±0.30	T	0.30±0.05	Po	4.00±0.10	Ao	8.35±0.1	A1	
		F	7.50±0.10	P2	2.00±0.10	Bo	8.35±0.1	B1	
E	1.75±0.10	P	12.00±0.10	D0	ø1.50 +0.10 0	Ko	2.10±0.10	K1	

Revision History

Version	Date	Change(s)
1.0	7/30/2020	Release formal datasheet