

General Description

The WST2300 is the highest performance trench N-Ch MOSFET with extreme high cell density, which provide excellent RDSON and gate charge for most of the small power switching and load switch applications.

The WST2300 meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

Product Summery

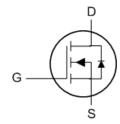
BVDSS	RDSON	ID
20V	50mΩ	4.4A

Applications

- High Frequency Point-of-Load Synchronous s Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

SOT-23-3L Pin Configuration





Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	±12	V
I _D @T _C =25℃	Continuous Drain Current, V _{GS} @ 4.5V ¹	4.4	А
I _D @T _C =70°C	Continuous Drain Current, V _{GS} @ 4.5V ¹	3.2	А
I _{DM}	Pulsed Drain Current ²	12	Α
P _D @T _A =25°C	Total Power Dissipation ³	1.0	W
T _{STG}	Storage Temperature Range -55 to 150		$^{\circ}$
T _J	Operating Junction Temperature Range	-55 to 150	$^{\circ}$

Thermal Data

Symbol	Parameter	Тур.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹		200	°C/W
$R_{ heta JC}$	Thermal Resistance Junction-Case ¹		75	°C/W



Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	20			V
$\triangle BV_{DSS}/\triangle T_{J}$	BVDSS Temperature Coefficient	Reference to 25℃, I _D =1mA		0.024		V/°C
	Static Drain-Source On-Resistance ²	V _{GS} =4.5V , I _D =1.8A		50	65	mΩ
R _{DS(ON)}		V _{GS} =2.5V , I _D =1.5A		60	75	
		V _{GS} =1.8V , I _D =1A		70	90	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250uA$	0.3	0.85	1.2	V
$\triangle V_{GS(th)}$	V _{GS(th)} Temperature Coefficient	V _{GS} -V _{DS} , I _D -2500A		-2.51		mV/℃
	Drain Source Leakage Current	V _{DS} =16V , V _{GS} =0V , T _J =25℃			1	
I _{DSS}	Drain-Source Leakage Current	V_{DS} =16V , V_{GS} =0V , T_J =55 $^{\circ}$ C			5	uA
I _{GSS}	Gate-Source Leakage Current	V_{GS} = $\pm 8V$, V_{DS} = $0V$			±100	nA
gfs	Forward Transconductance	V_{DS} =5V , I_D =3A		8.3		S
R_g	Gate Resistance	V _{DS} =0V , V _{GS} =0V , f=1MHz		1.7	3.4	Ω
Qg	Total Gate Charge (4.5V)			6.4		
Q_{gs}	Gate-Source Charge	V _{DS} =15V , V _{GS} =4.5V , I _D =1A		0.54		nC
Q_gd	Gate-Drain Charge			1.25		1
$T_{d(on)}$	Turn-On Delay Time	V_{DD} =10V , V_{GS} =4.5V , R_{G} =3.3 Ω		1.6		
Tr	Rise Time			29.6		
T _{d(off)}	Turn-Off Delay Time			18.8		ns
T _f	Fall Time			6		
Ciss	Input Capacitance	V _{DS} =15V , V _{GS} =0V , f=1MHz		382		
C _{oss}	Output Capacitance			41		pF
C _{rss}	Reverse Transfer Capacitance			33		

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V =V =0V Force Current			4.3	Α
I _{SM}	Pulsed Source Current ^{2,4}	$V_G=V_D=0V$, Force Current			12	Α
V_{SD}	Diode Forward Voltage ²	V_{GS} =0 V , I_{S} =1 A , T_{J} =25 $^{\circ}$ \mathbb{C}			1.2	V
t _{rr}	Reverse Recovery Time			5.5		nS
Qrr	Reverse Recovery Charge	lF=2A,dI/dt=100A/μs,T _J =25℃		1.8		nC

Note:

- 1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper ,t<10sec.
- 2.The data tested by pulsed , pulse width $\,\leq\,$ 300us , duty cycle $\,\leq\,$ 2%
- 3.The power dissipation is limited by 150 $^{\circ}\mathrm{C}$ junction temperature
- 4. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.



Typical Characteristics

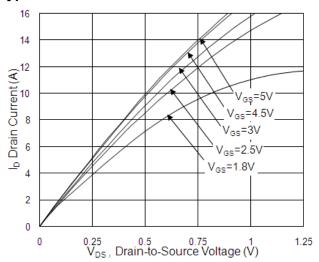


Fig.1 Typical Output Characteristics

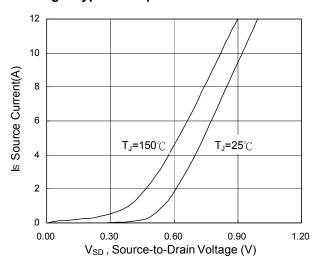


Fig.3 Forward Characteristics Of Reverse

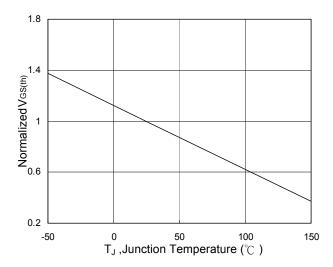


Fig.5 Normalized V_{GS(th)} vs. T_J

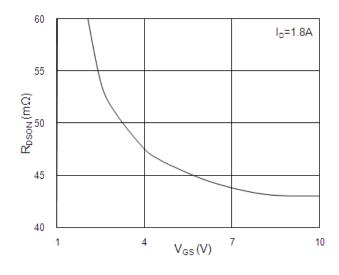


Fig.2 On-Resistance vs. Gate-Source

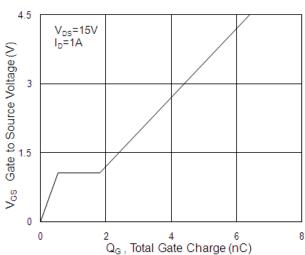


Fig.4 Gate-Charge Characteristics

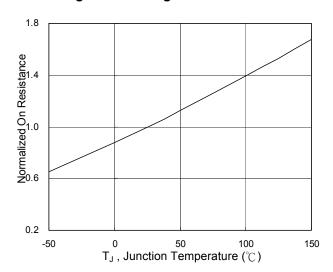
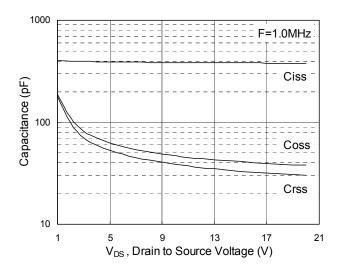


Fig.6 Normalized R_{DSON} vs. T_J





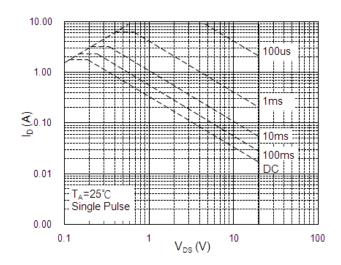


Fig.7 Capacitance

Fig.8 Safe Operating Area

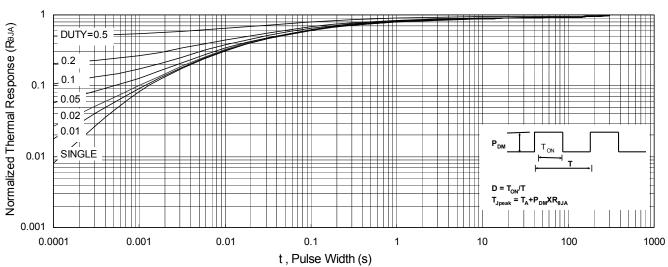


Fig.9 Normalized Maximum Transient Thermal Impedance

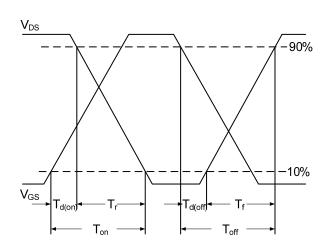


Fig.10 Switching Time Waveform

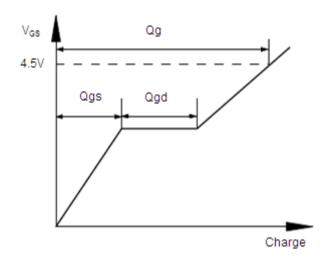


Fig.11 Gate Charge Waveform



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