Description

The F2950 is a high power, reflective 50Ω, single-pole double-throw (SP2T) RF switch. This device covers a 100MHz to 8GHz frequency range to support a wide variety of applications including WLAN 802.11.

The F2950 uses a single positive supply voltage and is compatible with both 1.8V and 3.3V control logic.

Competitive Advantage

The F2950 provides extremely low insertion loss across a very broad bandwidth while providing high linearity performance across its operating range.

- Optimized for Wi-Fi applications
- Wide bandwidth
- Low insertion loss
- Excellent linearity
- High power handling for large peak-to-average applications
- Fast switching
- No external matching required
- Minimal footprint

Typical Applications

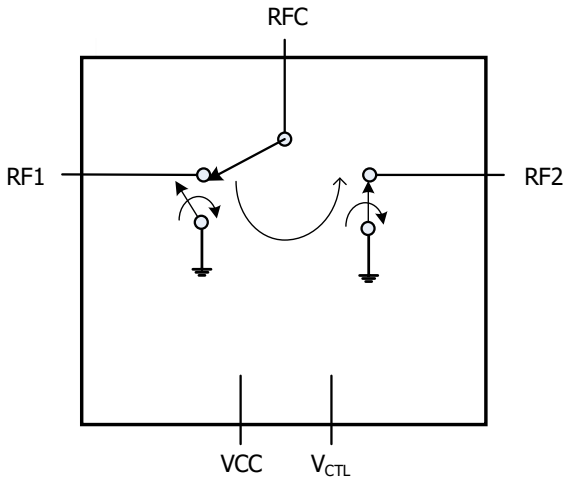
- 802.11 Wi-Fi
- Wireless Access Points, Gateways and Router Applications
- LTE and 4G Communication Systems
- 2-Way Radios
- General Purpose

Features

- Low insertion loss: 0.58dB at 2.5GHz
- High isolation: 44dB at 2.5GHz
- Excellent linearity:
  - IIP3 +69dBm at 2.4GHz and 5.9GHz
  - IIP2 +115dBm at 2.4GHz
  - IIP2 +117dBm at 5.9GHz
- Second Harmonic: -93dBc at 5.9GHz
- Third Harmonic: -85dBc at 5.9GHz
- Typical switching speed: 170ns
- Supply voltage: +2.7V to +5.5V
- 1.8V and 3.3V compatible control logic
- -40°C to +105°C operating temperature range
- 1.5mm x 1.5mm, 6-pin DFN package

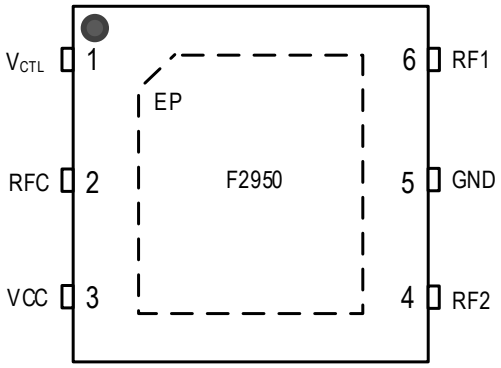
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 1.5mm x 1.5mm x 0.55mm DFN, NEG6 – Top View



Pin Descriptions

Table 1. Pin Descriptions

Pin	Name	Function
1	V_{CTL}	Logic control pin. See Table 7 for logic control states.
2	RFC	RF common port. Matched to 50Ω in the insertion loss state only. If this pin is not 0V DC, then an external coupling capacitor must be used.
3	V_{CC}	Power supply. Bypass to GND with capacitors as close as possible to the pin.
4	RF2	RF2 port. Matched to 50Ω in the insertion loss state only. If this pin is not 0V DC, then an external coupling capacitor must be used.
5	GND	Ground. Ground this pin as close to the device as possible.
6	RF1	RF1 port. Matched to 50Ω in the insertion loss state only. If this pin is not 0V DC, then an external coupling capacitor must be used.
	EP	Exposed pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Symbol	Minimum	Maximum	Units
V_{CC} to GND		V_{CC}	-0.3	+6.0	V
V_{CTL} to GND		V_{LOGIC}	-0.3	Lower of (V_{CC} + 0.3, 3.9)	V
RF1, RF2, RFC to GND		V_{RF}	-0.3	+0.3	V
Maximum Input CW Power, $Z_S = Z_L = 50\Omega$, $T_{EP} = 25°C$, $V_{CC} = 5.25V$ (any port, insertion loss state) [a]	100MHz ≤ f_{RF} ≤ 200MHz	P_{ABSCW1}		28	dBm
	200MHz < f_{RF} ≤ 500MHz	P_{ABSCW2}		29	
	500MHz < f_{RF} ≤ 1GHz	P_{ABSCW3}		30	
	1GHz < f_{RF} ≤ 6GHz	P_{ABSCW4}		31	
	f_{RF} > 6GHz	P_{ABSCW5}		30	
Maximum Peak Power, $Z_S = Z_L = 50\Omega$, $T_{EP} = 25°C$, $V_{CC} = 5.25V$ (any port, insertion loss state) [a], [b]	100MHz ≤ f_{RF} ≤ 200MHz	P_{ABSPK1}		35	dBm
	200MHz < f_{RF} ≤ 500MHz	P_{ABSPK2}		36	
	500MHz < f_{RF} ≤ 1GHz	P_{ABSPK3}		37	
	1GHz < f_{RF} ≤ 6GHz	P_{ABSPK4}		38	
	f_{RF} > 6GHz	P_{ABSPK5}		37	
Maximum Junction Temperature		T_{JMAX}		+140	°C
Storage Temperature Range		T_{STOR}	-65	+150	°C
Lead Temperature (soldering, 10s)		T_{LEAD}		+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)		V_{ESDHBM}		2000 (Class C2)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)		V_{ESDCDM}		500 (Class C2)	V

[a] T_{EP} is the temperature of the exposed paddle.

[b] 5% duty cycle of 4.6ms period in a 50Ω environment.

Recommended Operating Conditions

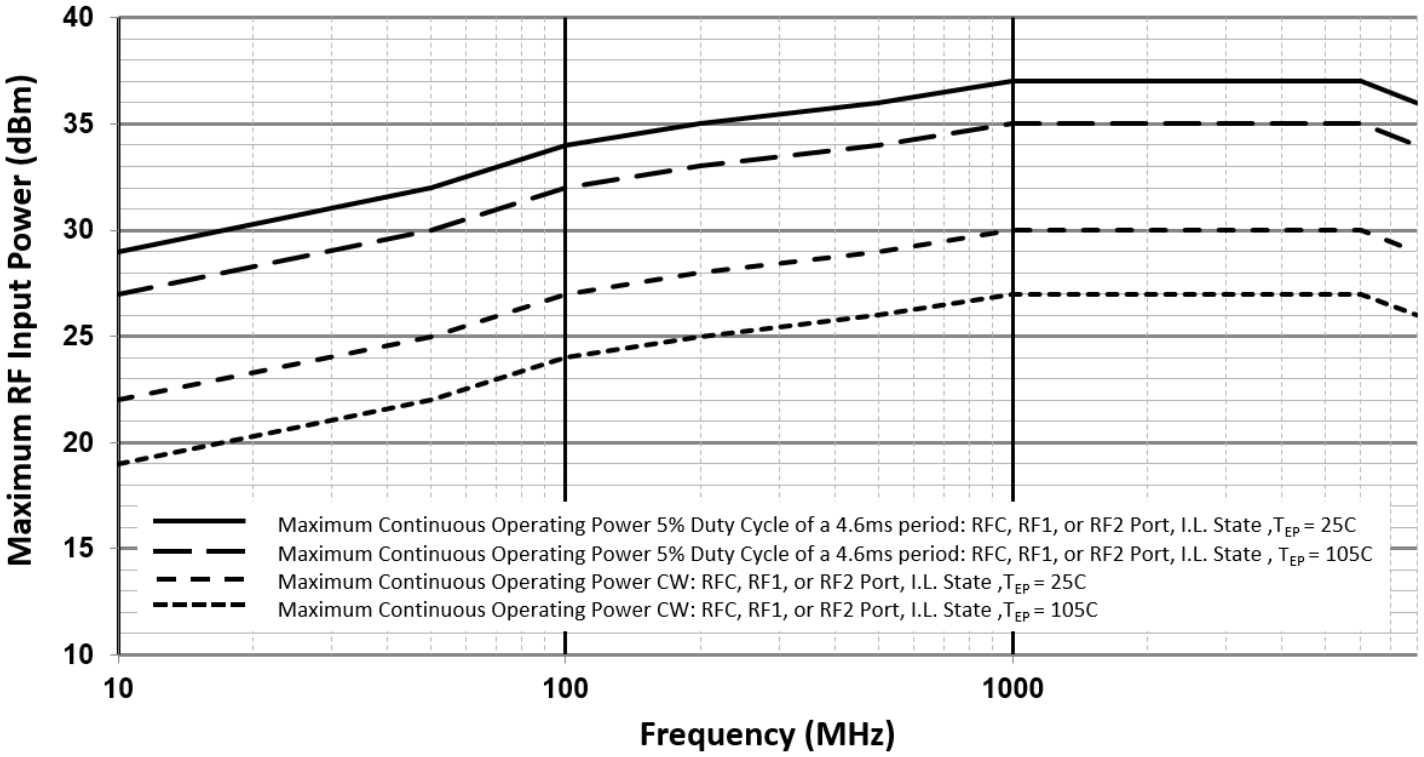
Table 3. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply Voltage	V_{CC}		2.7 [a]	3.3	5.5	V
Operating Temperature Range	T_{EP}	Exposed paddle	-40	+25	+105	°C
RF Frequency Range	f_{RF}		0.1		8	GHz
RF Input Power [b]	P_{RF_CW}	CW, insertion loss state	See Figure 3			dBm
	P_{RF_PULSE}	5% duty cycle of 4.6ms period, insertion loss state	See Figure 3			
RFC, RF1, RF2 Port Impedance	Z_{RF}			50		Ω

[a] Functional with reduced performance for $2.3V \le V_{CC} < 2.7V$.

[b] Levels based on: V_{CC} = 2.7V to 5.5V, $100MHz \le f_{RF} \le 8GHz$, $Z_S = Z_L = 50\Omega$. See Figure 3 for power handling derating vs. RF frequency.

Figure 3. Maximum RF Input Operating Power vs. RF Frequency ($Z_S = Z_L = 50\Omega$)



Electrical Characteristics

Table 4. Electrical Characteristics

See F2950 Typical Application Circuit. Specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C, P_{IN} = 0dBm, Z_S = Z_L = 50Ω, single tone and two tone signals applied at RF1 or RF2 and measured at RFC when in the ON state, PCB board trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Logic Input High Threshold	V_{IH}	V_{CTL} pin	1.1 [b]		Lower of (V_{CC}, 3.6)	V
Logic Input Low Threshold	V_{IL}	V_{CTL} pin	-0.3		0.6	V
Logic Current	I_{IH}, I_{IL}	V_{CTL} pin	***-1***		***+1***	µA
DC Current	I_{CC}			170	***250*** [a]	µA
Insertion Loss (RF1 or RF2 to RFC)	IL	f_{RF} = 100MHz to 900MHz		0.54	0.74	dB
		f_{RF} = 900MHz to 2500MHz [c]		0.58	***0.79***	
		f_{RF} = 2500MHz to 3700MHz		0.61	0.83	
		f_{RF} = 3700MHz to 4900MHz		0.64	0.88	
		f_{RF} = 4900MHz to 6000MHz		0.67	0.90	
		f_{RF} = 6000MHz to 8000MHz		0.73		
Isolation (RF1 or RF2 to RFC)	ISO1	f_{RF} = 100MHz to 900MHz	48	53		dB
		f_{RF} = 900MHz to 2500MHz	39	44		
		f_{RF} = 2500MHz to 3700MHz	35	40		
		f_{RF} = 3700MHz to 4900MHz	32	37		
		f_{RF} = 4900MHz to 6000MHz		34		
		f_{RF} = 6000MHz to 8000MHz		31		
Isolation (RF1 to RF2, RF2 to RF1)	ISO2	f_{RF} = 100MHz to 900MHz	50	54		dB
		f_{RF} = 900MHz to 2500MHz	40	44		
		f_{RF} = 2500MHz to 3700MHz	35	40		
		f_{RF} = 3700MHz to 4900MHz	32	37		
		f_{RF} = 4900MHz to 6000MHz		34		
		f_{RF} = 6000MHz to 8000MHz		30		
Return Loss (RFC, RF1, RF2)	RL	f_{RF} = 100MHz to 900MHz		25		dB
		f_{RF} = 900MHz to 2500MHz		23		
		f_{RF} = 2500MHz to 3700MHz		22		
		f_{RF} = 3700MHz to 4900MHz		21		
		f_{RF} = 4900MHz to 6000MHz		20		
		f_{RF} = 6000MHz to 8000MHz		20		

[a] Items in min/max columns in ***bold italics*** are guaranteed by test.
[b] Items in min/max columns that are not bold italics are guaranteed by design characterization.
[c] Minimum or maximum specification guaranteed by test at 2.5GHz and by design characterization over the whole frequency range.

Electrical Characteristics

Table 5. Electrical Characteristics

See F2950 Typical Application Circuit. Specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C, P_{IN} = 0dBm, Z_S = Z_L = 50Ω, single tone and two tone signals applied at RF1 or RF2 and measured at RFC when in the ON state, PCB board trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input IP3	IIP3	f_{RF} = 2.4GHz at P_{IN} = +24dBm/tone 100MHz tone spacing			69		dBm
		f_{RF} = 5.9GHz at P_{IN} = +24dBm/tone 100MHz tone spacing			69		
Input IP2	IIP2	f_1 = 700MHz, f_2 = 1.7GHz P_{IN} = +24dBm/tone Measure 2.4GHz product			115		dBm
		f_1 = 2.4GHz, f_2 = 3.5GHz P_{IN} = +24dBm/tone Measure 5.9GHz product			117		
Second Harmonic	H2	f_{RF} = 2.4GHz, P_{IN} = +30dBm Measure 4.8GHz product			104		dBc
		f_{RF} = 5.9GHz, P_{IN} = +30dBm Measure 11.8GHz product			93		
Third Harmonic	H3	f_{RF} = 2.4GHz, P_{IN} = +30dBm Measure 7.2GHz product			85		dBc
		f_{RF} = 5.9GHz, P_{IN} = +30dBm Measure 17.7GHz product			85		
Input 1dB compression [c]	P1dB	f_{RF} = 2.4GHz			40		dBm
		f_{RF} = 6GHz			40		
		f_{RF} = 8GHz			39		
Spurious Output [d]	Pspur1	f_{OUT} > 5MHz All ports terminated, RBW = 100Hz			-97		dBm
	Pspur2	f_{OUT} ≤ 5MHz All ports terminated, RBW = 100Hz			-125		
Maximum Video Feed-Through on RF Ports	VID_{FT}	Peak transient during switching. Measured with 20ns rise time, 0V to 3.3V (3.3V to 0V) control pulse applied to V_{CTL}.	Rise		10		mVpp
			Fall		21		
Switching Time [e]	SW_{TIME}	50% V_{CTL} to 90% RF			170	230	ns
		50% V_{CTL} to 10% RF			170	230	
		50% V_{CTL} to 99% RF			190	270	
		50% V_{CTL} to 1% RF			190	270	
Maximum Switching Rate	SW_{RATE}				125		kHz

[a] Items in min/max columns in ***bold italics*** are guaranteed by test.
[b] Items in min/max columns that are not bold italics are guaranteed by design characterization.
[c] The input 1dB compression point is a linearity figure of merit. Refer to the “Absolute Maximum Ratings” section and Figure 3 for the maximum RF input power.
[d] Spurious due to on-chip negative voltage generator. Spurious fundamental is approximately 5.7MHz.
[e] f_{RF} = 1GHz. Rise and fall time of V_{CTL} = 20ns.

Thermal Characteristics

Table 6. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	θ_{JA}	200	°C/W
Junction to Case Thermal Resistance (Case is defined as the exposed paddle)	θ_{JC_BOT}	132	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOCs)

Unless otherwise noted:

- V_{CC} = +3.3V
- T_{EP} = 25°C
- $Z_S = Z_L$ = 50Ω
- f_{RF} = 1GHz
- Small signal tests done at 0dBm input power
- All temperatures are referenced to the exposed paddle
- Evaluation Kit traces and connector losses are de-embedded

Typical Performance Characteristics [1]

Figure 4. RF1 to RFC Insertion Loss vs. Frequency across Temperature

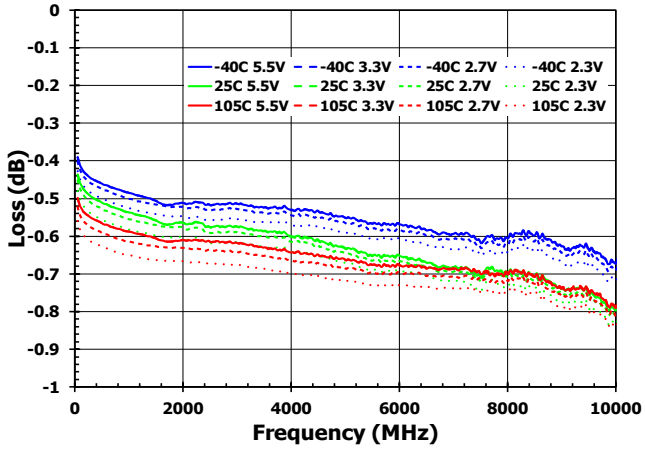


Figure 5. RF2 to RFC Insertion Loss vs. Frequency across Temperature

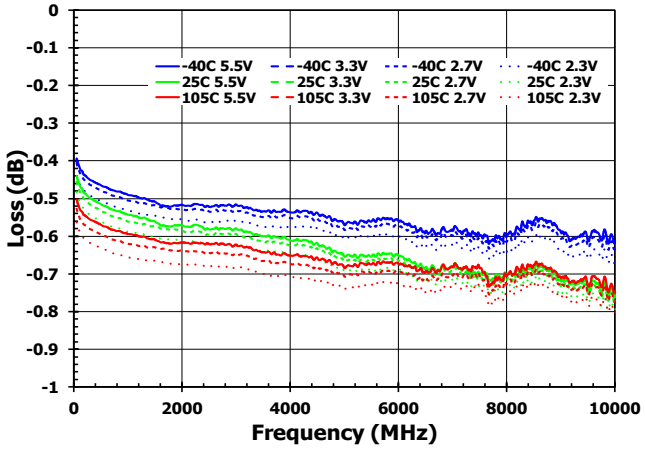


Figure 6. RF1 to RFC Isolation vs. Frequency across Temperature

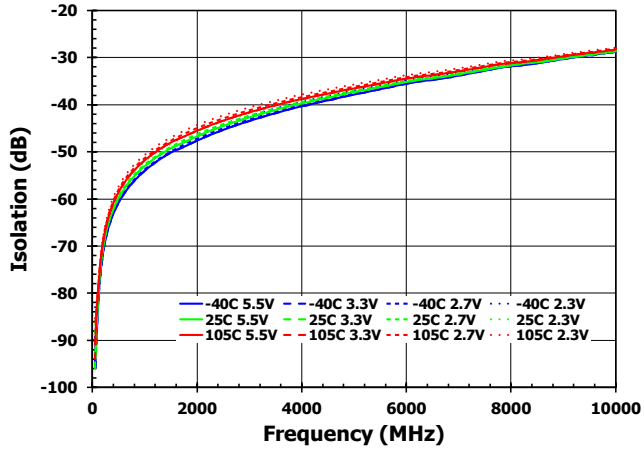


Figure 7. RF2 to RFC Isolation vs. Frequency across Temperature

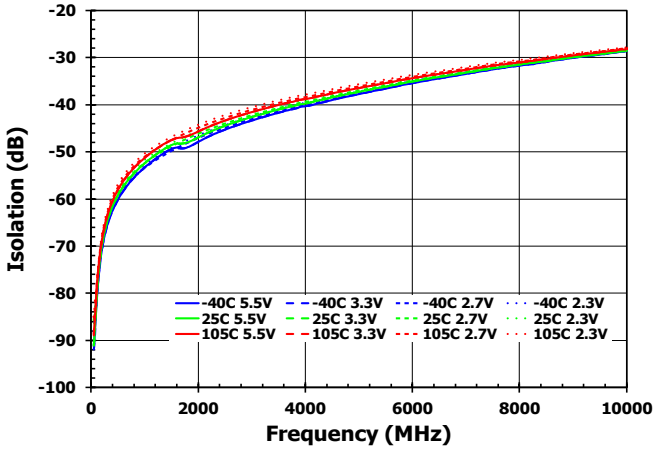


Figure 8. RF1 to RF2 Isolation vs. Frequency across Temperature [RF1 Selected]

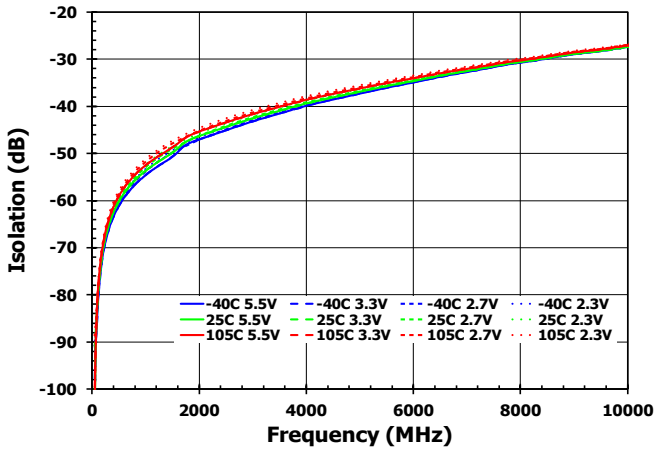
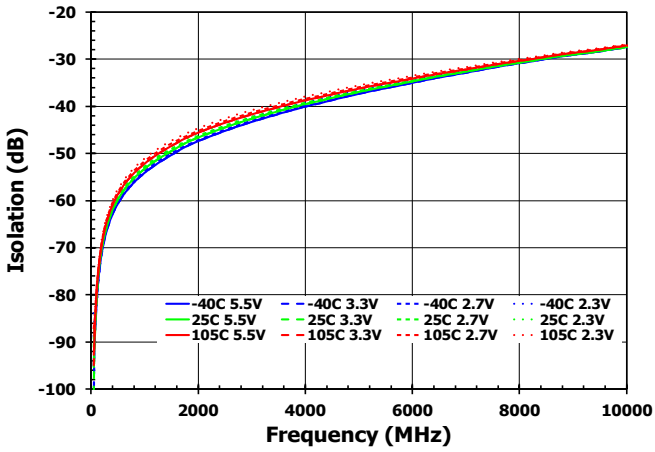


Figure 9. RF2 to RF1 Isolation vs. Frequency across Temperature [RF2 Selected]



Typical Performance Characteristics [2]

Figure 10. RF1 Return Loss vs. Frequency across Temperature [RF1 Selected]

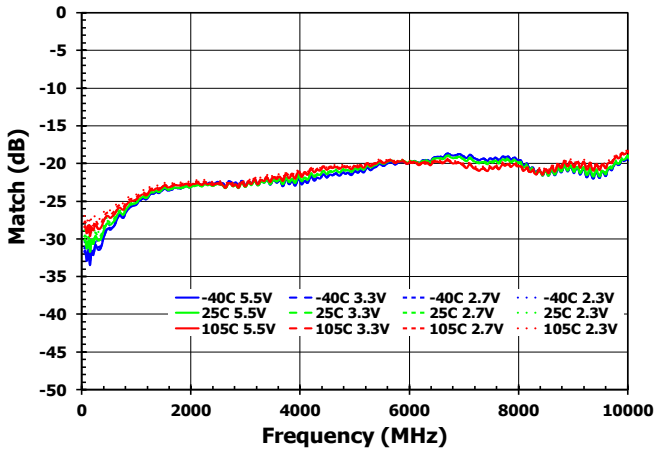


Figure 11. RF2 Return Loss vs. Frequency across Temperature [RF2 Selected]

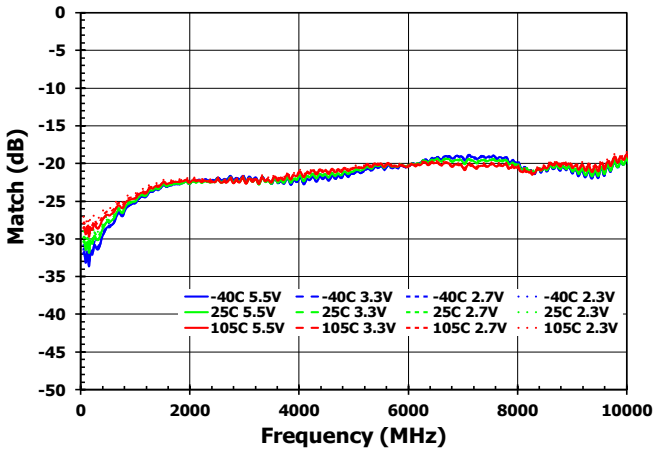


Figure 12. RFC Return Loss vs. Frequency across Temperature [RF1 Selected]

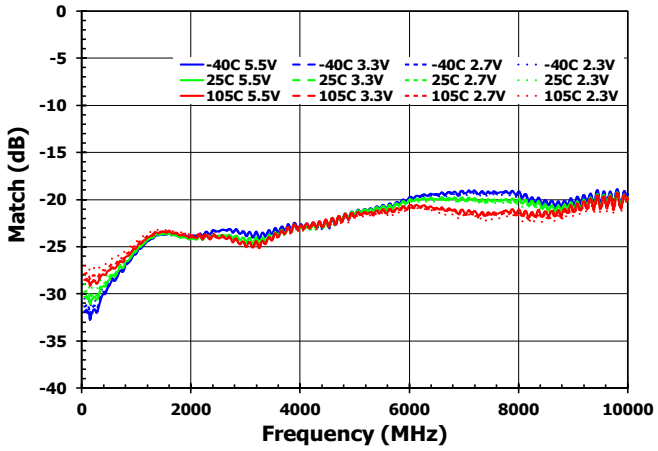


Figure 13. RFC Return Loss vs. Frequency across Temperature [RF2 Selected]

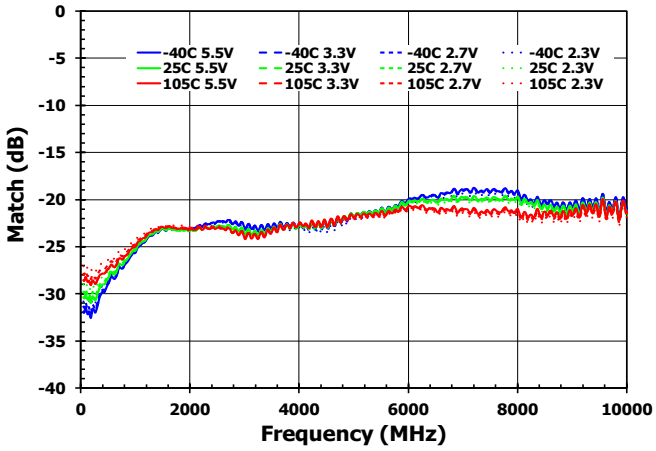
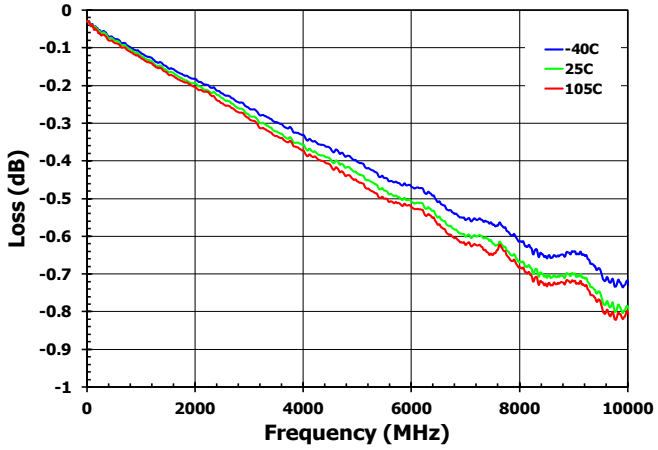


Figure 14. EVKit PCB and Connector Thru Loss vs. Frequency across Temperature



Typical Performance Characteristics [3]

Figure 15. Switching Time Isolation to Insertion Loss State

Figure 16. Switching Time Insertion Loss to Isolation State

Control Mode

Table 7. Switch Control Truth Table

V_{CTL}	RFC to RF1	RFC to RF2
LOW	OFF	ON
HIGH	ON	OFF

Application Information

Default Start-up

The V_{CTL} control pin includes no internal pull-down resistors to logic LOW or pull-up resistors to logic HIGH.

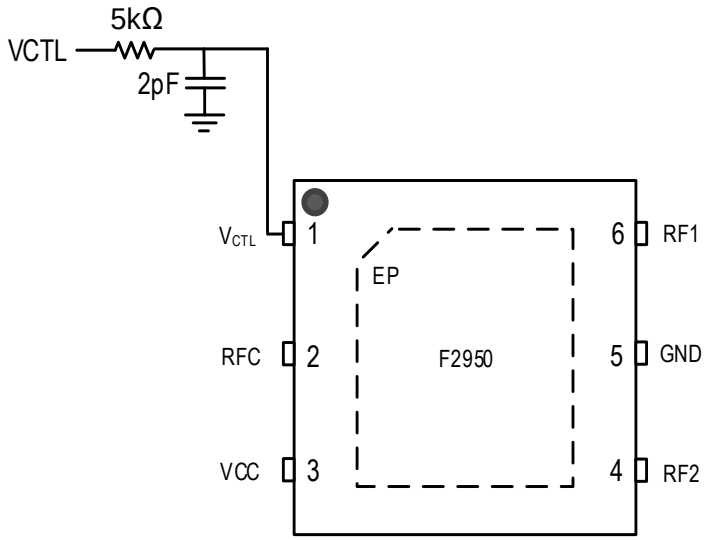
Power Supplies

A common V_{CC} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate slower than 1V / 20µs. In addition, all control pins should remain at 0V (± 0.3V) while the supply voltage ramps up or while it returns to zero.

Control Pin Interface

If a clean control signal cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of the control pin is recommended.

Figure 17. Control Pin Signal Integrity Improvement Circuit



Evaluation Kit Picture

Figure 18. Top View

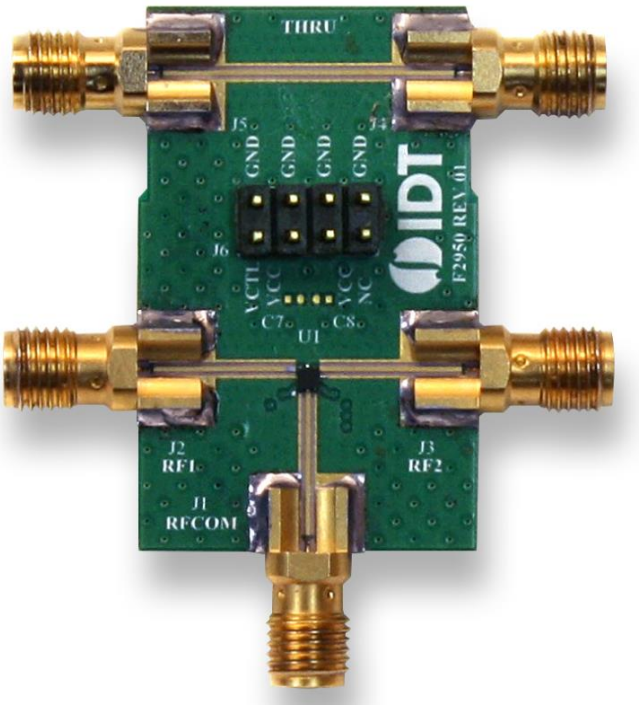
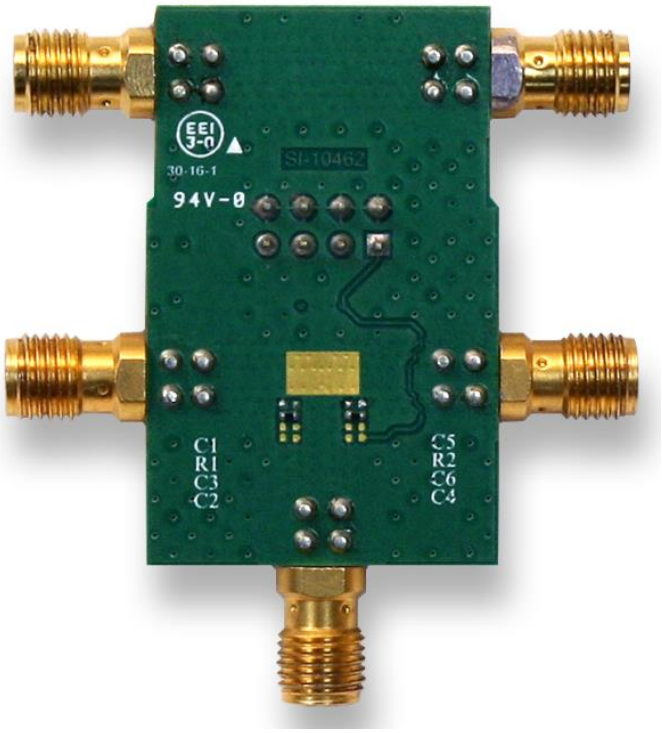


Figure 19. Bottom View



Evaluation Kit / Applications Circuit

Figure 20. Electrical Schematic

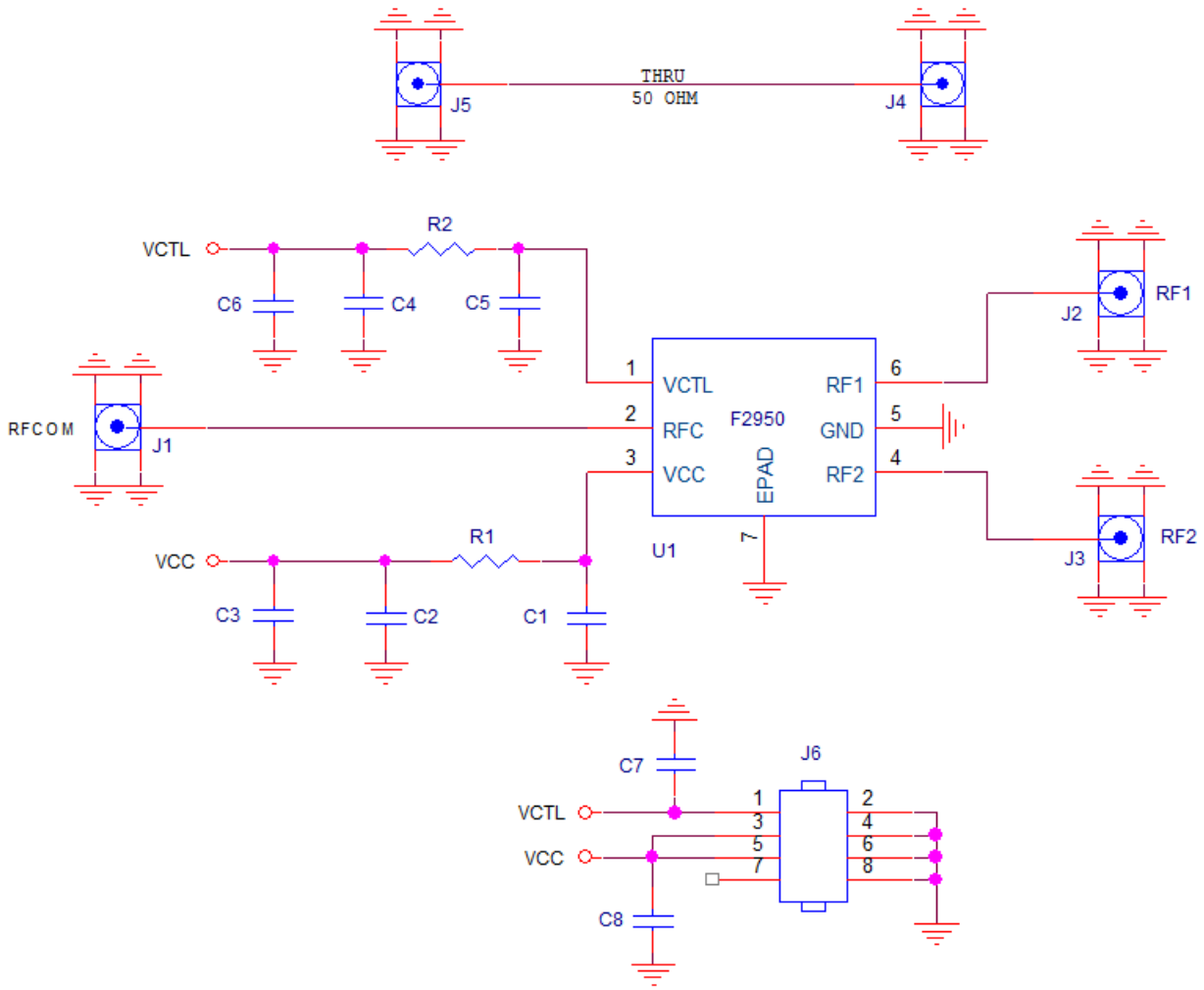


Table 8. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1	1	0.1µF ±10%, 16V, X7R, Ceramic Capacitor (0402)	GRM155R71C104K	Murata
C2 – C8	0	Not Installed (0402)		
R1, R2	2	0Ω, 1/10W, Jumper (0402)	ERJ-2GE0R00X	Panasonic
J1 – J5	5	50Ω Edge SMA Connector	142-0761-881	Cinch Connectivity
J6	1	Conn Header Vert 4x2 Pos Gold	67997-108HLF	Amphenol FCI
U1	1	SP2T Switch 1.5mm x 1.5mm 6-pin NEG6 DFN	F2950NEGK6	IDT
	1	Printed Circuit Board	F2950 EVKit	IDT

Evaluation Kit (EVKit) Operation

External Supply Setup

Set up a V_{CC} power supply in the voltage range of 2.7V to 5.5V with the power supply output disabled.

Connect the disabled V_{CC} supply connection to J6 pin 3 or 5 and GND to J6 pin 2, 4, 6, or 8.

Logic Control Setup

With the logic control line disabled, set the logic HIGH and LOW levels to satisfy the levels stated in the electrical specifications table.

Connect the disabled logic control line to VCTL (pin 1 of J6) and GND to J6 pin 2, 4, 6, or 8.

Turn On Procedure

Set up the supplies and EVKit as noted in the “External Supply Setup” and “Logic Control Setup” sections above.

Enable the V_{CC} supply.

Enable the logic control signal.

Set the VCTL logic setting to achieve the desired Table 7 configuration. Note that the VCTL control logic should not be applied without V_{CC} being present.

Enable any RF signal.

Turn Off Procedure

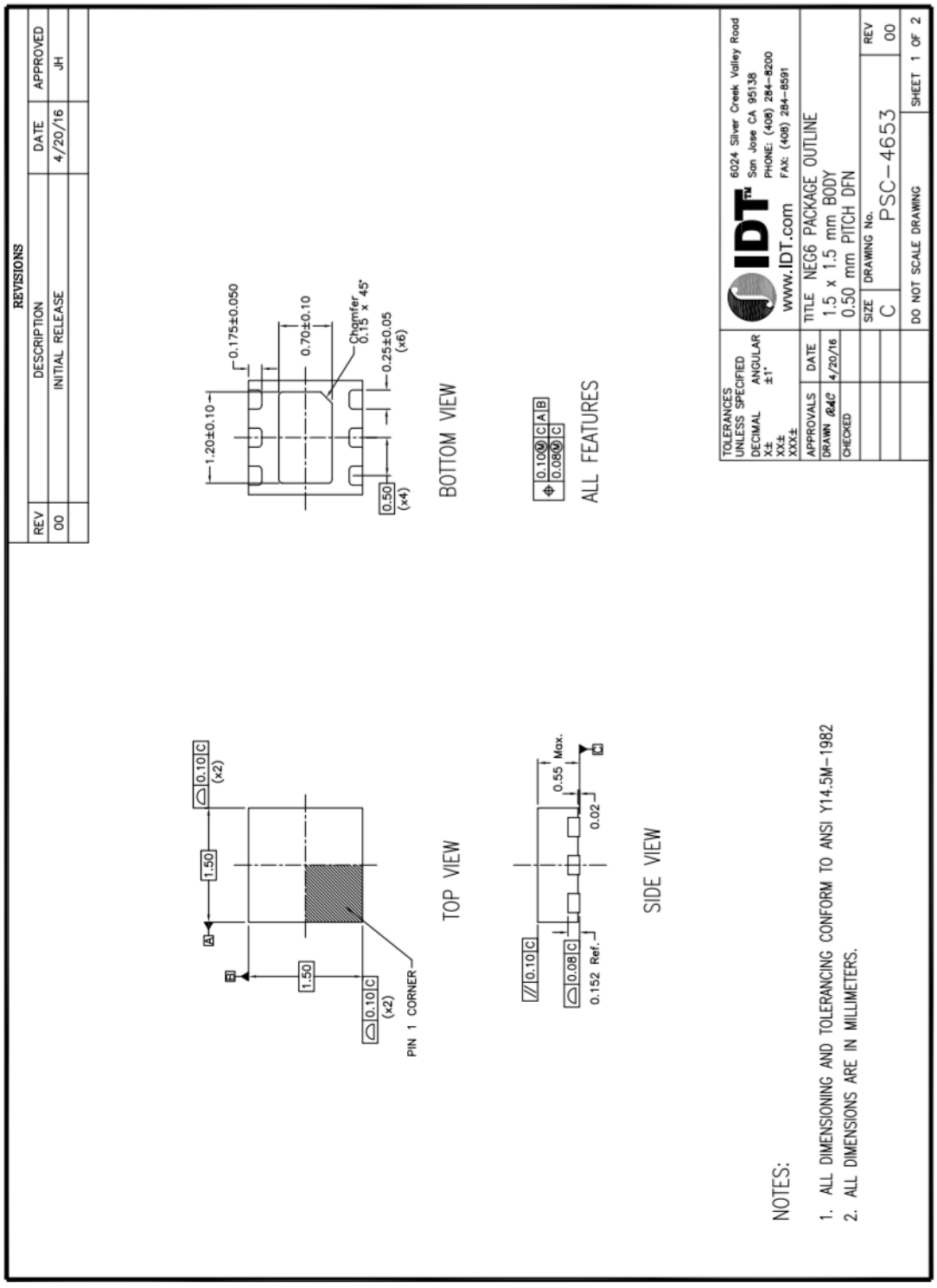
Disable any applied RF signal.

Set VCTL to GND.

Disable the V_{CC} supply.

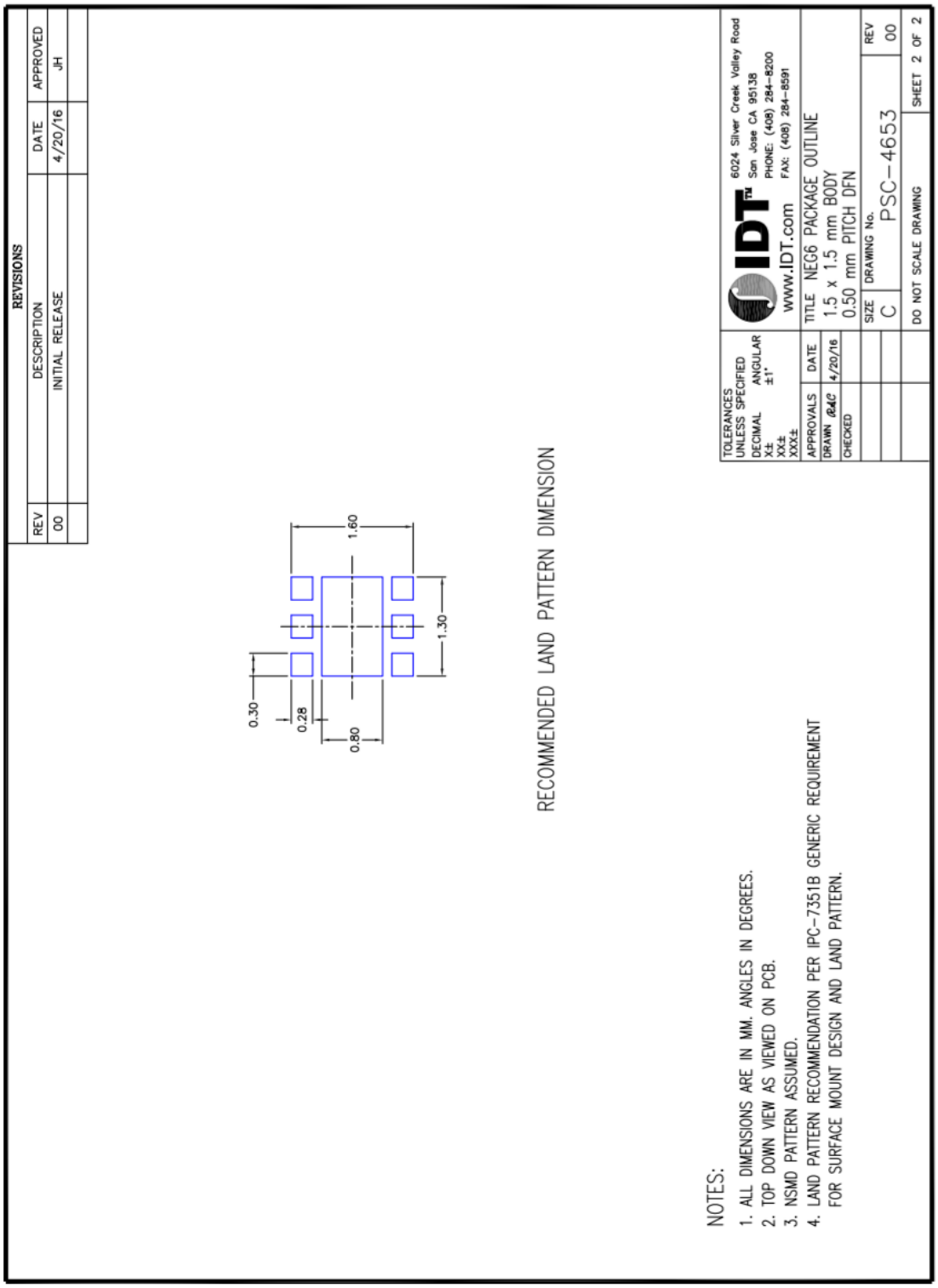
Package Drawings

Figure 21. Package Outline Drawing – NEG6 Package

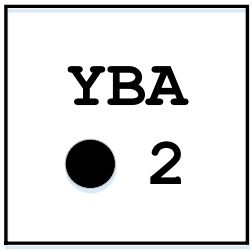


Recommended Land Pattern

Figure 22. Recommended Land Pattern – NEG6 Package



Marking Diagram



1. Line 1: Y = last digit of the year, BA = sequential letters for traceability purposes
2. Line 2: Pin 1 dot, 2 = F2950 part number code

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F2950NEGK	1.5mm x 1.5mm x 0.55mm NEG6 DFN	MSL1	Cut Tape	-40°C to +105°C
F2950NEGK8	1.5mm x 1.5mm x 0.55mm NEG6 DFN	MSL1	Reel	-40°C to +105°C
F2950EVBI	Evaluation Board			

Revision History

Revision	Revision Date	Description of Change
Rev O	August 8, 2017	Initial Release

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