

Vishay Siliconix

CMOS Analog Switches

DESCRIPTION

The DG304B, DG306B and DG307B monolithic CMOS switches were designed for applications in communications, instrumentation and process control. This series is well suited for applications requiring fast switching and nearly flat on-resistance over the entire analog range.

Designed on the Vishay Siliconix PLUS-40 CMOS process to achieve low power consumption and excellent on/off switch performance, these switches are ideal for battery powered applications, without sacrificing switching speed.

Break-before-make switching action is guaranteed, and an epitaxial layer prevents latchup. Single supply operation (for positive switch voltages) is allowed by connecting the V- rail to 0 V.

Each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. These switches are CMOS input compatible.

FEATURES

- ± 15 V input range
- Fast switching t_{ON}: 110 ns
- Low R_{DS(on)}: 30 Ω
- · Single supply operation
- CMOS logic levels
- Micropower: 30 nW

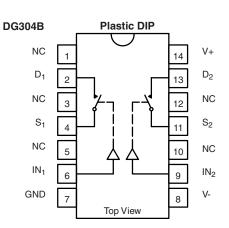
BENEFITS

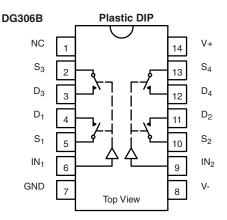
- Full rail-to-rail analog signal range
- Low signal error
- Wide dynamic range
- · Low power dissipation

APPLICATIONS

- Low level switching circuits
- Programmable gain amplifiers
- · Portable and battery powered systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION





TRUTH TABLE				
Logic	Switch			
0	OFF			
1	ON			

 $\begin{array}{l} \text{Logic "0"} \leq 3.5 \text{ V} \\ \text{Logic "1"} \geq 11 \text{ V} \end{array}$

TRUTH TABLE	
Logic	Switch
0	OFF
1	ON

 $\begin{array}{l} \text{Logic "0"} \leq 3.5 \ \text{V} \\ \text{Logic "1"} \geq 11 \ \text{V} \end{array}$

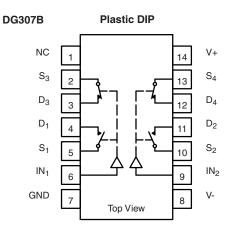
* Pb containing terminations are not RoHS compliant, exemptions may apply.



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FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Four SPST switches per package

TRUTH TABLE				
Logic	SW ₁ , SW ₂	SW ₃ , SW ₄		
0	OFF	ON		
1	ON	OFF		

Logic "0" ≤ 3.5 V

Logic "1" ≥ 11 V

ORDERING INFORMATION				
Temp. Range	Package	Standard Part Number	Lead (Pb)-free Part Number	
- 40 °C to 85 °C		DG304BDJ	DG304BDJ-E3	
	14-Pin Plastic DIP	DG306BDJ	DG306BDJ-E3	
		DG307BDJ	DG307BDJ-E3	

ABSOLUTE MAXIM	UM RATINGS (T _A = 25 °C, unless o	therwise noted)		
Parameter		Limit	Unit	
Voltages Referenced V+ to V-		44		
GND		25	V	
Digital Inputs ^a , V _S , V _D		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first		
Current (Any Terminal)		30	mA	
Continuous Current, S or D (Pulsed at 1 ms, 10 % duty cycle max.)		100		
Storage Temperature		- 65 to 150	°C	
Power Dissipation ^b	14-Pin Plastic DIP ^c	470	mW	

Notes:

a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC board.

c. Derate 11 mW/°C above 25 °C.



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SPECIFICATIONS ^a								
		Test Conditions Unless Otherwise Specified V+ = 15 V, V- = - 15 V			Limits - 40 °C to 85 °C			
Parameter	Symbol	V _{IN} = 3.5 V or	11 V ^f	Temp. ^b	Min. ^d	Typ. ^c	Max. ^d	Unit
Analog Switch	<u> </u>			•	•	•	•	
Analog Signal Range ^e	V _{ANALOG}			Full	- 15		15	V
Drain-Source On-Resistance	R _{DS(on)}	$V_D = \pm 10$ V, $I_S =$	= 10 mA	Room Full		30	50 75	Ω
Source Off Leakage Current	I _{S(off)}	$V_{s} = \pm 14 V, V_{D}$	= + 14 V	Room Full	- 5 - 100	± 0.1	5 100	
Drain Off Leakage Current	I _{D(off)}	······································		Room Full	- 5 - 100	± 0.1	5 100	nA
Drain On Leakage Current	I _{D(on)}	$V_D = V_S = \pm T$	14 V	Room Full	- 5 - 200	± 0.1	5 200	
Digital Control								
Input Current with	I _{INH} –	V _{IN} = 5 V	,	Room Full	- 1	- 0.001		
Input Voltage High	INH	V _{IN} = 15 V		Room Full		0.001	1	μΑ
Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0 V	,	Room Full	- 1	- 0.001		
Dynamic Characteristics								
Turn-On Time	t _{ON}	see figure	2	Room		110		
Turn-Off Time	t _{OFF}	0		Room		70		ns
Break-Before-Make Time	t _{OPEN}	DG305A/307A ONLY,		Room		50		
Charge Injection	Q	$C_L = 1 \text{ nF, } R_{gen} = 0 \Omega$ see figure	5	Room		30		рC
Source-Off Capacitance	C _{S(off)}			Room		14		
Drain-Off Capacitance	C _{D(off)}	$V_{S}, V_{D} = 0 V, f =$	1 MHz	Room		14		
Channel-On Capacitance	C _{D(on)}			Room		40		pF
Input Capacitance	C _{IN}	$f = 1 \text{ MHz} \qquad \frac{V_{IN} = 0 \text{ V}}{V_{IN} = 15 \text{ V}}$		Room		6		
input Capacitance	CIN			Room		7		
Off-Isolation	OIRR	$V_{IN} = 0 V, R_L = 1 k\Omega$		Room		62		dB
Crosstalk (Channel-to-Channel)	X _{TALK}	$V_{S} = 1 V_{rms}$, f = 500 kHz		Room		74		
Power Supplies				_				
Positive Supply Current	l+	V _{IN} = 15 V or 0 V		Room Full		0.001	100	μA
Negative Supply Current	l-	(all inputs)		Room Full	- 100	- 0.001		ри/

Notes:

a. Refer to PROCESS OPTION FLOWCHART.

b. Room = 25 $^{\circ}$ C, Full = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

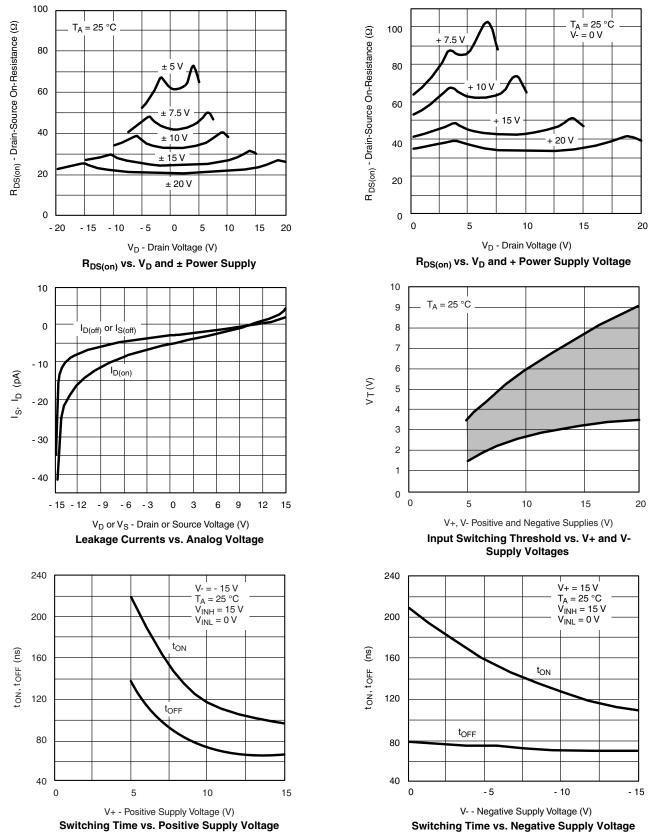
e. Guaranteed by design, not subject to production test.

f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

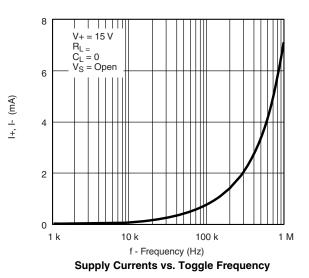




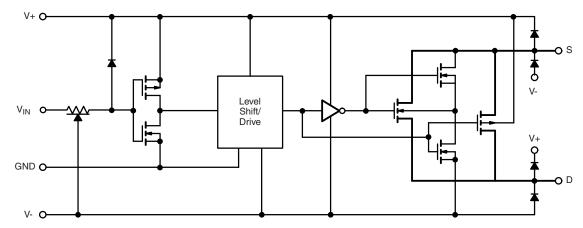


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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

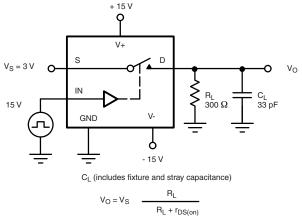


SCHEMATIC DIAGRAM (Typical Channel)





TEST CIRCUITS



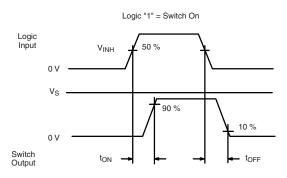
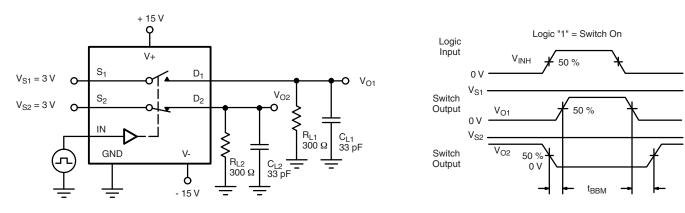


Figure 2. Switching Time

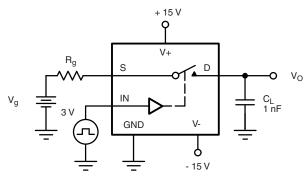
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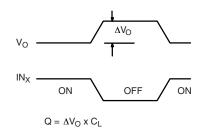
TEST CIRCUITS



C_L (includes fixture and stray capacitance)

Figure 3. Break-Before-Make SPDT (DG307B)







APPLICATIONS HINTS ^a					
V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND Voltage (V)	V _{IN} Logic Input Voltage V _{INH(min)} /V _{INL(max)} (V)	V _S or V _D Analog Voltage Range (V)	
15	- 15	0	11/3.5	- 15 to 15	
20	- 20	0	11/3.5	- 20 to 20	
15	0	0	11/3.5	0 to 15	

Notes:

a. Application hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.





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APPLICATIONS

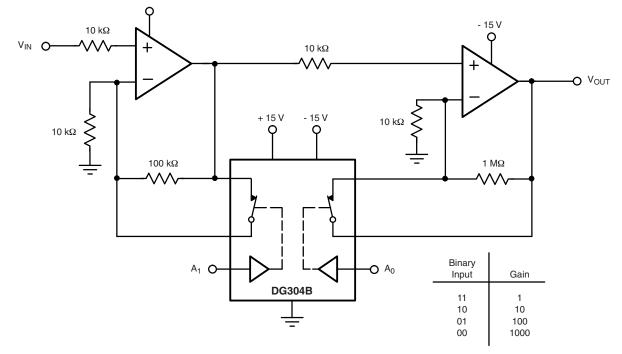


Figure 5. Low Power Binary to 10ⁿ Gain Low Frequency Amplifier

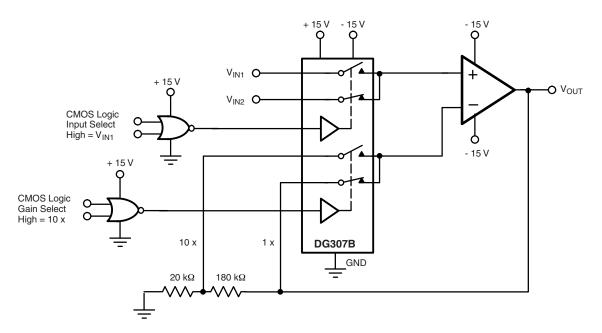
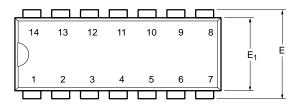


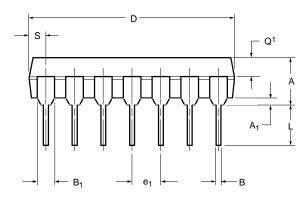
Figure 6. Low Power Instrumentation Amplifier with Digitally Selectable Inputs and Gain

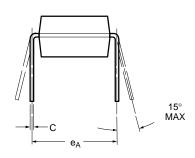
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <u>www.vishay.com/ppg?71403</u>.



PDIP: 14-LEAD







	MILLIMETERS		INC	HES
Dim	Min	Max	Min	Max
Α	3.81	5.08	0.150	0.200
A ₁	0.38	1.27	0.015	0.050
В	0.38	0.51	0.015	0.020
B ₁	0.89	1.65	0.035	0.065
С	0.20	0.30	0.008	0.012
D	17.27	19.30	0.680	0.760
Е	7.62	8.26	0.300	0.325
E ₁	5.59	7.11	0.220	0.280
e ₁	2.29	2.79	0.090	0.110
e _A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q 1	1.27	2.03	0.050	0.080
S	1.02	2.03	0.040	0.080
ECN: S-0 DWG: 54	3946—Rev. (181	C, 09-Jul-01	•	



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