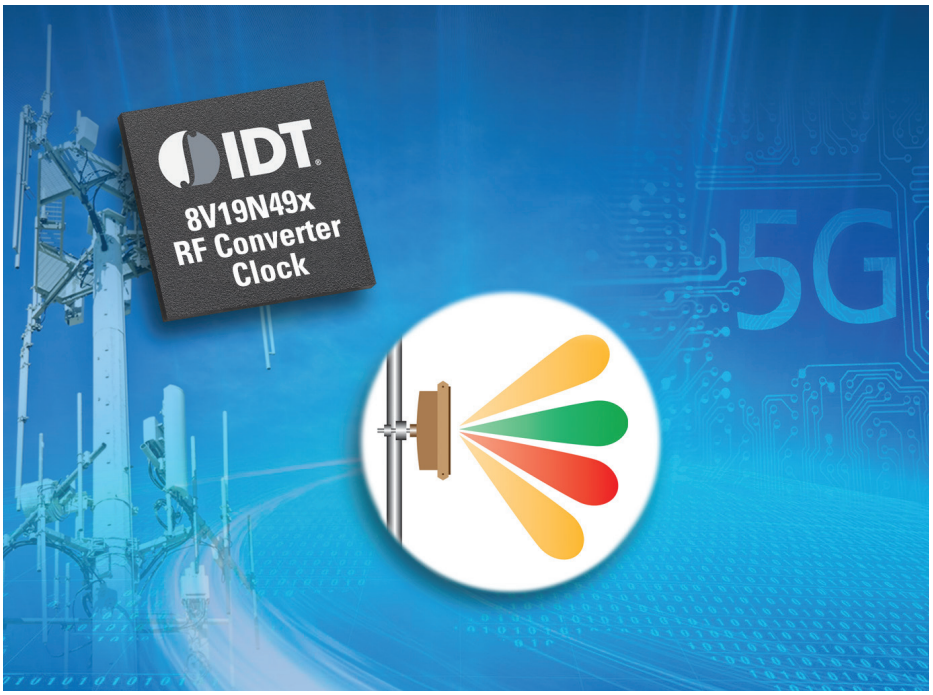
8V19N49x RF Sampling Clocks with Jitter Attenuation

FEATURES AND BENEFITS

- Supports RF DAC sampling clocks
  – 2.94912GHz
  – 2.4576GHz
  – 1.96608GHz
  – 3.6864GHz
  – 3.93216GHz
- Optimized for low Error Vector Magnitude (EVM) radio designs
- Single chip solution for 4T4T to 16T16R
- Ideal for synchronous clock / SYSREF generation in AAS and MIMO
- JESD204B subclass 0 / 1 converter synchronization
- High fanout options reduce clock buffer component count
- Cascaded operation and very-low output skew temperature drift for MIMO and beamforming applications
- Deterministic phase relationship and alignment
- Low integrated phase noise < 80fs RMS (12 kHz to 20 MHz)
- High spurious attenuation of 90dBc
- Four inputs and short-term holdover for redundancy / system operation protection
- Single 3.3V supply

TYPICAL APPLICATIONS

- Wireless infrastructure radio
- Reference clock for high-speed, high-performance DAC / ADC
- JESD204B synchronization
- Instrumentation
- CPRI



High Frequency, Low Phase Noise, High Spurious Attenuation, ADC / DAC Reference Clock

The 8V19N49x FemtoClock® NG family of RF sampling clock generators with jitter attenuation supports 5G New Radio (NR) designs for wireless base station radio equipment boards. The devices are optimized to deliver excellent phase noise and spurious performance for radio board implementations. The 8V19N49x family provides very-low phase skew drift in temperature, reducing radio path recalibration occurrences in beamforming applications.

These devices generate up to five clock frequencies from an internal VCO(s) distributed to up to 18 low-skew differential outputs. An integrated pulse generator provides JESD204B-compliant SYSREF synchronization signals. The outputs support symmetrical 100Ω (LVDS type) and LVPECL 50Ω termination, with a configurable amplitude up to 2000mV differential.

Integrated phase delay circuits enable clock / SYSREF phase adjustments to meet stringent receiver hold / setup time requirements, achieving zero device delay and board trace length compensation.

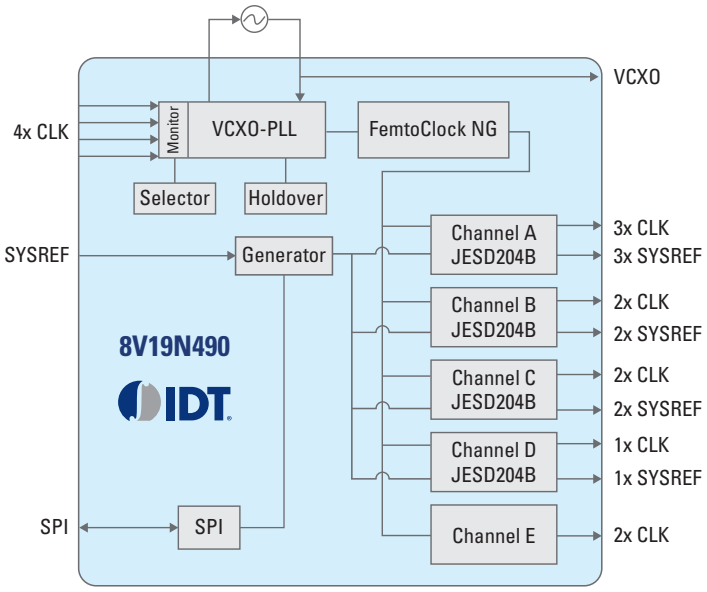
RF Sampling Clocks with Jitter Attenuation

PERFORMANCE

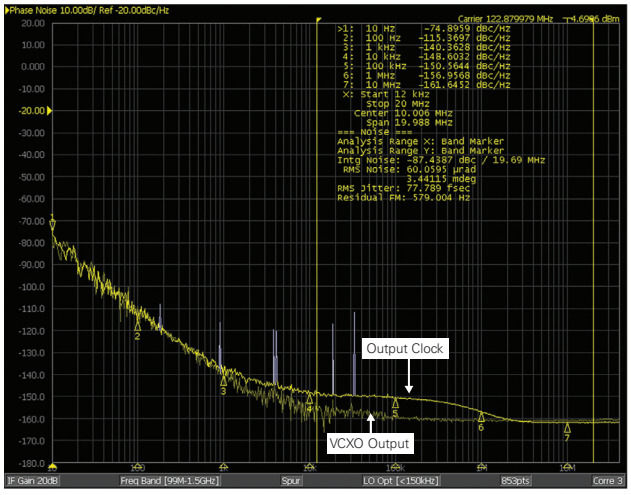
- Typical –153dBc / Hz phase noise (800kHz offset, 245.76MHz clock)
- Maximum –150dBc / Hz phase noise (800kHz offset, 245.76MHz clock)
- Maximum –85dBc Spurious (<100MHz offset, 245.76MHz clock)

CONFIGURATION OPTIONS

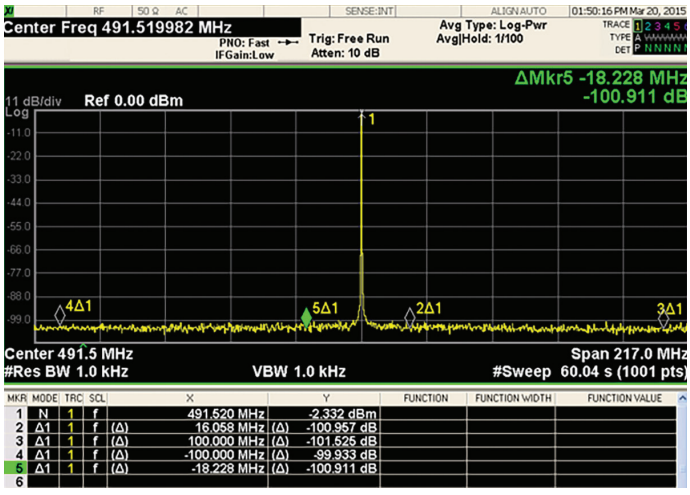
- Input and output frequency
- Auto / manual input selection
- Output amplitude
- Output termination style (LVDS / LVPECL)
- AC and DC output coupling for pulsed SYSREF
- Output delay position (absolute and relative to other outputs)
- 3-wire SPI
- Power-down features



Phase Noise Generation – 122.88MHz Clock Output 78fs RMS (12 kHz to 20 MHz)



Spurious Attenuation – 491.52MHz Clock Output: 99dBc



To request samples, download documentation or learn more visit: **idt.com/RFConverterClock**