Description

The F0452B is an integrated dual-path RF front-end consisting of an RF switch and two gain stages with 6dB gain control used in the analog front-end receiver of an Active Antenna System (AAS). The F0452B supports frequencies from 2.3GHz to 2.7GHz.

The F0452B provides 34dB gain with +23dBm OIP3, +15dBm output P1dB, and 1.5dB noise figure (NF) at 2.6GHz. Gain is reduced 6dB in a single step with a maximum settling time of 31ns. The device uses a single 3.3V supply and 130mA of I_{DD}.

The F0452B is offered in a 5 × 5 × 0.8 mm, 32-LGA package with 50Ω input and output amplifier impedances for ease of integration into the signal path.

Competitive Advantage

- High integration
- Low noise and high linearity
- On-chip matching and bias
- Extremely low current consumption

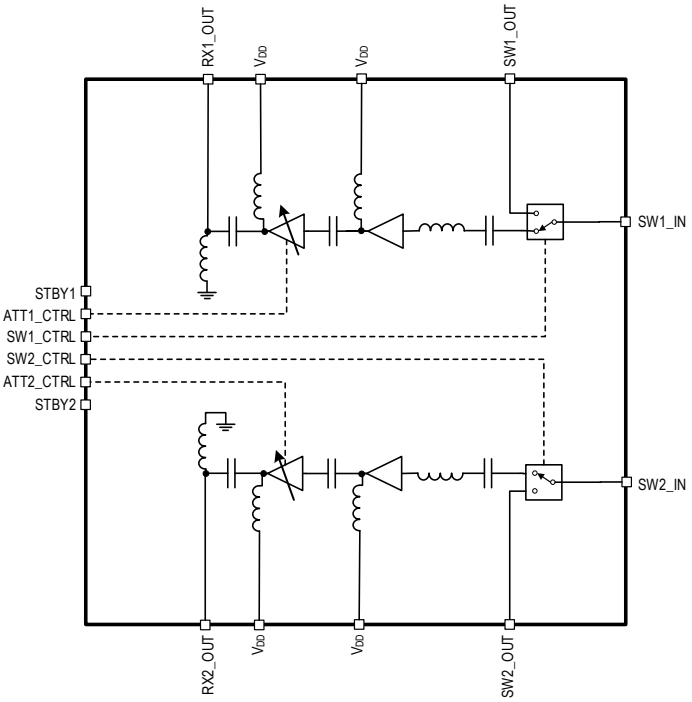
Typical Applications

- Multi-mode, multi-carrier receivers
- 4.5G (LTE Advanced)
- 5G band 42

Features

- Gain at 2.6GHz
  - 34dB typical in High Gain Mode
  - 28dB typical in Low Gain Mode
- 1.5dB NF at 2.6GHz
- +23dBm OIP3 at 2.6GHz
- OP1dB at 2.6GHz
  - +15dBm in High Gain Mode
  - +14dBm in Low Gain Mode
- 50Ω single-ended input / output amplifier impedances
- I_{DD} = 130mA
- Independent Standby Mode for power savings
- Supply voltage: +3.15V to +3.45V
- 5 × 5 mm, 32-LGA package
- -40°C to +105°C exposed pad operating temperature range

Block Diagram



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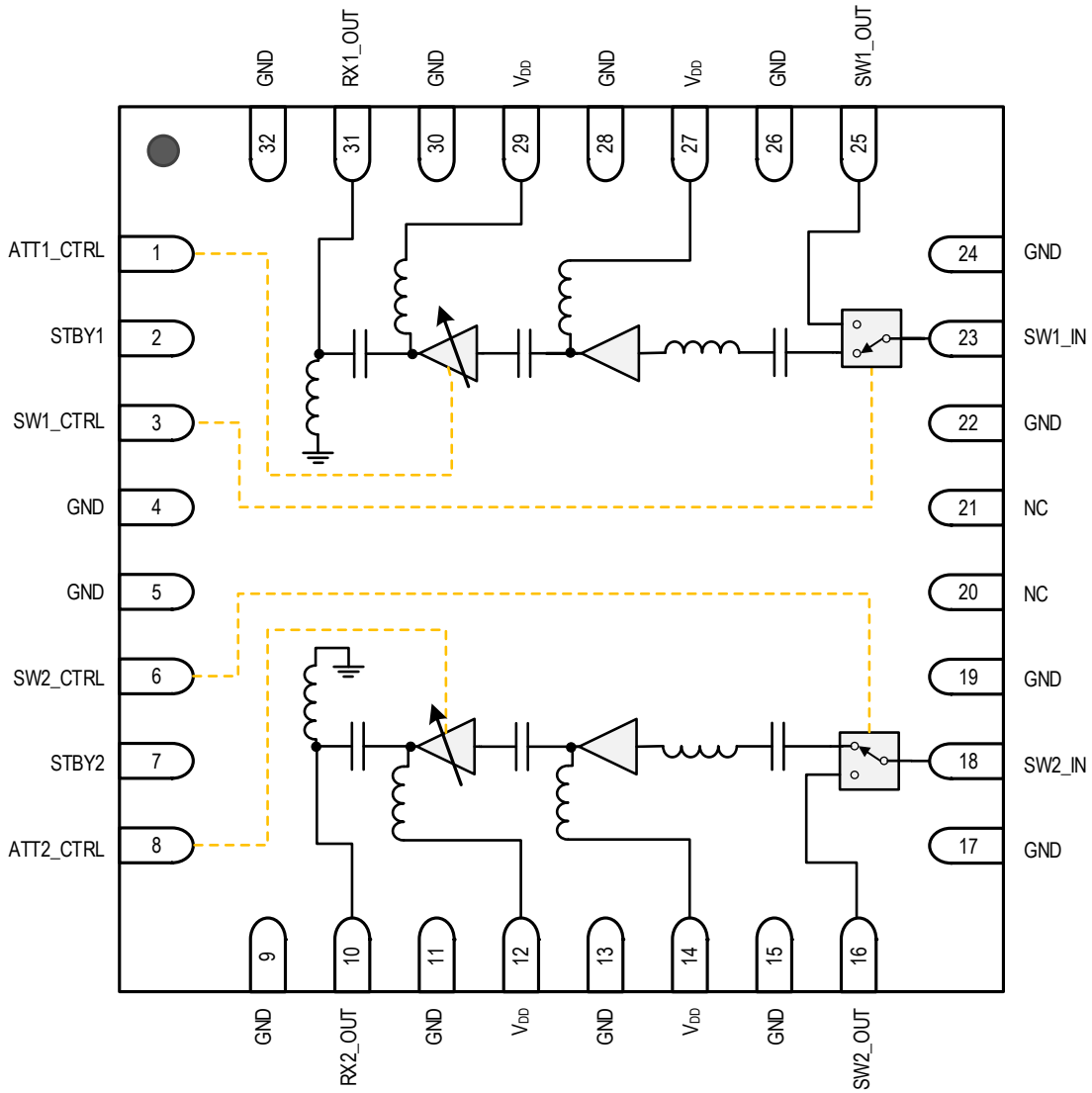
Pin Assignments

Figure 1. Pin Assignments for 5 × 5 × 0.8 mm 32-LGA – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1	ATT1_CTRL	1-bit 6dB gain control for path 1. (LOW/open = no attenuation; HIGH = 6dB attenuation). A 500kΩ pull-down resistor is connected between this input and GND.
2	STBY1	Standby (LOW/open = path 1 power ON; HIGH = path 1 power OFF). A 500kΩ pull-down resistor is connected between this input and GND.
3	SW1_CTRL	RF SWITCH 1 control (LOW/open = select main RX PATH 1; HIGH = switch output). SW1_CTRL also puts path 1 into Standby Mode for minimum current consumption. A 500kΩ pull-down resistor is connected between this input and GND.
4, 5, 9, 11, 13, 15, 17, 19, 22, 24, 26, 28, 30, 32	GND	Ground these pins.
6	SW2_CTRL	RF SWITCH 2 control (LOW/open = select main RX PATH 2; HIGH = switch output). SW2_CTRL also puts path 2 into Standby Mode for minimum current consumption. A 500kΩ pull-down resistor is connected between this input and GND.
7	STBY2	Standby (LOW/open = path 2 power ON; HIGH = path 2 power OFF). A 500kΩ pull-down resistor is connected between this input and GND.
8	ATT2_CTRL	1-bit 6dB gain control for path 2. (LOW/open = no attenuation; HIGH = 6dB attenuation). A 500kΩ pull-down resistor connects between this input and GND.
10	RX2_OUT	RF output path 2 matched to 50Ω. Use external DC block as close to the pin as possible.
12, 14, 27, 29	VDD	Power supply. Bypass to GND with capacitors shown in the F0452B Application Circuit (see Figure 30) as close as possible to the pins.
16	SW2_OUT	RF2 switch output matched to 50Ω. Use external 50Ω terminating resistor with proper power rating as required for the application.
18	SW2_IN	RF2 switch input matched to 50Ω. Use an external DC block as close to the pin as possible.
23	SW1_IN	RF1 switch input matched to 50Ω. Use an external DC block as close to the pin as possible.
25	SW1_OUT	RF1 switch output matched to 50Ω. Use an external 50Ω terminating resistor with proper power rating as required for the application.
31	RX1_OUT	RF output path 1 matched to 50Ω. Use an external DC block as close to the pin as possible.
20, 21	NC	Not internally connected.
	— EPAD	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the specified RF performance.

Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
V_{DD} to GND	V_{DD}	-0.3	+3.6	V
STBY1, STBY2, ATT1_CTRL, ATT2_CTRL, SW1_CTRL, SW2_CTRL to GND	V_{CTRL}	-0.3	V_{DD} + 0.25	V
SW1_IN, SW2_IN, RX1_OUT, RX2_OUT, SW1_OUT, SW2_OUT to GND Externally Applied DC Voltage	V_{SW}	-50	50	mV
TX Mode CW Average Input Power +7.5dB PAR at SW1_IN, SW2_IN Ports, 10s, 89% Duty Cycle 50Ω, T_{EPAD} = 105°C [a], V_{DD} = +3.3V	P_{ABS_TX}	+31	+33 [b]	dBm
RX Mode Average Input Power +7.5dB PAR at SW1_IN, SW2_IN Ports, 1 Hour Single Event, 50% Duty Cycle 50Ω, T_{EPAD} = 105°C [a], V_{DD} = +3.3V	P_{ABS_RX}		+8	dBm
Storage Temperature Range	T_{ST}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}		+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		1500 (Class 1C)	V
Electrostatic Discharge – CDM (JEDEC JS-002-2014) ALL pins except pins 16, 18, 23, 25	V_{ESDCDM}		500 (Class C2A)	V
Electrostatic Discharge – CDM (JEDEC JS-002-2014) Pins 16, 18, 23, 25	V_{ESDCDM}		125 (Class C0B)	V

[a] T_{EPAD} = Temperature of the exposed paddle.

[b] RF input exposures greater than +31dBm and up to +33dBm for multiple extended periods will affect device reliability and lifetime if the maximum recommended input junction temperature is exceeded.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

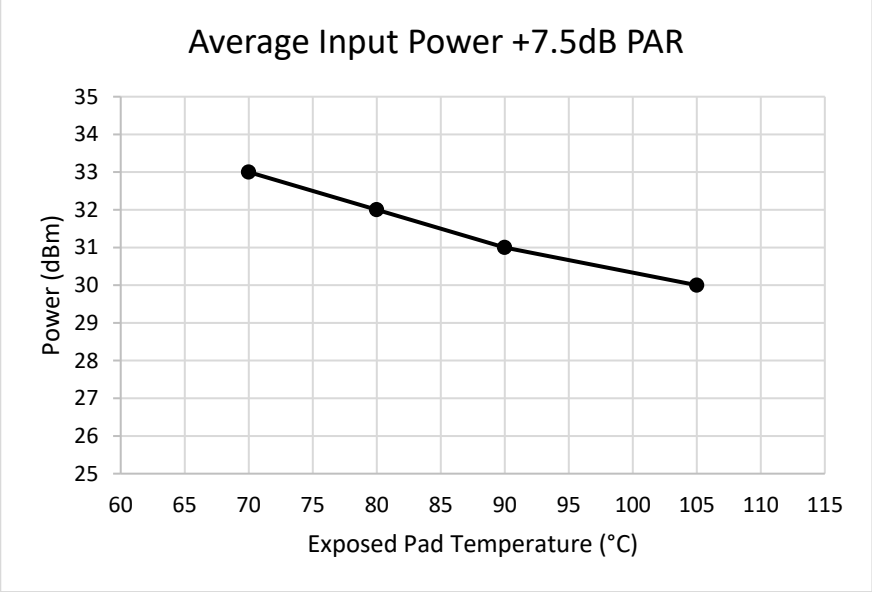
Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Power Supply Voltage	V_{DD}		3.15	3.3	3.45	V
Operating Temperature Range	T_{EPAD}	Exposed Paddle	-40		+105	°C
RF Frequency Range	f_{RF}		2.3		2.7	GHz
TX Mode CW Average Input Power, +7.5dB PAR, Full Life Time [a] 50Ω, V_{DD} = +3.3V	P_{MAX_TX}	89% Duty Cycle			+30[b]	dBm
RX Mode CW Average Input Power, +7.5dB PAR, Full Life Time [a] 50Ω, V_{DD} = +3.3V	P_{MAX_RX}	89% Duty Cycle			-25	dBm
Port Impedance (SW1_IN, SW2_IN, RX1_OUT, RX2_OUT)	Z_{RF}			50		Ω
Junction Temperature	T_J				+125	°C

[a] Assumes device environmental temperature cycling within the specified exposed pad operating temperature range of -40°C and 105°C and a maximum junction temperature of 125°C.

[b] Operation beyond the maximum recommended operating input power level should be limited and have reduced exposed pad temperatures to maintain device reliability per foundry guidelines (see Figure 2). Electrical characteristics and lifetime are not guaranteed for RF input power levels beyond what is specified in this table.

Figure 2. Typical TX Input Power and Reduced Exposed Pad Temperature Profile

Note: This graph estimates the maximum input power without exceeding the maximum junction temperature of 125°C using an IDT-specific evaluation board and test environment.



Electrical Characteristics

Table 4. Electrical Characteristics

See F0452B Application Circuit in Figure 30. Specifications apply when operated as an RX RF amplifier with V_{DD} = +3.3V, T_{EPAD} = +25°C, STBYx = LOW, RX output power = -10dBm, $Z_S = Z_L$ = 50Ω, and EVKit trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold	V_{IH}		***1.17***[a]		Lower of (V_{DD}, 3.3)	V
Logic Input Low Threshold	V_{IL}		-0.3		***0.63***	V
Logic Current	I_{IH}, I_{IL}	For each control pin	***-10***		***10***	µA
DC Current	I_{DD}	2 paths in RX Mode		130	***180***	mA
		1 path in RX Mode 1 path in TX Mode		70	***100***	
		1 path in RX Mode 1 path in Standby Mode		67		
		1 path in TX Mode 1 path in Standby Mode		5		
		2 paths in Standby Mode		5		
Gain Step	G_{STEP}			6		dB
Gain Step Absolute Error	G_{STEP_ERR}	Relative to maximum gain, over-voltage, and temperature		±0.5		dB
Relative Phase Gain Step	G_{STEP_PH}			28		deg
Gain Step Settling Time [b]	G_{STEP_SET}	50% control logic to RF output within ±0.1dB of final value		20	31	ns
Gain Step Phase Settling Time [b]	G_{STEP_PHSET}	50% control logic to RF output within ±1 degree of final value		16	30	ns
Power ON Switching Time [b]	SW_{ON}	To RX Mode from TX Mode 50% control logic to RF output settled to within ±0.1dB of final value			1	µs
Power OFF Switching Time [b]	SW_{OFF}	To TX Mode from RX Mode 50% control logic to RF input settled within ±0.1dB of final value			0.5	µs

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Power ON from Standby Mode [b]	$SW_{ON\_STANDBY}$	To RX Mode from Standby Mode 50% STBYx to RF output settled within ±0.1dB of final value			1	µs
Power OFF to Standby Mode [b]	$SW_{OFF\_STANDBY}$	To Standby Mode from RX Mode 50% STBYx to gain below -25dB from maximum gain			1	µs

[a] Items in the "Minimum"/"Maximum" columns in ***bold italics*** are guaranteed by test. Items in the "Minimum"/"Maximum" columns not in bold italics are guaranteed by design characterization.

[b] f_{RF} = 2.6GHz. Assumes the control signal is clean and no external RC circuitry is required on the pin. Adding RC circuitry increases switching time. Timing tests performed with a control logic signal of +3.3V and a rise/fall time ≤ 30ns.

Table 5. Electrical Characteristics: RX Path in RX Mode Cascaded Performance

See the F0452B Application Circuit in Figure 30. Specifications apply when operated as an RX RF amplifier with V_{DD} = +3.3V, f_{RF} = 2.6GHz, T_{EPAD} = +25°C, STBYx = LOW, RX output power = -10dBm, Z_S = Z_L = 50Ω, and EVKit trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Input Return Loss	RL_{IN}	Measured at SW1_IN, SW2_IN, High/Low Gain Mode, f_{RF} = 2.4GHz		12 [a]		dB
		Measured at SW1_IN, SW2_IN, High/Low Gain Mode, f_{RF} = 2.6GHz		20		
		Measured at SW1_IN, SW2_IN, High/Low Gain Mode, f_{RF} = 2.3GHz to 2.7GHz	6			
Output Return Loss	RL_{OUT}	Measured at RX1_OUT, RX2_OUT, High/Low Gain Modes, f_{RF} = 2.3GHz to 2.7GHz	7			dB
Reverse Isolation, RX1_OUT to SW1_IN, or RX2_OUT to SW2_IN	ISO_{REV}	f_{RF} = 2.3GHz to 2.7GHz	50	58		dB
Gain	G_{HG}	High Gain Mode	***32***	34	***37***	dB
	G_{HG_TEMP}	T_{EPAD} = -40°C to 105°C	31		38	
Gain Attenuated	G_{LG}	Low Gain Mode	25.5	28	31.5	dB
Gain Ripple	G_{RIPPLE}	f_{RF} = 2.3GHz to 2.7GHz (Difference between maximum and minimum gain in each 100MHz subrange within the specified frequency range)		±0.75		dB
Noise Figure	NF	Measured at antenna port ideally matched to LNA		1.5	1.7	dB
		T_{EPAD} = 105°C			2.3	
		Low Gain Mode		1.5		

[a] Items in the "Minimum"/"Maximum" columns in ***bold italics*** are guaranteed by test. Items in the "Minimum"/"Maximum" columns NOT in bold italics are guaranteed by design characterization.

Table 6. Electrical Characteristics: RX Path in RX Mode Cascaded Performance and TX Performance

See the F0452B Application Circuit in Figure 30. Specifications apply when operated as an RX RF amplifier with V_{DD} = +3.3V, f_{RF} = 2.6GHz, T_{EPAD} = +25°C, STBYx = LOW, RX output power = -10dBm, Z_S = Z_L = 50Ω, and EVKit trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Output Third-Order Intercept Point	$OIP3_1$	Pout = 0dBm/tone 5MHz tone separation		23[a]		dBm
	$OIP3_2$	Pout = 0dBm/tone 5MHz tone separation T_{EPAD} = -40°C to 105°C	20			
	$OIP3_3$	Pout = 0dBm/tone 5MHz tone separation Low Gain Mode		23		
	$OIP3_4$	Pout = 0dBm/tone 5MHz tone separation Low Gain Mode T_{EPAD} = -40°C to 105°C	18			
Output 1dB Compression	$OP1dB_1$	High Gain Mode [b]	13	15		dBm
	$OP1dB_2$	High Gain Mode T_{EPAD} = -40°C to 105°C	11			
	$OP1dB_3$	Low Gain Mode		14		
	$OP1dB_4$	Low Gain Mode T_{EPAD} = -40°C to 105°C	10			
Channel Isolation	ISO_{CH}	$RFISO_1 = \left(\frac{RX1\_OUT}{RX2\_OUT}\right)_{dB}$ with -60 ≤ SW1_IN ≤ -30dBm $RFISO_2 = \left(\frac{RX2\_OUT}{RX1\_OUT}\right)_{dB}$ with -60 ≤ SW2_IN ≤ -30dBm	40	50		dB
RF Switch Isolation	ISO_{SW}	TX Mode Measured at SW_IN to RX_OUT of the same channel	55	65		dB

[a] Items in the "Minimum"/"Maximum" columns in ***bold italics*** are guaranteed by test. Items in the "Minimum"/"Maximum" columns not in bold italics are guaranteed by design characterization.

[b] In the OP1dB calculation formula, "G" denotes the gain of each part instance at the frequency of interest and appropriate HIGH / LOW gain state.

Thermal Characteristics

Table 7. Thermal Characteristics

Parameter	Symbol	Value	Units
Junction-to-Ambient Thermal Resistance	θ_{JA}	43	°C/W
Junction-to-Case Thermal Resistance (Case is defined as the exposed paddle)	θ_{JC_BOT}	11.7	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL3	

Typical Operating Conditions

Unless otherwise noted:

- V_{DD} = +3.3V
- T_{EPAD} = 25°C
- $Z_L = Z_S$ = 50Ω single-ended with matching networks
- STBY1 = STBY2 = LOW or open
- SW_CTRL = LOW or open
- Gain Setting = High Gain Mode
- $P_{IN} \leq$ -30dBm
- All temperatures are referenced to the exposed paddle
- Evaluation kit traces and connector losses are de-embedded

Typical Performance Characteristics: Part 1

Figure 3. RX Mode Gain (High Gain)

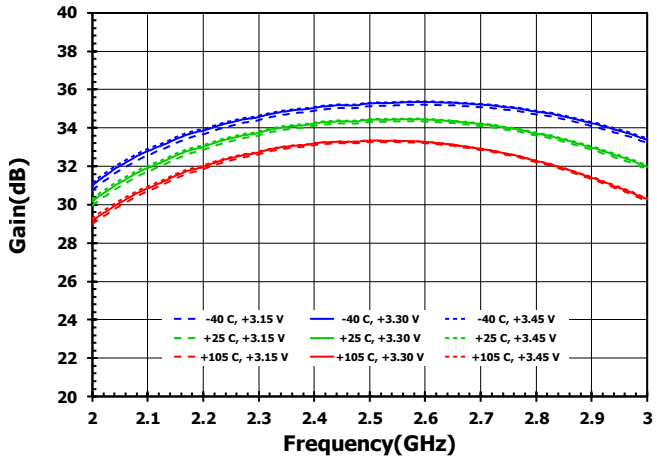


Figure 4. RX Mode Gain (Low Gain)

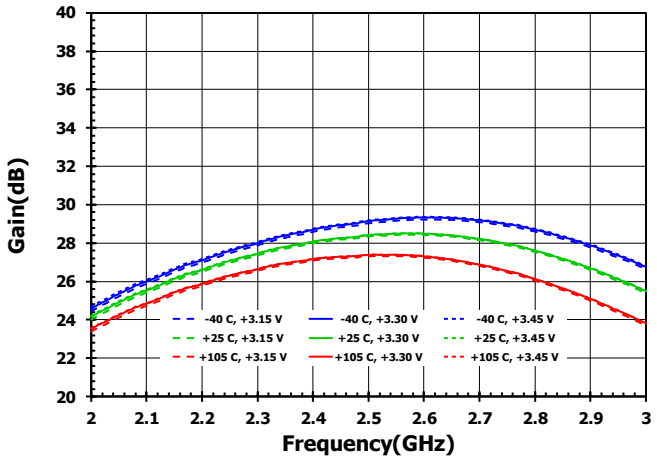


Figure 5. RX Mode Channel Isolation (High Gain)

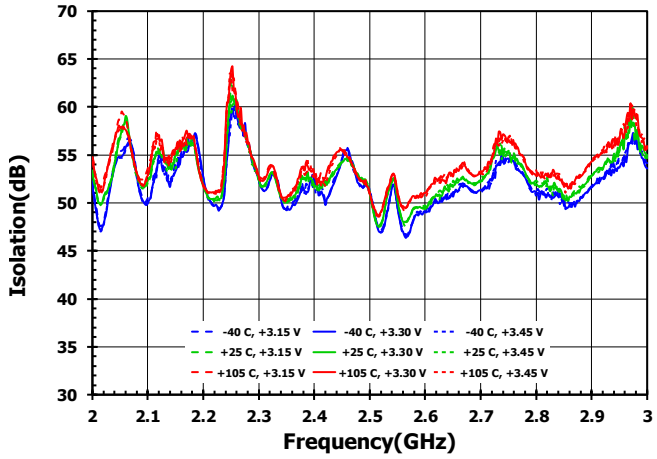


Figure 6. RX Mode Channel Isolation (Low Gain)

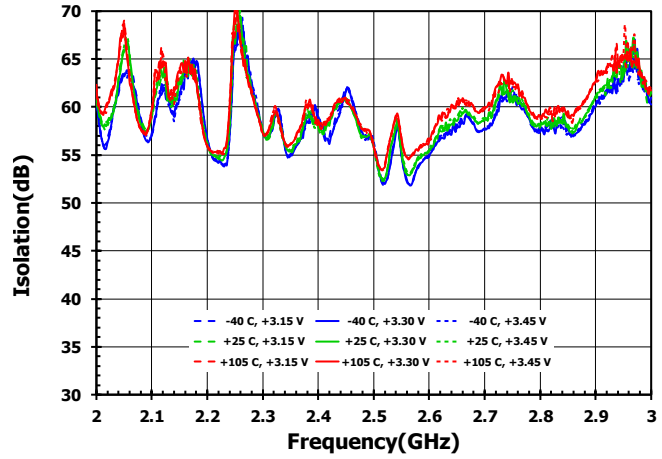


Figure 7. RX Mode Input Return Loss (High Gain)

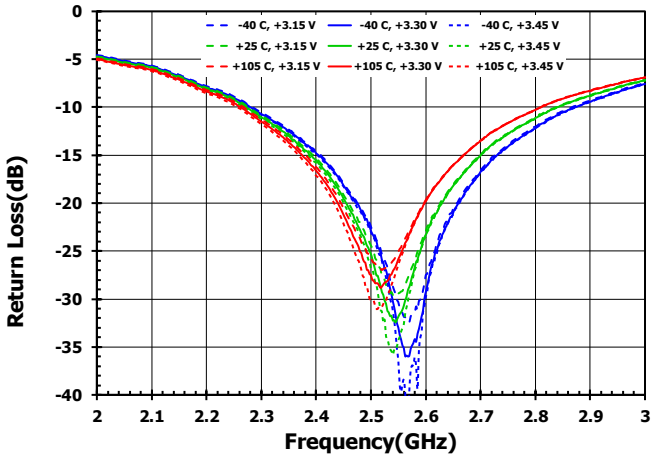
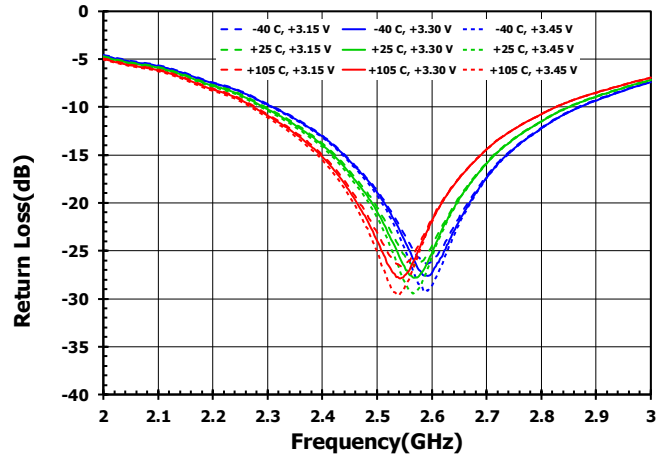


Figure 8. RX Mode Input Return Loss (Low Gain)



Typical Performance Characteristics: Part 2

Figure 9. RX Mode Output Return Loss (High Gain)

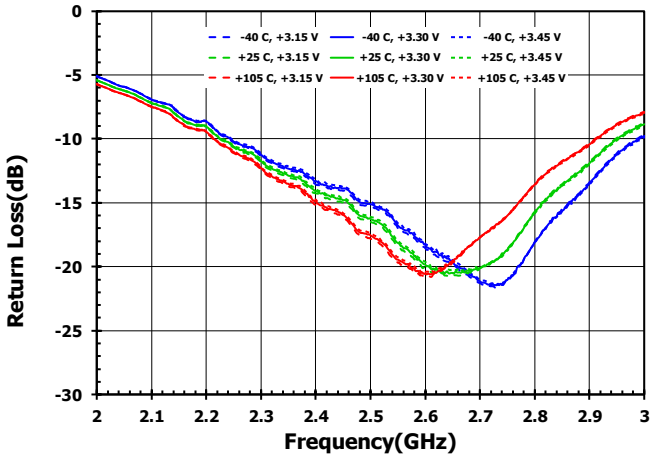


Figure 10. RX Mode Output Return Loss (Low Gain)

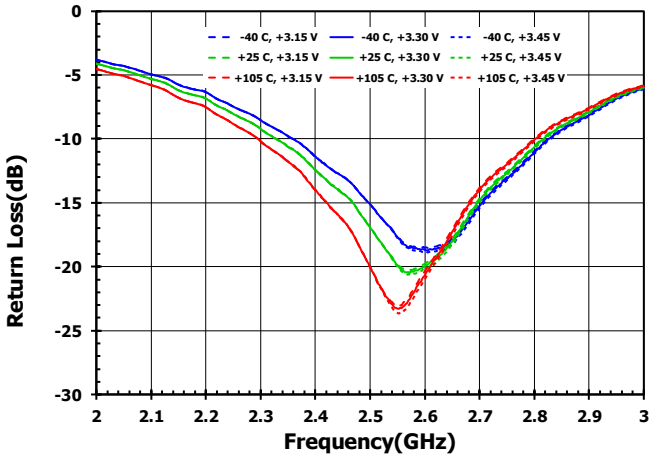


Figure 11. RX Mode OP1dB vs. Frequency (High Gain)

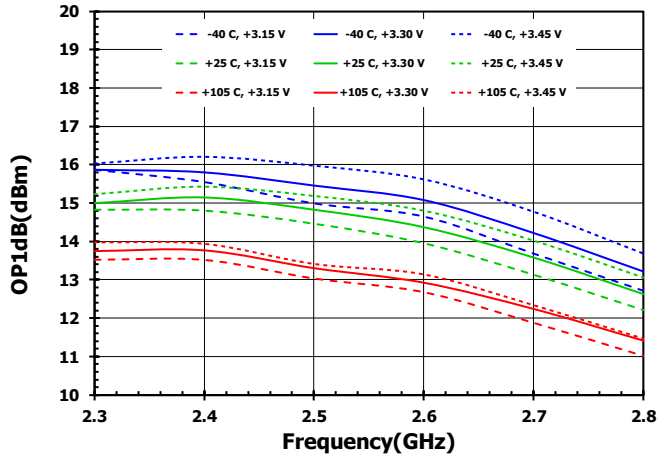


Figure 12. RX Mode OP1dB vs. Frequency (Low Gain)

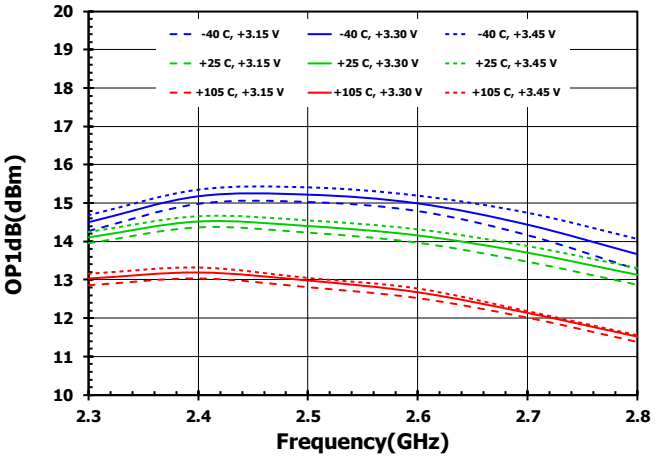


Figure 13. RX Mode OIP3 vs. Frequency (High Gain)

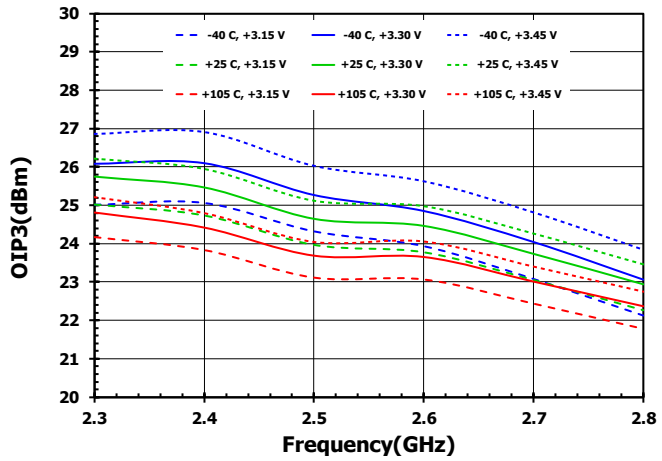
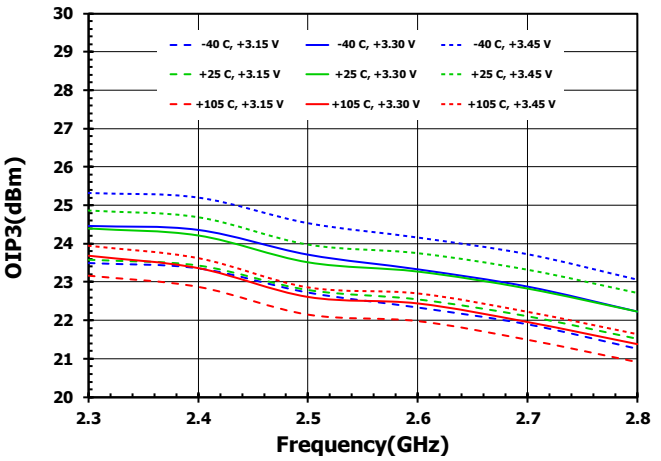


Figure 14. RX Mode OIP3 vs. Frequency (Low Gain)



Typical Performance Characteristics: Part 3

Figure 15. TX Mode Switch Isolation (SWx_IN to RXx_OUT)

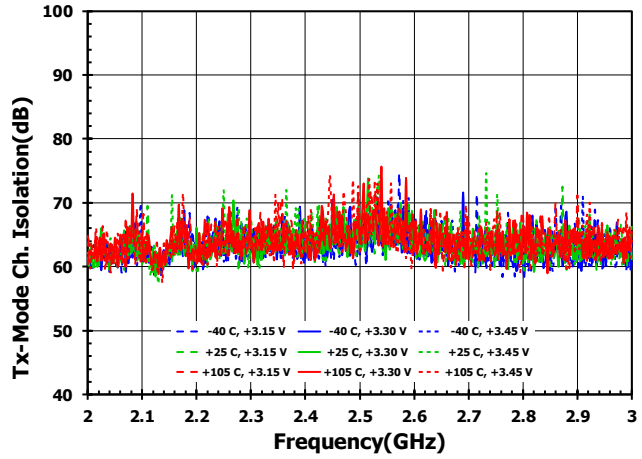


Figure 16. TX Mode Channel Isolation (Switch Inputs)

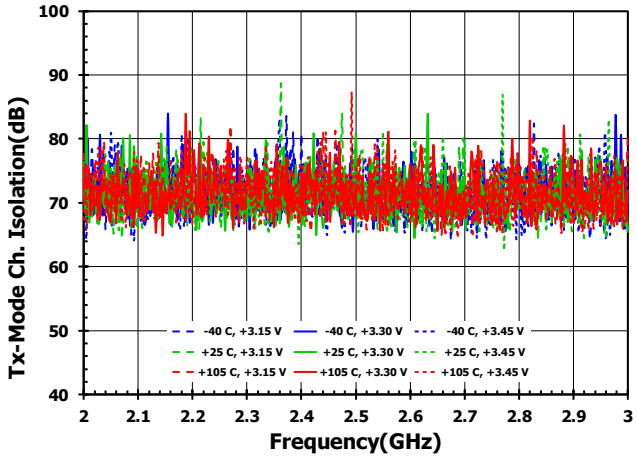


Figure 17. TX Mode Input Return Loss

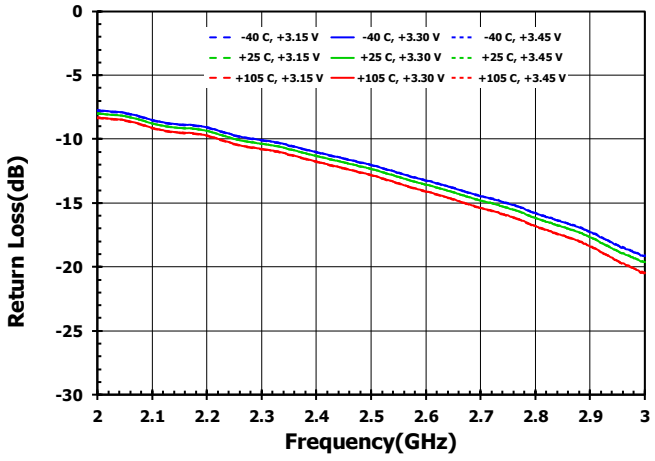


Figure 18. Stability Factor

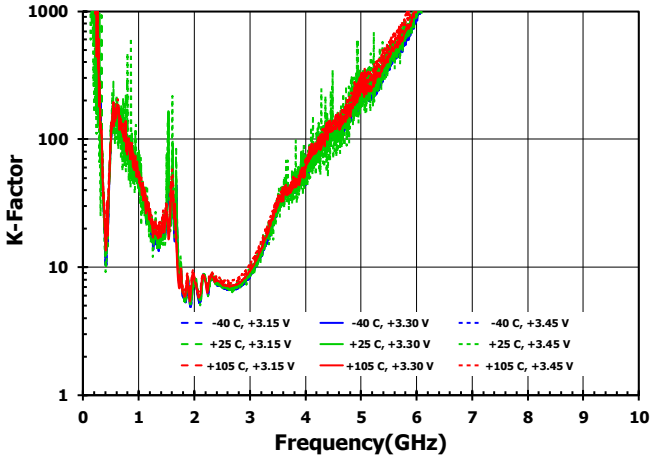


Figure 19. RX Mode Noise Figure (High Gain)

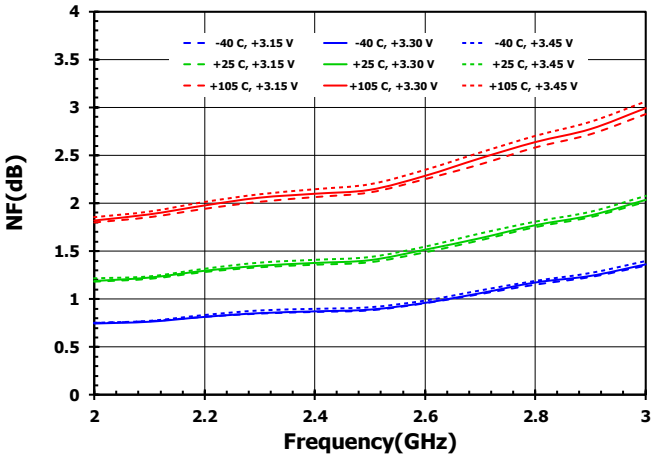
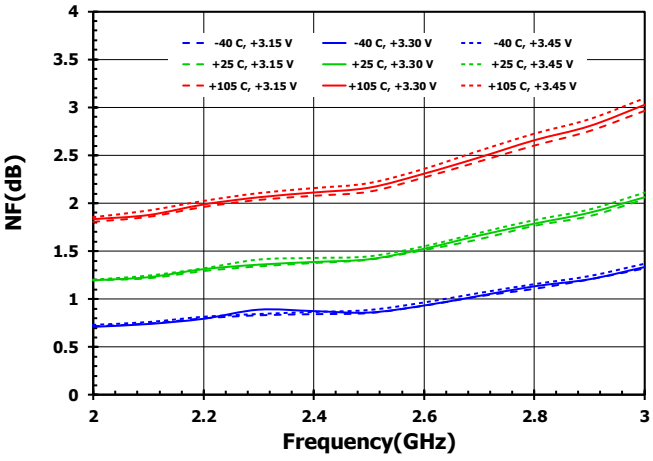


Figure 20. RX Mode Noise Figure (Low Gain)



Typical Performance Characteristics: Part 4

Figure 21. Switching Time from TX to RX Mode

Figure 22. Switching Time from RX to TX Mode

Figure 23. Standby to RX Mode Transient Time

Figure 24. RX Mode to Standby Transient Time

Figure 25. 6dB Gain Reduction Transient Time

Figure 26. 6dB Gain Increase Transient Time

Programming

Table 8. Gain Step Truth Table

ATT1_CTRL, ATT2_CTRL	Attenuation Setting
LOW or Open	0dB
HIGH	6dB

Table 9. Standby and RF Switch Truth Table

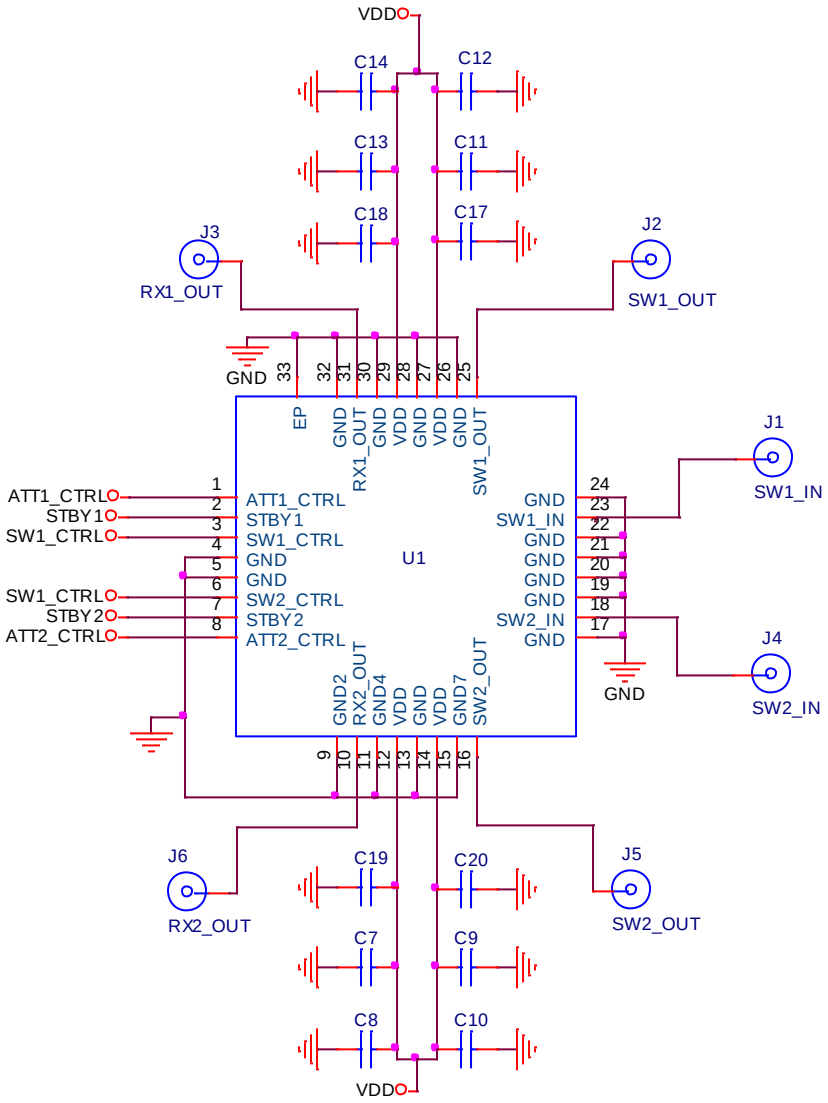
In TX Mode, the amplifiers are OFF but the bias will remain ON for fast turn-on recovery time.

STBY1, STBY2	SW1_CTRL, SW2_CTRL	MODE	Amplifier State
LOW or Open	LOW or Open	RX	ON
LOW or Open	HIGH	TX	OFF
HIGH	HIGH or LOW or Open	STANDBY	OFF

Typical Application Circuit

Figure 27 is a typical circuit (minimum components) that can be used in a design for the F0452B by the customer.

Figure 27. Electrical Schematic



Evaluation Kit Picture

Figure 28. Evaluation Kit: Top View

TBD

Figure 29. Evaluation Kit: Bottom View

TBD

Evaluation Kit / Applications Circuit

Figure 30. Electrical Schematic

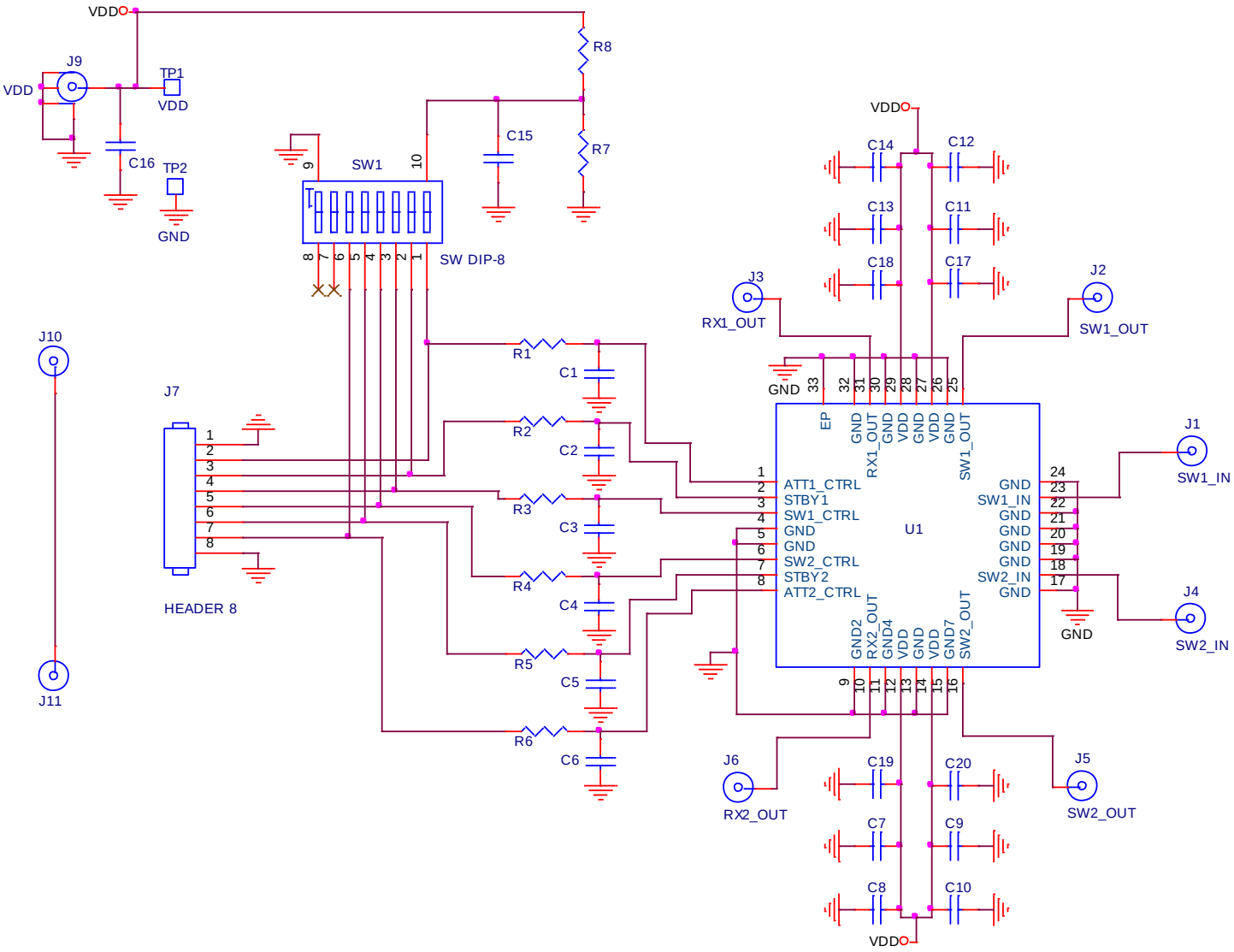


Table 10. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1, C6	0	DNP		
C2 - C5	4	CAP CER 100pF 50V 5% NP0 (0402)	GRM1555C1H101JA01D	Murata
C7, C9, C11, C13	4	CAP CER 10000pF 50V 10% X7R (0402)	GRM155R71H103KA88D	Murata
C8, C10, C12, C14	4	CAP CER 1µF 10V 10% X5R (0402)	GRM155R61A105KE15D	Murata
C15	1	CAP CER 10000pF 50V 5% C0G/NP0 (0603)	GRM1885C1H103JA01D	Murata
C17-C20	1	CAP CER 8.0pF ±0.1pF 50V NP0 (0402)	GJM1555C1H8R0BB01D	Murata
R1, R6	1	0Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF0000X	Panasonic
R2-R5	4	100Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	Panasonic
R7	1	1kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1001X	Panasonic
R8	1	1.3kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1301X	Panasonic
J1- J6, J10, J11	8	SMA Edge Mount	142-0761-881	Cinch Connectivity
J7	1	CONN HEADER VERT SGL 8POS GOLD	961108-6404-AR	3M
J9	1	CONN SMA JACK STR 50OHM EDGE MNT	142-0701-851	Cinch Connectivity
TP1, TP2				
SW1	1	8 Pin DIP Switch (3 POS)	KAT1108E	E-Switch
U1	1	Dual Path RF Switch + LNA + DVGA 5X5 LGA	F0452BLEGK	IDT
	1	Printed Circuit Board	F0453 EVKIT Stripline R2	

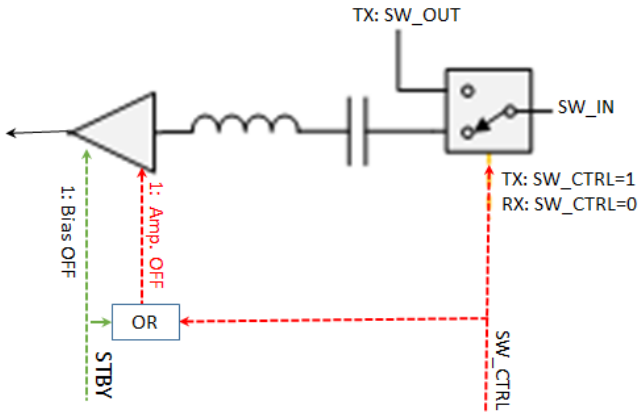
Evaluation Kit Operation

TBD

Mode Control Setup

There are three operation modes as described in Table 9: RX Mode, TX Mode, and Standby Mode. Based on each mode, set up the standby pins and switch control pins as described in Table 9. The standby and switch control logic are shown in Figure 31.

Figure 31. Standby and Switch Control Logic



Power-On Procedure

Set up the voltage supplies and Evaluation Board so that the STBY1 and STBY2 pins are either open or connected to logic LOW, and then enable the power supply.

Power-Off Procedure

Disable the power supply.

Application Information

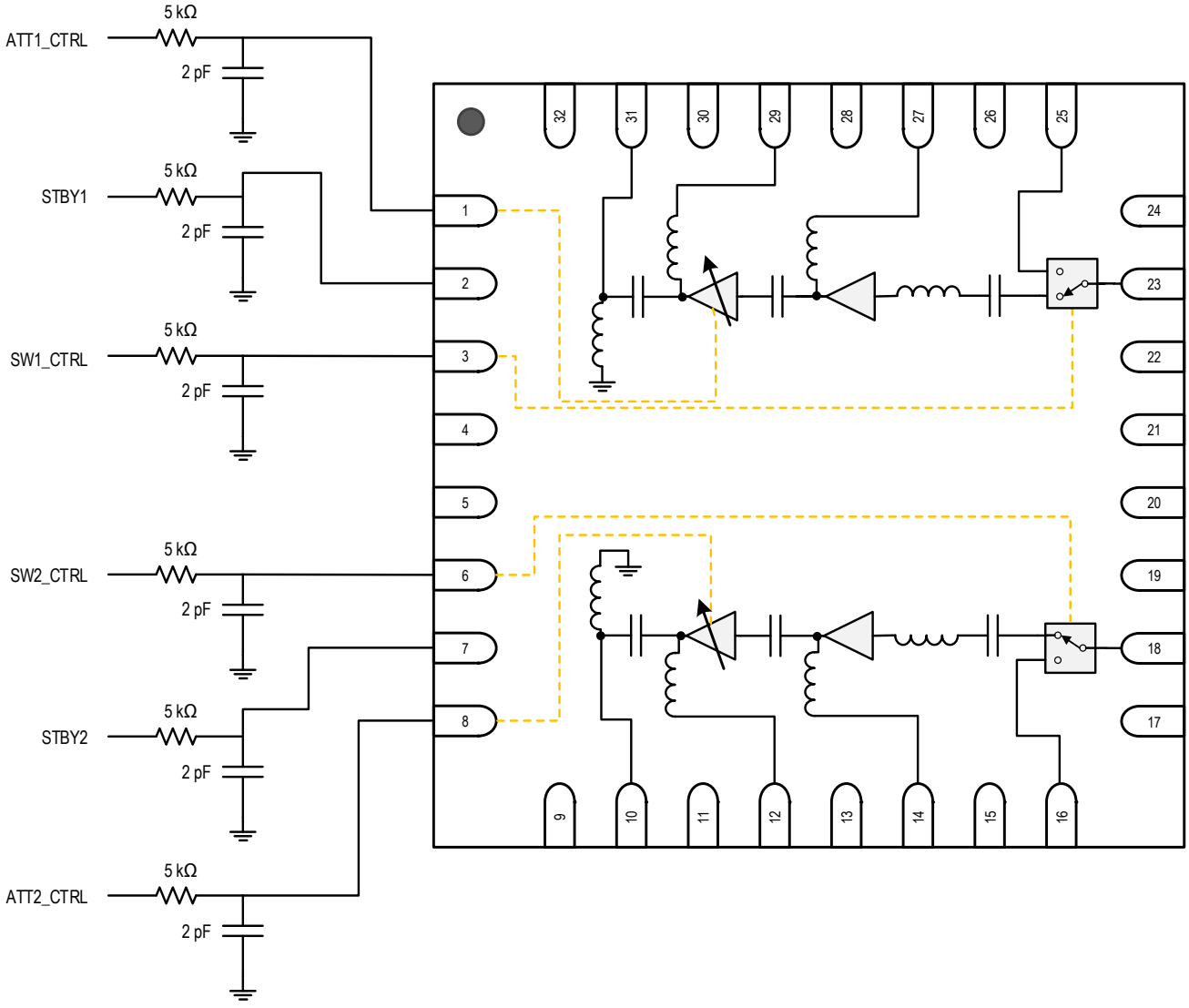
Power Supplies

A common V_{DD} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade the noise figure, and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V / 20µs. In addition, all control pins should remain at 0V (±0.3V) while the supply voltage ramps up or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 1, 2, 3, 6, 7, and 8 shown in Figure 32.

Figure 32. Control Pin Interface Schematic



Package Outline Drawings

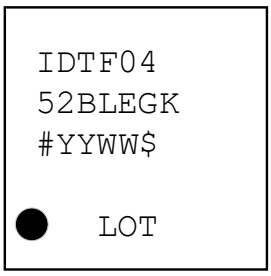
The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/leg32-package-outline-50-x-50-mm-body-08-mm-thick-05mm-pitch-lga

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F0452BLEGK	5.0 × 5.0 × 0.8 mm 32-LGA	MSL3	Tray	-40° to +105°C
F0452BLEGK8	5.0 × 5.0 × 0.8 mm 32-LGA	MSL3	Reel	-40° to +105°C
F0452BEVB	Evaluation Board			

Marking Diagram

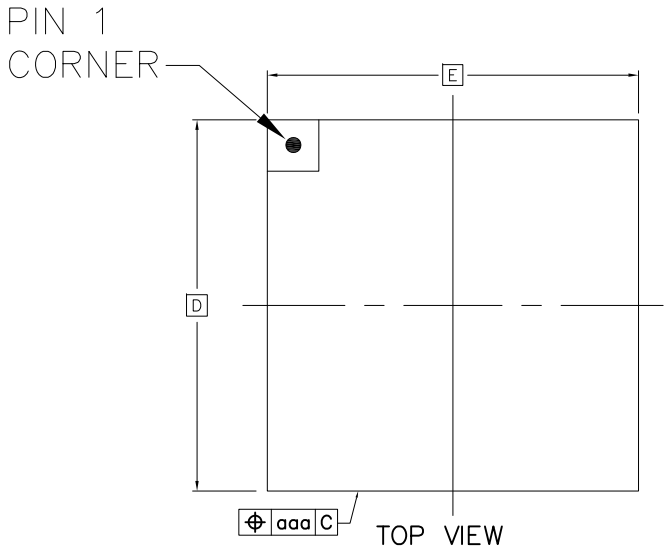


- Lines 1 and 2 indicate the part number
- Line 3 indicates the following:
  - "#" denotes stepping
  - "YY" is the last two digits of the year; "WW" is the work week number when the part was assembled.
  - "$" denotes the mark code.
- Line 4 is the lot number

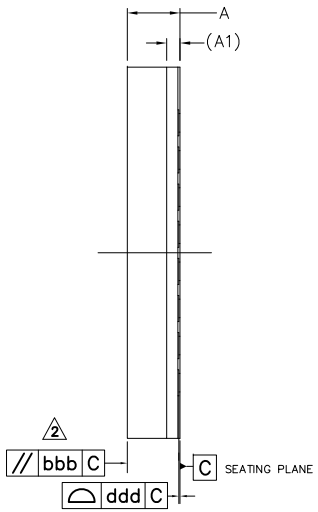
Revision History

Revision Date	Description of Change
May 7, 2019	Initial release.

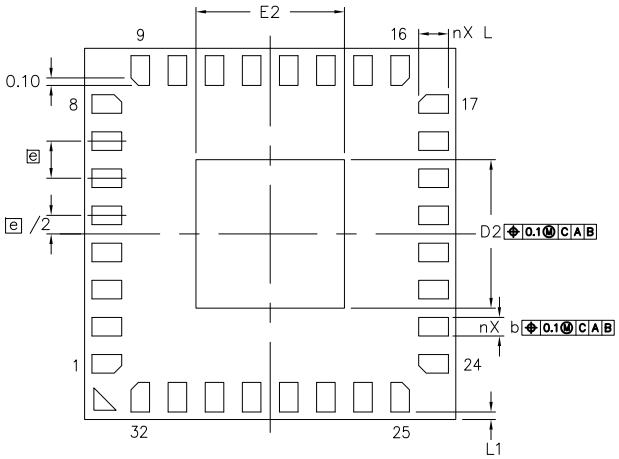
REVISIONS			
REV	DESCRIPTION	DATE CREATED	AUTHOR
01	MODIFIED DIMENSION "A"	2/8/17	SRIKANTH
00	INITIAL RELEASE	1/9/17	SRIKANTH
	REFER TO DCP FOR OFFICIAL RELEASE DATE		



TOP VIEW



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	0.64	–	0.80
A1	0.18 REF.		
D	5.0 BSC		
E	5.0 BSC		
b	0.20	0.25	0.30
L	0.35	0.40	0.45
L1	0.05	0.10	0.15
e	0.5 BSC		
D2	1.95	2.00	2.05
E2	1.95	2.00	2.05
aaa	0.10		
bbb	0.10		
ddd	0.08		



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS IN MM.
2. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

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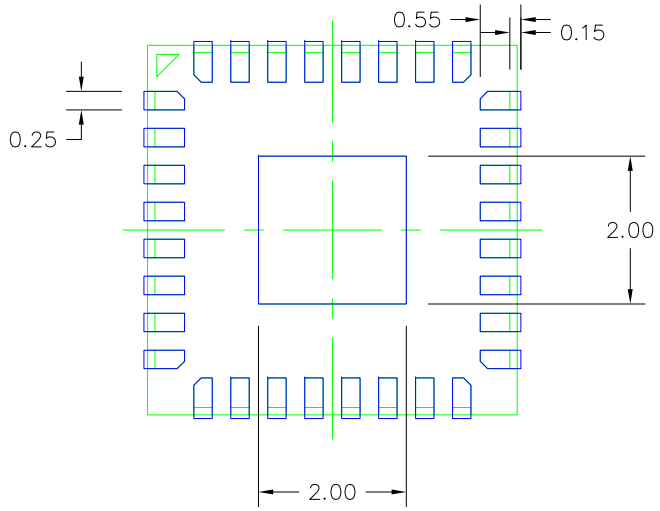
TITLE LEG32 PACKAGE OUTLINE
5.0 x 5.0 mm BODY
0.8 mm Thick, 0.5mm PITCH LGA

SIZE	DRAWING No.	REV
C	PSC-4684	01

DO NOT SCALE DRAWING | SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE CREATED	AUTHOR
01	MODIFIED DIMENSION "A"	2/8/17	SRIKANTH
00	INITIAL RELEASE	1/9/17	SRIKANTH
	REFER TO DCP FOR OFFICIAL RELEASE DATE		



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

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0.8 mm Thick, 0.5mm PITCH LGA

SIZE	DRAWING No.	REV
C	PSC-4684	01

DO NOT SCALE DRAWING

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