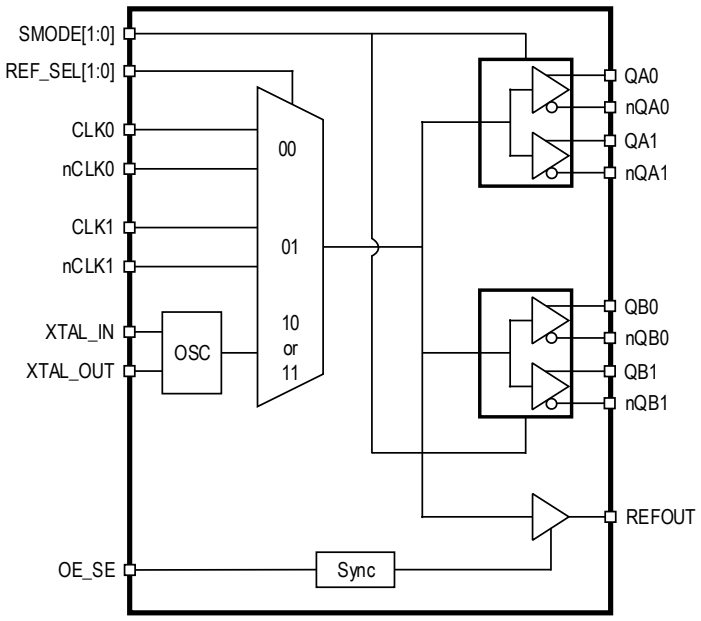
Description

The 8T39204 is a high-performance clock fanout buffer. The input clock can be selected from two differential inputs or one crystal input. The internal oscillator circuit is automatically disabled if the crystal input is not selected. The crystal pin can be driven by a single-ended clock. The selected signal is distributed to four differential outputs which can be configured as LVPECL, LVDS or HCSL outputs. In addition, an LVCMOS output is provided. All outputs can be disabled into a high-impedance state.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. The outputs are at a defined level when inputs are open or tied to ground. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.

Block Diagram

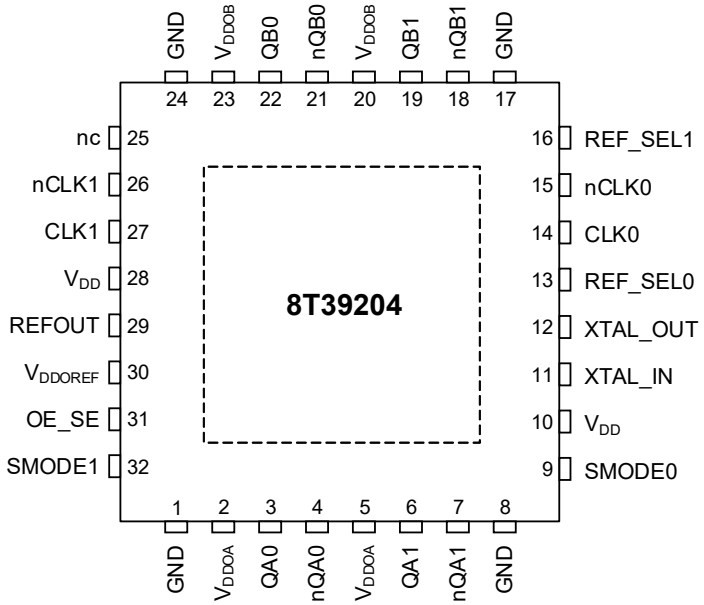


Features

- Two differential reference clock input pairs
- Differential input pairs can accept the following input levels: LVPECL, LVDS, HCSL, HSTL, and Single-ended
- Crystal Oscillator Interface
- Crystal input frequency range: 10MHz to 40MHz
- Maximum Output Frequency
  - LVPECL - 1.5GHz
  - LVDS - 1.5GHz
  - HCSL - 750MHz
  - LVCMOS - 250MHz
- Two banks, each has two differential output pairs that can be configured as LVPECL, LVDS, or HCSL
- One single-ended reference output with synchronous enable to avoid clock glitch
- Output skew: 81ps (maximum), Bank A and Bank B at the same output level
- Part-to-part skew: 200ps (typical), design target
- Additive RMS phase jitter at 156.25MHz, (12kHz - 20MHz): 37.6fs (typical), 3.3V/3.3V
- Supply voltage modes:
  - V_{DD}/V_{DDO}
  - 3.3V/3.3V
  - 3.3V/2.5V
  - 2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Contents

Pin Assignments



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type[a]		Description
1	GND	Power		Power supply ground.
2	V_{DDOA}	Power		Output supply pin for Bank QA outputs.
3	QA0	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
4	nQA0	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
5	V_{DDOA}	Power		Output supply pin for Bank QA outputs.
6	QA1	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
7	nQA1	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
8	GND	Power		Power supply ground.
9	SMODE0	Input	Pull-down	Output driver select for Bank A and Bank B outputs. See Table 3 for function. LVCMOS/LVTTL interface levels.
10	V_{DD}	Power		Power supply pin.
11	XTAL_IN	Input		Crystal oscillator interface.
12	XTAL_OUT	Output		Crystal oscillator interface.
13	REF_SEL0	Input	Pull-down	Input clock selection. LVCMOS/LVTTL interface levels. See Table 3 for function.
14	CLK0	Input	Pull-up/ Pull-down	Non-inverting differential clock. Internally biased to $0.33V_{DD}$.
15	nCLK0	Input	Pull-up/ Pull-down	Inverting differential clock. Internal resistor bias to $0.4V_{DD}$.
16	REF_SEL1	Input	Pull-down	Input clock selection. LVCMOS/LVTTL interface levels. See Table 3 for function.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type[a]		Description
17	GND	Power		Power supply ground.
18	nQB1	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
19	QB1	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
20	V_{DDOB}	Power		Output supply pin for Bank QB outputs.
21	nQB0	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
22	QB0	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
23	V_{DDOB}	Power		Output supply pin for Bank QB outputs.
24	GND	Power		Power supply ground.
25	nc	Unused		No connect pin.
26	nCLK1	Input	Pull-up/ Pull-down	Inverting differential clock. Internal resistor bias to $0.4V_{DD}$.
27	CLK1	Input	Pull-up/ Pull-down	Non-inverting differential clock. Internally biased to $0.33V_{DD}$.
28	V_{DD}	Power		Power supply pin.
29	REFOUT	Output		Single-ended reference clock output. LVCMOS/LVTTL interface levels.
30	V_{DDOREF}	Power		Output supply pin for REFOUT output.
31	OE_SE	Input	Pull-down	Output enable. LVCMOS/LVTTL interface levels. See Table 4.
32	SMODE1	Input	Pull-down	Output driver select for Bank A and Bank B outputs. See Table 6 for function. LVCMOS/LVTTL interface levels.
0	ePAD	Power		Connect ePAD to ground to ensure proper heat dissipation.

[a] *Pull-down* and *Pull-up* refer to internal input resistors. See Table 2 for typical values

Pin Characteristics

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	OE_SE, SMODE[1:0], REF_SEL[1:0]			2		pF
$R_{PULLDOWN}$	Input Pull-down Resistor				50		kΩ
R_{PULLUP}	Input Pull-up Resistor	CLK0, CLK1			100		kΩ
		nCLK0, nCLK1			75		kΩ
C_{PD}	Power Dissipation Capacitance	REFOUT	V_{DDOREF} = 3.465V		5.0		pF
			V_{DDOREF} = 2.625V		4.5		pF
R_{OUT}	Output Impedance	REFOUT	V_{DDOREF} = 3.3V		45		Ω
			V_{DDOREF} = 2.5V		58		Ω

Function Tables

Table 3. REF_SELx Function Table

Control Input REF_SEL[1:0]	Selected Input Reference Clock
00 (default)	CLK0, nCLK0
01	CLK1, nCLK1
10	XTAL
11	XTAL

Table 4. OE_SE Function Table[a]

OE_SE	REFOUT
0 (default)	High-Impedance
1	Enabled

[a] Synchronous output enable to avoid clock glitch.

Table 5. Input/Output Operation Table, OE_SE

Input Status			Output State
OE_SE	REF_SEL [1:0]	CLKx and nCLKx	REFOUT
0 (default)	Don't care	Don't Care	High Impedance
1	10 or 11	Don't Care	Fanout Crystal Oscillator
1	00 (default)	CLK0 and nCLK0 are both open circuit	Logic Low
		CLK0 and nCLK0 are tied to ground	Logic Low
		CLK0 is high, nCLK0 is low	Logic High
		CLK0 is low, nCLK0 is high	Logic Low
1	01	CLK1 and nCLK1 are both open circuit	Logic Low
		CLK1 and nCLK1 are tied to ground	Logic Low
		CLK1 is high, nCLK1 is low	Logic High
		CLK1 is low, nCLK1 is high	Logic Low

Table 6. Output Level Selection Table, QX[0:1], nQX[0:1][a]

SMODE1	SMODE0	Output Type
0	0	LVPECL (default)
0	1	LVDS
1	0	HCSL
1	1	High-Impedance

[a] X denotes A and B.

Table 7. Input/Output Operation Table, SMODE[1:0]

Input Status			Output State
SMODE[1:0]	REF_SEL[1:0]	CLKx and nCLKx	QA[1:0], nQA[1:0]
11	Don't care	Don't Care	High Impedance
00, 01 or 10	10 or 11	Don't Care	Fanout crystal oscillator
00, 01 or 10	00 (default)	CLK0 and nCLK0 are both open circuit	QA[1:0] = Low nQA[1:0] = High
		CLK0 and nCLK0 are tied to ground	QA[1:0] = Low nQA[1:0] = High
		CLK0 is high, nCLK0 is low	QA[1:0] = High nQA[1:0] = Low
		CLK0 is low, nCLK0 is high	QA[1:0] = Low nQA[1:0] = High

Table 7. Input/Output Operation Table, SMODE[1:0] (Cont.)

Input Status			Output State
00, 01 or 10	01	CLK1 and nCLK1 are both open circuit	QA[1:0] = Low nQA[1:0] = High
		CLK1 and CLK1 are tied to ground.	QA[1:0] = Low nQA[1:0] = High
		CLK1 is high, nCLK1 is low	QA[1:0] = High nQA[1:0] = Low
		CLK1 is low, nCLK1 is high	QA[1:0] = Low nQA[1:0] = High

Table 8. Input/Output Operation Table, SMODE[1:0]

Input Status			Output State
SMODE[1:0]	REF_SEL[1:0]	CLKx and nCLKx	QB[1:0], nQB[1:0]
11	Don't care	Don't Care	High Impedance
00, 01 or 10	10 or 11	Don't Care	Fanout Crystal Oscillator
00, 01 or 10	00 (default)	CLK0 and nCLK0 are both open circuit	QB[1:0] = Low nQB[1:0] = High
		CLK0 and nCLK0 are tied to ground	QB[1:0] = Low nQB[1:0] = High
		CLK0 is high, nCLK0 is low	QB[1:0] = High nQB[1:0] = Low
		CLK0 is low, nCLK0 is high	QB[1:0] = Low nQB[1:0] = High
00, 01 or 10	01	CLK1 and nCLK1 are both open circuit	QB[1:0] = Low nQB[1:0] = High
		CLK1 and nCLK1 are tied to ground	QB[1:0] = Low nQB[1:0] = High
		CLK1 is high, nCLK1 is low	QB[1:0] = High nQB[1:0] = Low
		CLK1 is low, nCLK1 is high	QB[1:0] = Low nQB[1:0] = High

Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 9. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to 2V -0.5V to V_{DD} + 0.5V
Outputs, V_O, (HCSL, LVCMOS)	-0.5V to V_{DDOX}[a]+ 0.5V
Outputs, I_O, (LVPECL) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O, (LVDS) Continuous Current Surge Current	 10mA 15mA
Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Mode[b]	2000V
ESD - Charged Device Mode[b]	500V

[a] V_{DDOX} denotes V_{DDOA}, V_{DDOB}.

[b] According to JEDEC/JSED JS-001-2012/22-C101 E.

DC Electrical Characteristics

Table 10. Power Supply Current, V_{DD} = 3.3V ±5, V_{DDOA} = V_{DDOB} = 3.3V ±5, GND = 0V, T_A = -40°C to 85°C[a]

Symbol	Parameter	Test Conditions			Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage				3.135		3.465	V
V_{DDOA}, V_{DOOB}, V_{DDOREF}	Output Power Voltage				3.135		3.465	V
I_{DD}	Power Supply Current					33	37	mA
I_{EE}	Output Power Supply Current	SMODE[1:0]=00 (default; LVPECL) V_{DDOA} = V_{DDOB} = 3.465V	Outputs Unloaded	f_{OUT} = 156.25MHz		90	101	mA
				f_{OUT} = 781.25MHz		124	141	mA
				f_{OUT} = 1500MHz		141	159	mA

[a] V_{DDOX} denotes V_{DDOA}, V_{DDOB}

Table 11. Output Supply Current, V_{DD} = 3.3V ±5, or 2.5V ±5, V_{DDOA} = V_{DDOB} = 2.5V ±5, GND = 0V, T_A = -40°C to 85°C[a]

Symbol	Parameter	Test Conditions			Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage				2.375		3.465	V
V_{DDOA}, V_{DOOB}, V_{DDOREF}	Output Power Voltage				2.375		3.465	V
I_{DD}	Power Supply Current					33	37	mA
I_{EE}	Output Power Supply Current	SMODE[1:0]=00 (default; LVPECL) V_{DDOA} = V_{DDOB} = 2.625V	Outputs Unloaded	f_{OUT} = 156.25MHz		88	100	mA
				f_{OUT} = 781.25MHz		120	136	mA
				f_{OUT} = 1500MHz		145	164	mA

[a] V_{DDOX} denotes V_{DDOA}, V_{DDOB}

Table 12. Maximum Output Supply Current, V_{DDO} = 3.3V +5, or 2.5V +5, V_{EE} = 0V[a]

Symbol	Parameter	Test Conditions		V_{DDOx} = 3.3 +5%			V_{DDOx} = 2.5 +5%			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{DDOA} + I_{DDOB}	Bank A & Bank B Current SMODE[1:0]=00 (default; LVPECL)	Outputs Unloaded	f_{OUT} = 156.25MHz		49	57		42	48	mA
			f_{OUT} = 781.25MHz		78	90		70	81	mA
			f_{OUT} = 1500MHz		105	121		96	111	mA
		Outputs Loaded 50Ω to V_{DDOx} - 2V	f_{OUT} = 156.25MHz		106	122		100	114	mA
			f_{OUT} = 781.25MHz		138	159		122	140	mA
			f_{OUT} = 1500MHz		165	190		145	167	mA
I_{DDOA} + I_{DDOB}	Bank A & Bank B Current SMODE[1:0]=01 (LVDS)	Outputs Unloaded	f_{OUT} = 156.25MHz		55	63		57	66	mA
			f_{OUT} = 468.75MHz		72	83		72	82	mA
			f_{OUT} = 800MHz		88	101		88	101	mA
		Outputs Loaded	f_{OUT} = 156.25MHz		61	70		64	73	mA
			f_{OUT} = 468.75MHz		78	90		78	90	mA
			f_{OUT} = 800MHz		96	110		95	109	mA

Table 12. Maximum Output Supply Current, V_{DDO} = 3.3V +5, or 2.5V +5, V_{EE} = 0V[a]

Symbol	Parameter	Test Conditions		V_{DDOx} = 3.3 +5%			V_{DDOx} = 2.5 +5%			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{DDOA} + I_{DDOB}	Bank A & Bank B Current SMODE[1:0]=10 (HCSL)	Outputs Unloaded	f_{OUT} = 100MHz		29	33		28	33	mA
			f_{OUT} = 156.25MHz		31	35		30	35	mA
			f_{OUT} = 250MHz		35	41		35	40	mA
			f_{OUT} = 750MHz		58	66		58	66	mA
		Outputs Loaded	f_{OUT} = 100MHz		101	116		101	116	mA
			f_{OUT} = 156.25MHz		103	119		103	118	mA
			f_{OUT} = 250MHz		107	123		107	123	mA
			f_{OUT} = 750MHz		121	137		120	136	mA

[a] V_{DDOX} denotes V_{DDOA}, V_{DDOB}

Table 13. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ±5%, 2.5V ±5%, V_{DDOREF} = = 3.3V ±5% or 2.5V ±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OE_SE, SMODE[1:0], REF_SEL[1:0]	V_{DD} = 3.3V±5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V±5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OE_SE, SMODE[1:0], REF_SEL[1:0]	V_{DD} = 3.3V±5%	-0.3		0.8	V
			V_{DD} = 2.5V±5%	-0.3		0.7	V
I_{IH}	Input High Current	OE_SE, SMODE[1:0], REF_SEL[1:0]	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	OE_SE, SMODE[1:0], REF_SEL[1:0]	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage	REFOUT	V_{DDOREF} = 3.3V±5%: I_{OH} = -1mA	2.6			V
			V_{DDOREF} = 2.5V±5%: I_{OH} = -1mA	1.8			V
V_{OL}	Output Low Voltage	REFOUT	V_{DDOREF} = 3.3V±5% or 2.5V±5%: I_{OL} = 1mA			0.5	V

Table 14. Differential DC Characteristics, V_{DD} = 3.3V ±5% or 2.5V ±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK[1:0], nCLK[1:0]	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK[1:0], nCLK[1:0]	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage[a]			0.240		1.3	V
V_{CMR}	Common Mode Input Voltage[a][b]			GND + 0.5		V_{DD} – 0.85	V

[a] Input voltage should not be less than -0.3V and greater than V_{DD}.

[b] Common mode voltage is defined as the crosspoint.

Table 15. LVPECL DC Characteristics, V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V ±5%, GND = 0V, T_A = -40°C to 85°C[a][b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[b]		V_{DDOX} – 1.135		V_{DDOX} – 0.8	V
V_{OL}	Output Low Voltage[b]		V_{DDOX} – 2.1		V_{DDOX} – 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing[b]	DC ≤ f_{OUT} ≤ 500MHz	0.6		1.24	V
		500MHz < f_{OUT} ≤ 1GHz	0.4		1.10	V
		f_{OUT} > 1GHz		0.60		V

[a] V_{DDOX} denotes V_{DDOA} and V_{DDOB}.

[b] Outputs terminated with 50Ω to V_{DDOX} – 2V.

Table 16. LVPECL DC Characteristics, V_{DD} = V_{DDOA} = V_{DDOB} = 2.5V ±5%, GND = 0V, T_A = -40°C to 85°C[a][b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[b]		V_{DDOX} – 1.125		V_{DDOX} – 0.8	V
V_{OL}	Output Low Voltage[b]		V_{DDOX} – 2.1		V_{DDOX} – 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing[b]	DC ≤ f_{OUT} ≤ 500MHz	0.6		1.20	V
		500MHz < f_{OUT} ≤ 1GHz	0.4		1.00	V
		1GHz < f_{OUT} ≤ 1.5GHz		0.56		V

[a] V_{DDOX} denotes V_{DDOA} and V_{DDOB}.

[b] Outputs terminated with 50Ω to V_{DDOX} – 2V.

Table 17. LVDS DC Characteristics, V_{DDOA} = V_{DDOB} = 3.3V ±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		435		570	mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage		1.16		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 18. LVDS DC Characteristics, V_{DDOA} = V_{DDOB} = 2.5V ±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		425		570	mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage		1.15		1.365	V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 19. Crystal Characteristics[a]

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Capacitive Loading (C_L)			12	18	pF

[a] Crystal operation requires tuning caps. For more information, see Applications Information.

AC Electrical Characteristics

Table 20. V_{DD} = V_{DDOA} = V_{DDOB} = V_{DDOREF} = 3.3V ±5%, GND = 0V, T_A = -40°C to 85°C[a][b]

Symbol	Parameter		Test Conditions		Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	LVPECL Outputs			DC		1500	MHz
		LVDS Outputs			DC		800	MHz
		HCSL Outputs			DC		750	MHz
		LVCMOS (REFOUT)			DC		250	MHz
t_{jit}	Buffer Additive Phase Jitter, RMS: Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01		Clock Frequency = 156.25MHz; Input Clock from 8T49NS010A; Input Clock Jitter = 83.9fs SMODE[1:0] = 00 (default; LVPECL)			37.6		fs
tjit(Ø)	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz		REF_SEL[1:0] = 10 or 11[c]			0.307		ps
NF	Noise Floor	LVPECL	Offset Frequency > 10MHz; 156.25MHz Clock Frequency			-159.5		dBc/Hz
		LVDS				-157.9		dBc/Hz
		HCSL				-157.7		dBc/Hz
t_{PD}	Propagation Delay[d]	CLK0, nCLK0 or, CLK1, nCLK1 any Qx, nQx Outputs	SMODE[1:0] = 00 (default; LVPECL)	f_{OUT} ≤ 1GHz	0.75		1.50	ns
				f_{OUT} > 1GHz		1.23		ns
			SMODE[1:0] = 01 (LVDS)		0.820		1.475	ns
			SMODE[1:0] = 10 (HCSL)		0.860		1.440	ns
tsk(o)	Output Skew[e][f]						81	ps
tsk(pp)	Part-to-Part Skew[f][g]					200		ps
V_{OH}	Voltage High[h][i]	HCSL Outputs	R_T = 50Ω to GND, C_L ≤ 5pF		520		931	mV
V_{OL}	Voltage Low[h][j]	HCSL Outputs			-150		150	mV
V_{CROSS}	Absolute Crossing Voltage[h][k][l]	HCSL Outputs			225		460	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all Edges[h][k][m]	HCSL Outputs					140	mV
	Rise/Fall Edge Rate[c][n][o]	HCSL Outputs			0.6		4	V/ns
t_R / t_F	Output Rise/Fall Time	LVPECL Outputs	20% to 80%			200	695	ps
		LVDS Outputs	20% to 80%			230	510	ps
		HCSL Outputs	20% to 80%			260	420	ps
		REFOUT	20% to 80%			438	575	ps

Table 20. V_{DD} = V_{DDOA} = V_{DDOB} = V_{DDOREF} = 3.3V ±5%, GND = 0V, T_A = -40°C to 85°C[a][b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
odc	Output Duty Cycle[p]	With Crystal Input	45		55	%
		With External 50% / 50% Duty Cycle Clock Input	45		55	%
MUX_ISOLATION	MUX Isolation	156.25MHz		75		dB

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] LVPECL parameters characterized up to 1.5GHz. LVDS parameters characterized up to 800MHz. HCSL parameters characterized up to 750MHz.

[c] Measurement taken from differential waveform.

[d] Measured from the differential input crosspoint to the differential output crosspoint.

[e] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross- point.

[f] This parameter is defined in accordance with JEDEC Standard 65.

[g] Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoint.

[h] Measurement taken from single-ended waveform.

[i] Vlow is defined as the statistical average Low value as obtained by using the oscilloscope Vlow Math function.

[j] Vhigh is defined as the statistical average High value as obtained by using the oscilloscope Vhigh Math function.

[k] Measured at crosspoint where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

[l] Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoint for this measurement.

[m] Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.

[n] Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

[o] Measured at 100MHz.

[p] Measured for the following frequencies: 25MHz, 100MHz, 125MHz, 156.25MHz, 312.5MHz, 400MHz, 644.5313MHz, and 750MHz.

Table 21. V_{DD} = 3.3V ±5%, V_{DDA} = V_{DDB} = V_{DDOREF} = 2.5V ±5% GND = 0V, T_A = -40°C to 85°C[a][b]

Symbol	Parameter		Test Conditions		Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	LVPECL Outputs			DC		1500	MHz
		LVDS Outputs			DC		800	MHz
		HCSL Outputs			DC		750	MHz
		LVCMOS (REFOUT)			DC		250	MHz
t_{jit}	Buffer Additive Phase Jitter, RMS: Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01		Clock Frequency = 156.25MHz; Input Clock from 8T49NS010A; Input Clock Jitter = 83.9fs SMODE[1:0] = 00 (default; LVPECL)			45.5		fs
tjit(Ø)	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz		REF_SEL[1:0] = 10 or 11[c]			0.309		ps
NF	Noise Floor	LVPECL	Offset Frequency > 10MHz; 156.25MHz Clock Frequency			-158.5		dBc/Hz
		LVDS				-158.1		dBc/Hz
		HCSL				-157.6		dBc/Hz
t_{PD}	Propagation Delay[d]	CLK0, nCLK0 or, CLK1, nCLK1 any Qx, nQx Outputs	SMODE[1:0] = 00 (default; LVPECL)	f_{OUT} ≤ 1GHz	0.58		1.66	ns
				f_{OUT} > 1GHz		1.23		ns
			SMODE[1:0] = 01 (LVDS)		0.75		1.50	ns
			SMODE[1:0] = 10 (HCSL)		0.87		1.43	ns
tsk(o)	Output Skew[e][f]						75	ps
tsk(pp)	Part-to-Part Skew[f][g]					200		ps
V_{OH}	Voltage High[h][i]	HCSL Outputs	R_T = 50Ω to GND, C_L ≤ 5pF		520		931	mV
V_{OL}	Voltage Low[h][j]	HCSL Outputs			-150		150	mV
V_{CROSS}	Absolute Crossing Voltage[h][k][l]	HCSL Outputs			225		460	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all Edges[h][k][m]	HCSL Outputs					140	mV
	Rise/Fall Edge Rate[c][n][o]	HCSL Outputs			0.6		4	V/ns
t_R / t_F	Output Rise/Fall Time	LVPECL Outputs	20% to 80%			130	450	ps
		LVDS Outputs	20% to 80%			225	475	ps
		HCSL Outputs	20% to 80%			275	485	ps
		REFOUT	20% to 80%			434	600	ps
odc	Output Duty Cycle[p]		With Crystal Input		45		55	%
			With External 50% / 50% Duty Cycle Clock Input		45		55	%
$MUX_{\_ISOLATION}$	MUX Isolation		156.25MHz			75		dB

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] LVPECL parameters characterized up to 1.5GHz. LVDS parameters characterized up to 800MHz. HCSL parameters characterized up to 750MHz.

[c] Measurement taken from differential waveform.

[d] Measured from the differential input crosspoint to the differential output crosspoint.

[e] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross- point.

[f] This parameter is defined in accordance with JEDEC Standard 65.

[g] Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoint.

[h] Measurement taken from single-ended waveform.

[i] Vlow is defined as the statistical average Low value as obtained by using the oscilloscope Vlow Math function.

[j] Vhigh is defined as the statistical average High value as obtained by using the oscilloscope Vhigh Math function.

[k] Measured at crosspoint where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

[l] Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoint for this measurement.

[m] Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.

[n] Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

[o] Measured at 100MHz.

[p] Measured for the following frequencies: 25MHz, 100MHz, 125MHz, 156.25MHz, 312.5MHz, 400MHz, 644.5313MHz, and 750MHz.

Table 22. $V_{DD} = V_{DDA} = V_{DDB} = V_{DDOREF}$ = 2.5V ±5% GND = 0V, T_A = -40°C to 85°C[a][b]

Symbol	Parameter		Test Conditions		Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	LVPECL Outputs			DC		1500	MHz
		LVDS Outputs			DC		800	MHz
		HCSL Outputs			DC		750	MHz
		LVCMOS (REFOUT)			DC		250	MHz
t_{jit}	Buffer Additive Phase Jitter, RMS: Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01		Clock Frequency = 156.25MHz; Input Clock from 8T49NS010A; Input Clock Jitter = 83.9fs SMODE[1:0] = 00 (default; LVPECL)			46.91		fs
tjit(Ø)	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz		REF_SEL[1:0] = 10 or 11[c]			0.313		ps
NF	Noise Floor	LVPECL	Offset Frequency > 10MHz; 156.25MHz Clock Frequency			-159.3		dBc/Hz
		LVDS				-157.9		dBc/Hz
		HCSL				-157.8		dBc/Hz
t_{PD}	Propagation Delay[d]	CLK0, nCLK0 or, CLK1, nCLK1 any Qx, nQx Outputs	SMODE[1:0] = 00 (default; LVPECL)	$f_{OUT} \le$ 1GHz	0.63		1.60	ns
				f_{OUT} > 1GHz		1.23		ns
			SMODE[1:0] = 01 (LVDS)		0.825		1.60	ns
			SMODE[1:0] = 10 (HCSL)		0.865		1.50	ns
tsk(o)	Output Skew[e][f]						75	ps
tsk(pp)	Part-to-Part Skew[f][g]					200		ps
V_{OH}	Voltage High[h][i]	HCSL Outputs	R_T = 50Ω to GND, $C_L \le$ 5pF		520		920	mV
V_{OL}	Voltage Low[h][j]	HCSL Outputs			-150		150	mV
V_{CROSS}	Absolute Crossing Voltage[h][k][l]	HCSL Outputs			225		460	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all Edges[h][k][m]	HCSL Outputs					140	mV
	Rise/Fall Edge Rate[c][n][o]	HCSL Outputs			0.6		4	V/ns
t_R / t_F	Output Rise/Fall Time	LVPECL Outputs	20% to 80%			200	525	ps
		LVDS Outputs	20% to 80%			220	485	ps
		HCSL Outputs	20% to 80%			265	485	ps
		REFOUT	20% to 80%			432	625	ps
odc	Output Duty Cycle[p]		With Crystal Input		45		55	%
			With External 50% / 50% Duty Cycle Clock Input		45		55	%
MUX_ISOLATION	MUX Isolation		156.25MHz			75		dB

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] LVPECL parameters characterized up to 1.5GHz. LVDS parameters characterized up to 800MHz. HCSL parameters characterized up to 750MHz.

[c] Measurement taken from differential waveform.

[d] Measured from the differential input crosspoint to the differential output crosspoint.

[e] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross- point.

[f] This parameter is defined in accordance with JEDEC Standard 65.

[g] Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoint.

[h] Measurement taken from single-ended waveform.

[i] Vlow is defined as the statistical average Low value as obtained by using the oscilloscope Vlow Math function.

[j] Vhigh is defined as the statistical average High value as obtained by using the oscilloscope Vhigh Math function.

[k] Measured at crosspoint where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

[l] Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoint for this measurement.

[m] Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.

[n] Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

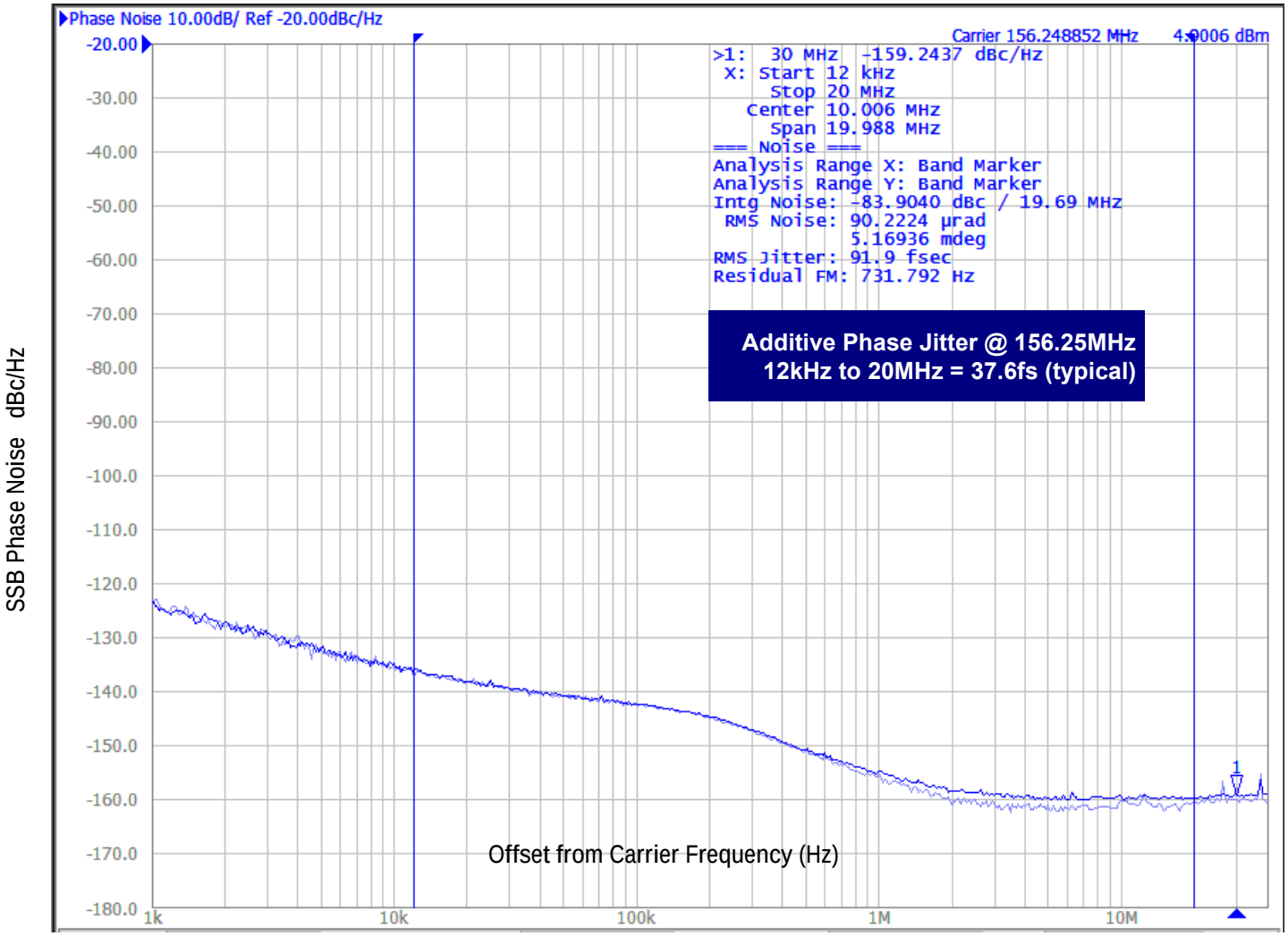
[o] Measured at 100MHz.

[p] Measured for the following frequencies: 25MHz, 100MHz, 125MHz, 156.25MHz, 312.5MHz, 400MHz, 644.5313MHz, and 750MHz.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise.* This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

Figure 1. Additive Phase Jitter



As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

The additive phase jitter for this device was measured using a Renesas Clock Driver 8T49NS010 as an input source and Agilent E5052 phase noise analyzer.

Applications Information

Recommendations for Unused Input and Output Pins

Inputs

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, 1kΩ resistors can be tied from CLK to ground and nCLK to V_{DD}.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs

LVCMOS Output (REFOUT)

If LVCMOS output is not used, then disable the output and it can be left floating.

LVPECL and HCSL Outputs

All unused output pairs can be left floating. We recommend that there is no trace attached.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

Crystal Input Interface

The 8T39204 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in Figure 2 were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. In addition, the recommended 12pF parallel resonant crystal tuning is shown in Figure 3.The optimum C1 and C2 values can be slightly adjusted for different board layouts.

Figure 2. Crystal Input Interface

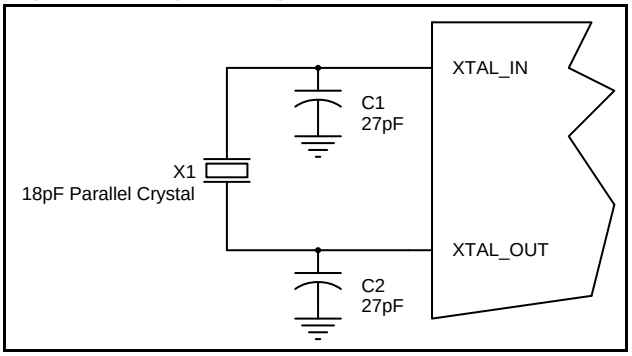
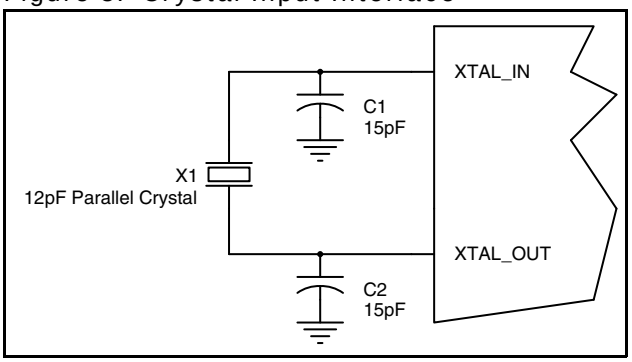


Figure 3. Crystal Input Interface



Power-up Ramp Sequence

This device has multiple supply pins dedicated for different blocks. Output power supplies V_{DDOx} (V_{DDOA}, V_{DDOB}, V_{DDOREF}) must ramp up before, or concurrently with core power supply V_{DD}. All power supplies must ramp up in a linear fashion and monotonically.

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 4 shows an example of the interface diagram for a high speed 3.3V LVCMOS driver.

This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Figure 5 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

Figure 4. LVCMOS Driver to XTAL Input Interface

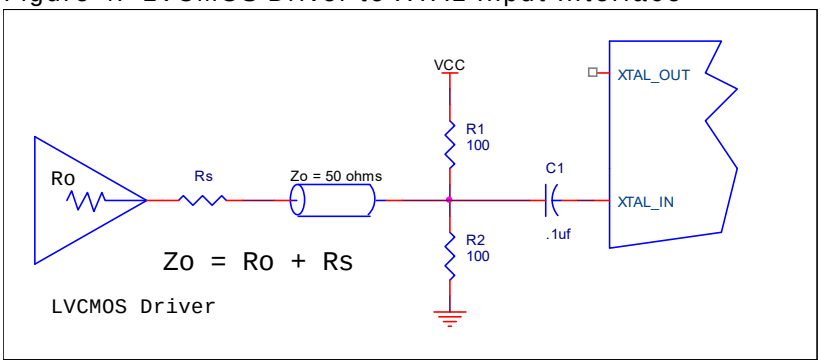
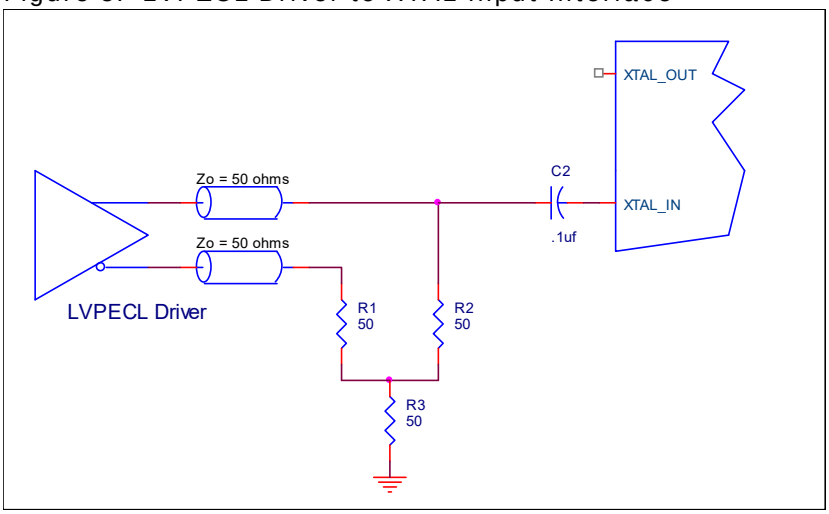


Figure 5. LVPECL Driver to XTAL Input Interface

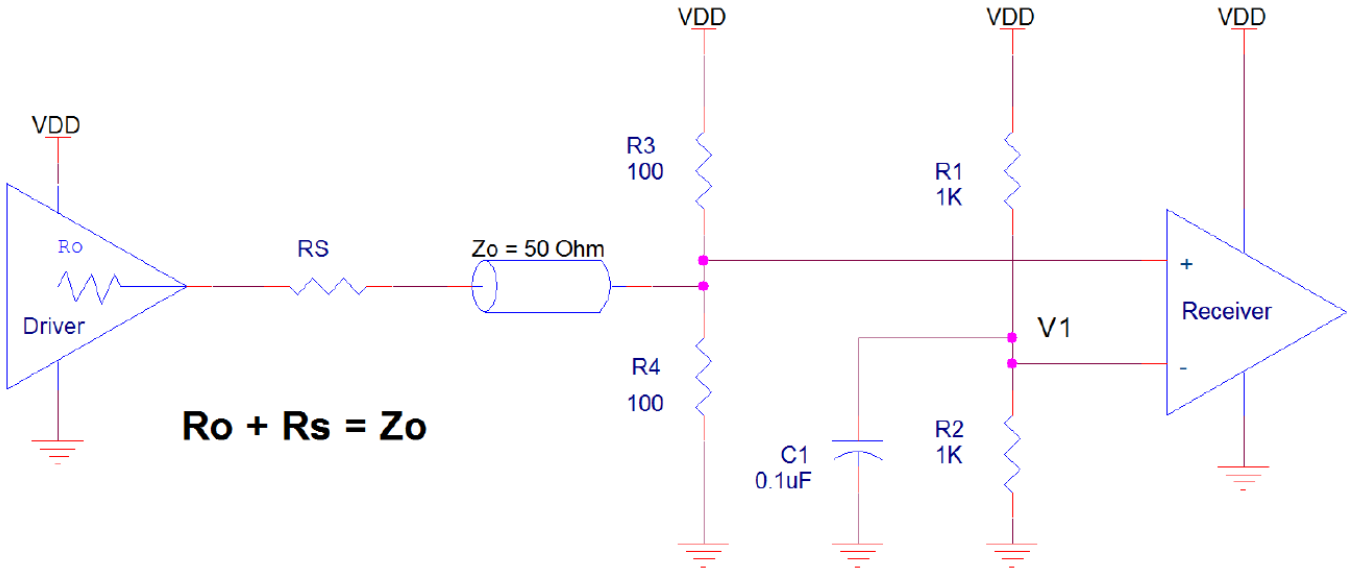


Wiring the Differential Input to Accept Single-Ended Levels

Figure 6 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

Figure 6. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels



3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HSTL and other differential signals. Both differential inputs must meet the V_{PP} and V_{CMR} input requirements. Figure 7 to Figure 11 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 7, the input termination applies for Renesas open emitter HSTL drivers. If you are using an HSTL driver from another vendor, use their termination recommendation.

Figure 7. CLK/nCLK Input Driven by an Renesas Open Emitter HSTL Driver

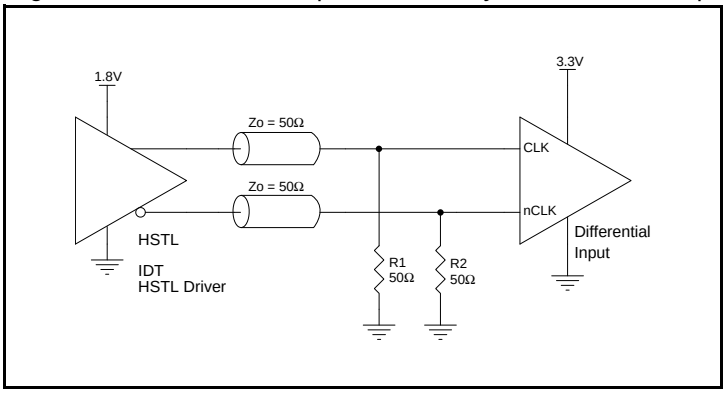


Figure 8. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

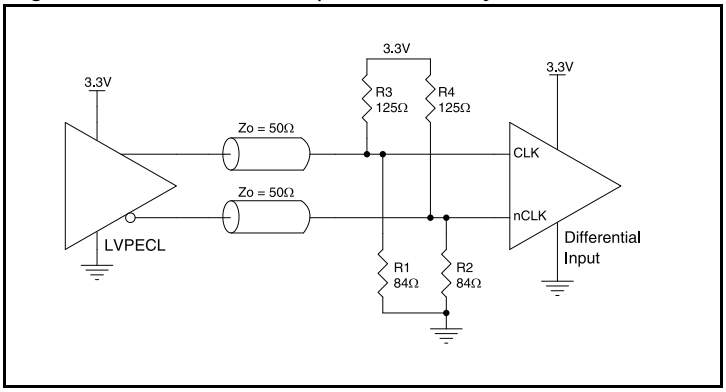


Figure 9. CLK/nCLK Input Driven by an Renesas Open Collector CML Driver

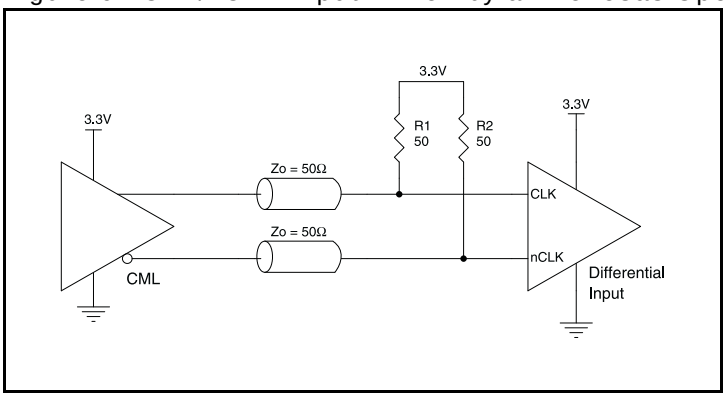


Figure 10. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

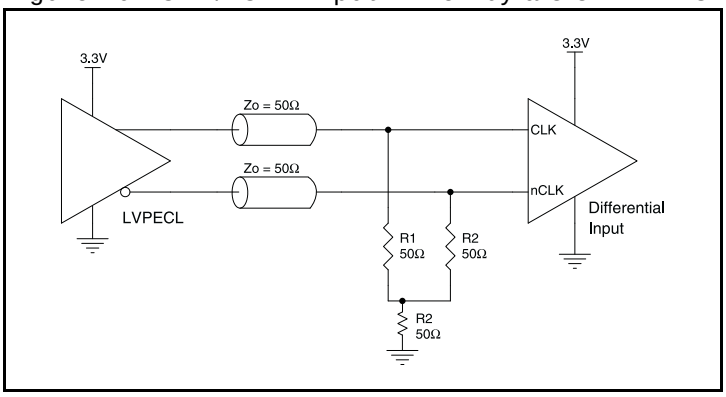
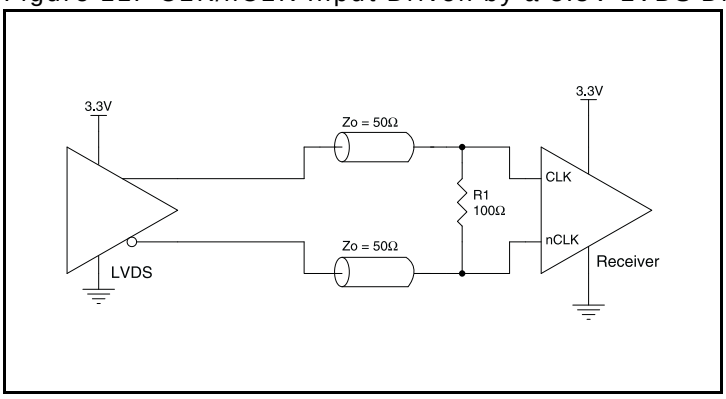


Figure 11. CLK/nCLK Input Driven by a 3.3V LVDS Driver



2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figure 12 to Figure 16 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 12, the input termination applies for Renesas open emitter HSTL drivers. If you are using an HSTL driver from another vendor, use their termination recommendation.

Figure 12. CLK/nCLK Input Driven by an Renesas Open Emitter HSTL Driver

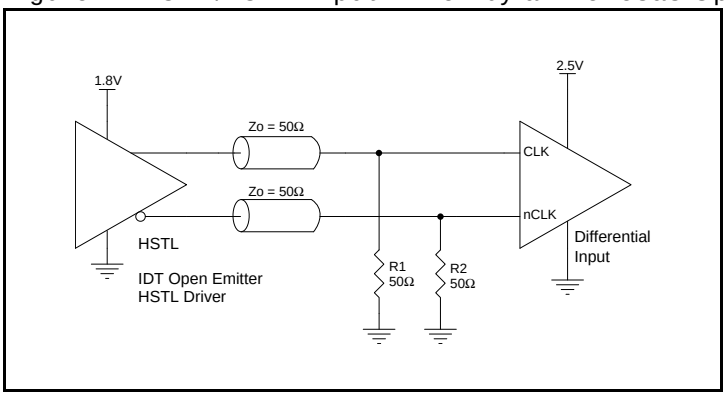


Figure 13. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

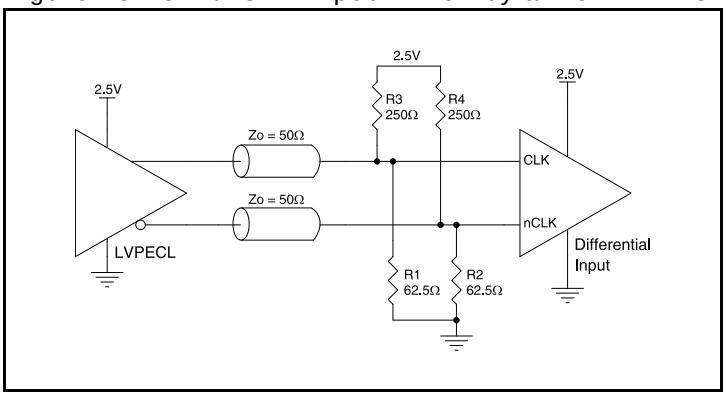


Figure 14. CLK/nCLK Input Driven by a 2.5V LVDS Driver

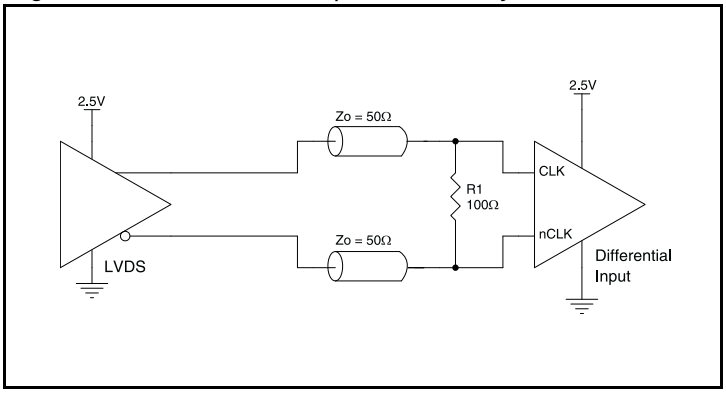


Figure 15. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

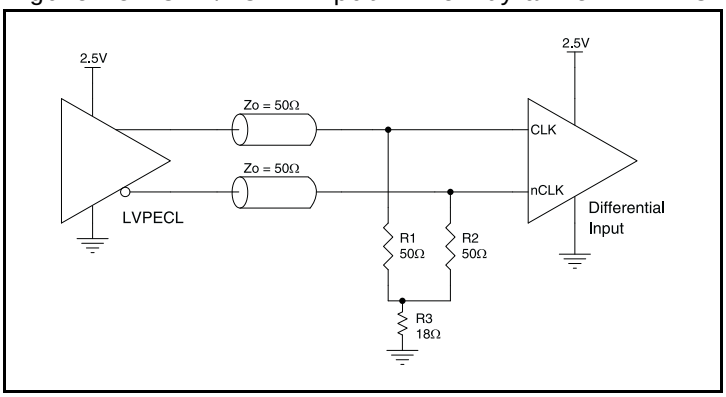
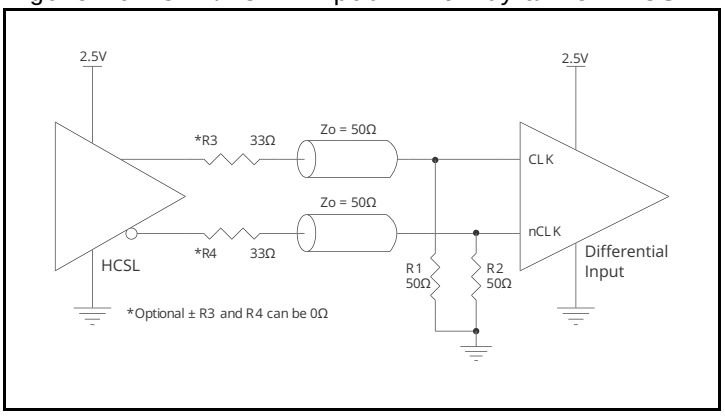


Figure 16. CLK/nCLK Input Driven by a 2.5V HCSL Driver



LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. Renesas offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 17 can be used with either type of output structure. Figure 18, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact Renesas and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

Figure 17. Standard Termination

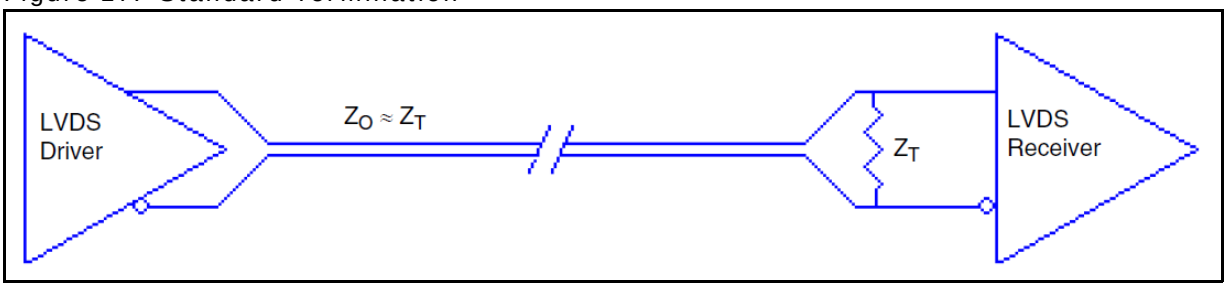
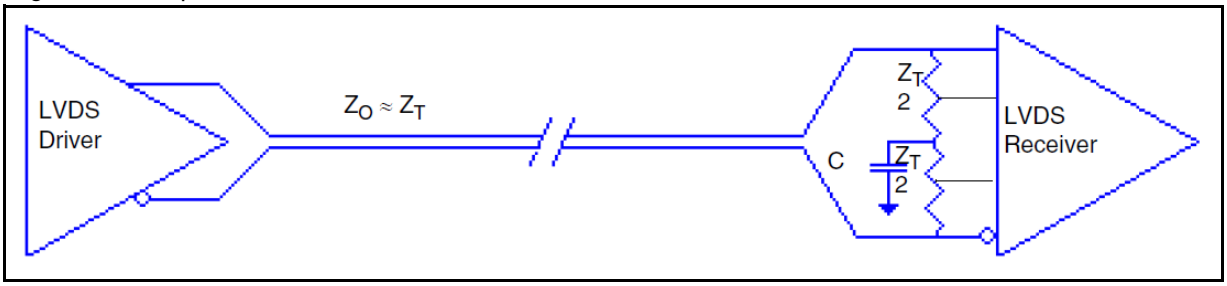


Figure 18. Optional Termination



Termination for 3.3V LVPECL Outputs

The clock topology shown below is a typical termination for LVPECL outputs. The two different terminations mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figure 19. 3.3V LVPECL Output Termination

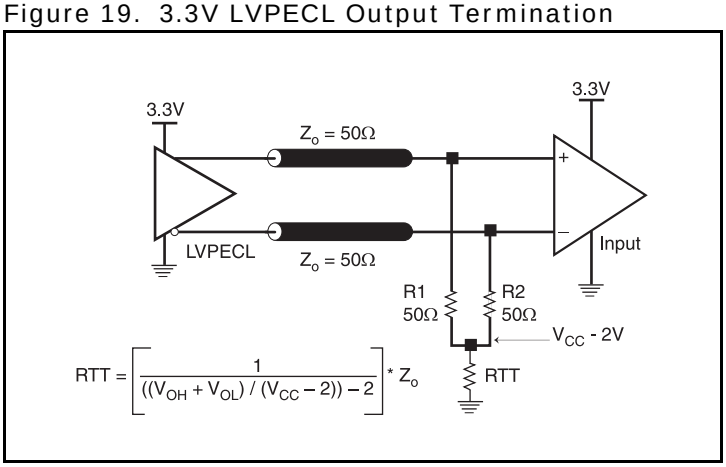
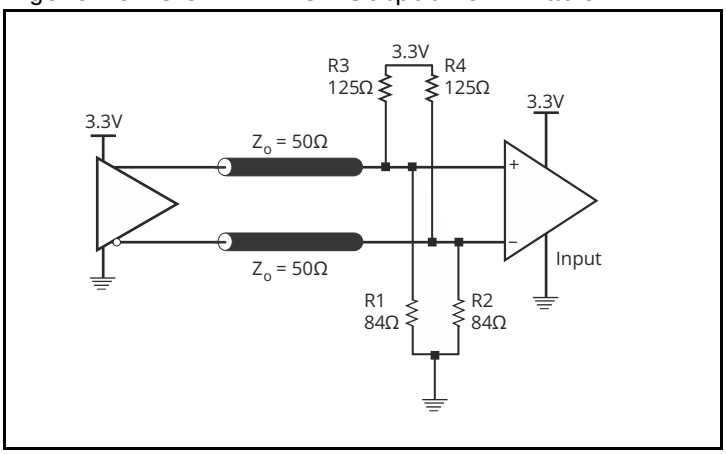


Figure 20. 3.3V LVPECL Output Termination



Termination for 2.5V LVPECL Outputs

Figure 21 and Figure 22 show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{DDO} – 2V. For V_{DDO} = 2.5V, the V_{DDO} – 2V is very close to ground level. The R3 in Figure 22 can be eliminated and the termination is shown in Figure 23.

Figure 21. 2.5V LVPECL Driver Termination Example

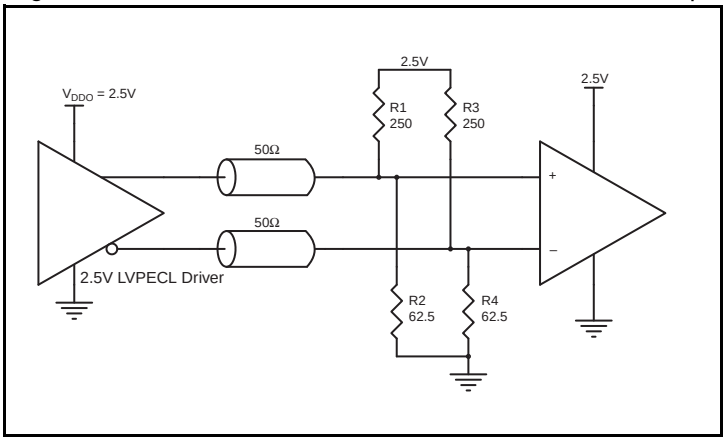


Figure 22. 2.5V LVPECL Driver Termination Example

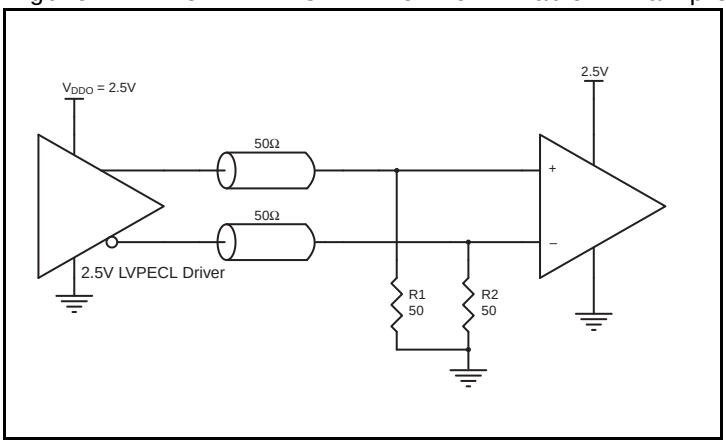
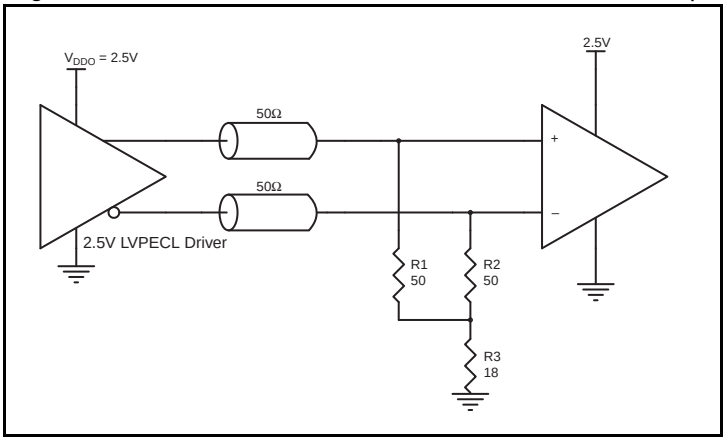


Figure 23. 2.5V LVPECL Driver Termination Example



Recommended Termination

Figure 24 is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

Figure 24. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

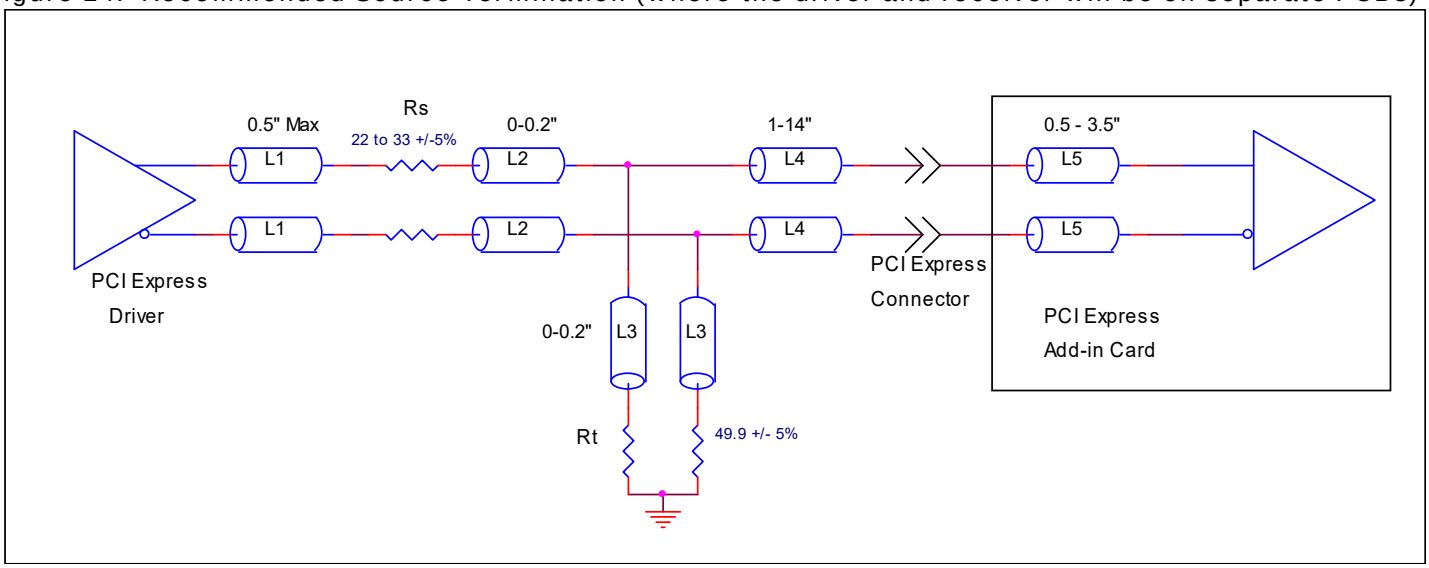
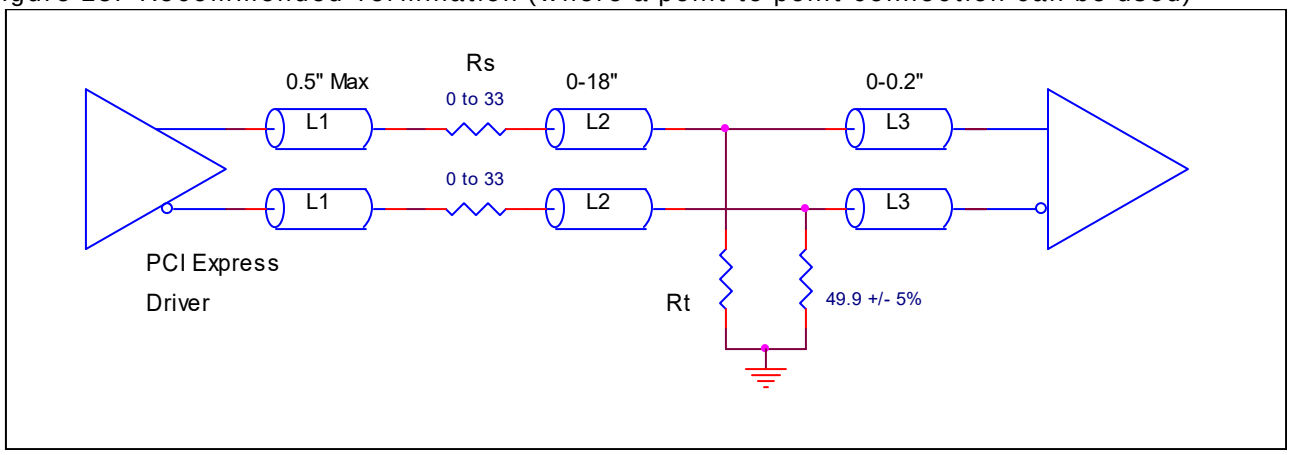


Figure 25 is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

Figure 25. Recommended Termination (where a point-to-point connection can be used)

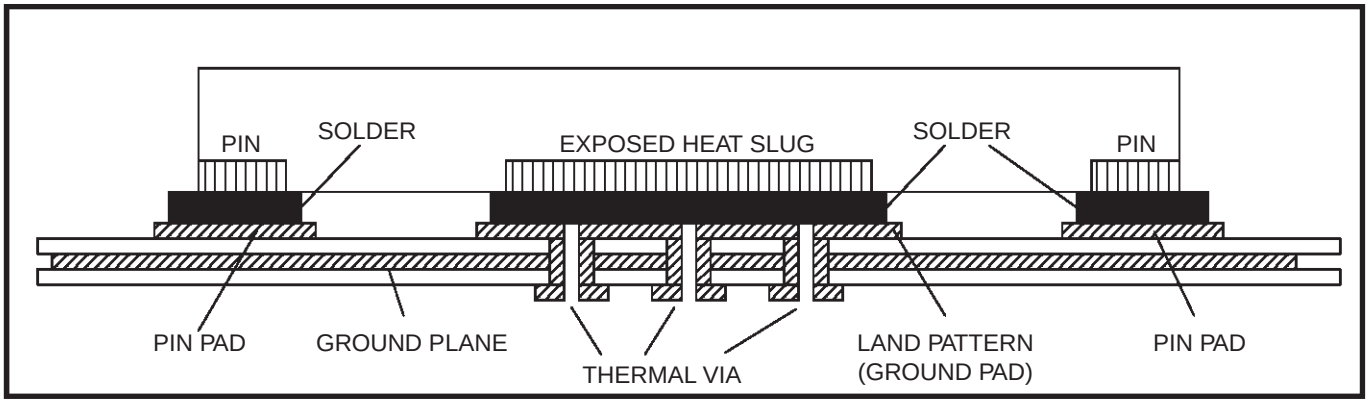


VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 26. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

Figure 26. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)



LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the 8T39204.
Equations and example calculations are also provided.

1.Power Dissipation.

The total power dissipation for the 8T39204 is the sum of the core power plus the power dissipated due to outputs switching.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

I_{EE_MAX} = 159.17mA.

- Power $(core)_{MAX} = I_{EE\_MAX} * V_{DD\_MAX}$ = 3.465V * 159.17mA = 551.52mW
- Power $(outputs)_{MAX}$ = 32mW/Loaded Output pair

If all outputs are loaded, the total power is 4 * 32mW = 128mW

Max LVPECL Power Dissipation = 551.52mW + 128mW = 679.52mW

LVCMOS Output Power Dissipation

- Static Power Dissipation:
  Power $(static)_{MAX} = V_{DDOREF\_MAX} * I_{DDREF\_MAX}$ = 3.465V * 2mA = 6.93mW
  (I_{DDREF_MAX} = 2mA)
- Dynamic Power Dissipation at 250MHz:
  Power $(Dynamic)_{MAX} = C_{PD} * F_{MAX} * N * V_{DDOREF}^2$ = 5.0pF * 250MHz * 1 * 3.465^2 = 15.01mW
- LVCMOS Power Dissipation = 6.93mW + 15.01mW = 21.938mW

Total Power Dissipation = 679.52mW + 21.938mW = 701.46mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37.88°C/W per Table 23. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.701W * 37.88°C/W = 111.57°C. This is below the limit of 125°C.

LVPECL Power Considerations (Application Frequency 156.25MHz)

This section provides information on power dissipation and junction temperature for the 8T39204.
Equations and example calculations are also provided.

1.Power Dissipation.

The total power dissipation for the 8T39204 is the sum of the core power plus the power dissipated due to outputs switching.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

I_{EE_MAX} = 101.35mA.

- Power $(core)_{MAX} = I_{EE\_MAX} * V_{DD\_MAX}$ = 3.465V * 101.35mA = 351.16mW
- Power $(outputs)_{MAX}$ = 32mW/Loaded Output pair

If all outputs are loaded, the total power is 4 * 32mW = 128mW

Max LVPECL Power Dissipation = 351.16mW + 128mW = 479.16mW

LVCMOS Output Power Dissipation

- Static Power Dissipation:
  Power $(static)_{MAX} = V_{DDOREF\_MAX} * I_{DDREF\_MAX}$ = 3.465V * 2mA = 6.93mW
  (I_{DDREF_MAX} = 2mA)
- Dynamic Power Dissipation at 250MHz:
  Power $(Dynamic)_{MAX} = C_{PD} * F_{MAX} * N * V_{DDOREF}^2$ = 5.0pF * 156.25MHz * 1 * 3.465^2 = 9.34mW
- LVCMOS Power Dissipation = 6.93mW + 9.34mW = 16.31mW

Total Power Dissipation = 479.16mW + 16.31mW = 495.47mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37.88°C/W per Table 23. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.495W * 37.88°C/W = 103.77°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

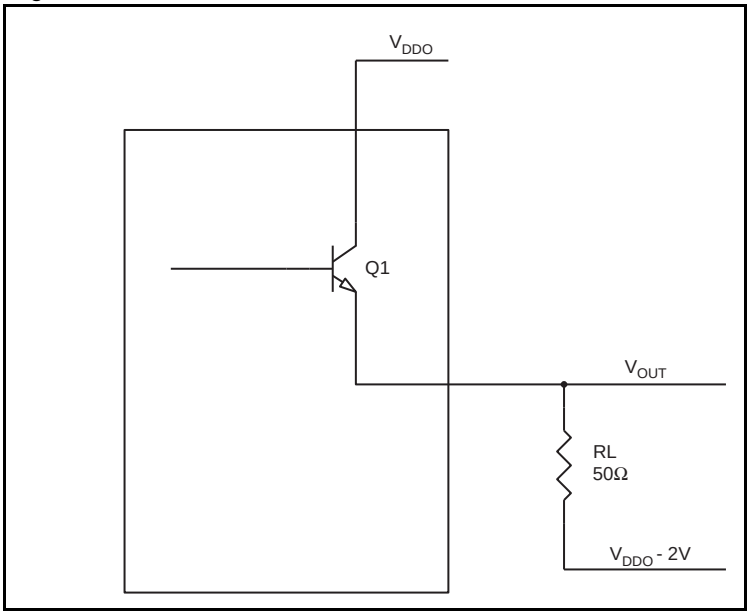
Table 23. Thermal Resistance θ_{JA} for 32-Lead VFQFN

Symbol	Parameter		Value	Unit
θ_{JA}	Theta J_A, Junction to Ambient Air Thermal Coefficient	0m/s air flow	37.88	°C/W
		1m/s air flow	34.35	
		2m/s air flow	32.8	
θ_{JB}	Theta J_B, Junction to Board Thermal Coefficient		2.876	°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs. LVPECL output driver circuit and termination are shown in Figure 27.

Figure 27. LVPECL Driver Circuit and Termination



To calculate power dissipation due to outputs switching, use the following equations which assume a 50Ω load, and a termination voltage of V_{DDO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{DDO\_MAX} – 0.8V$
  $(V_{DDO\_MAX} – V_{OH\_MAX}) = 0.8V$
- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{DDO\_MAX} – 1.6V$
  $(V_{DDO\_MAX} – V_{OL\_MAX}) = 1.6V$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{DDO\_MAX} – 2V))/R_L] * (V_{DDO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{DDO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{DDO\_MAX} – V_{OH\_MAX}) = [(2V – 0.8V)/50Ω] * 0.8V = 19.80mW$

$Pd\_L = [(V_{OL\_MAX} – (V_{DDO\_MAX} – 2V))/R_L] * (V_{DDO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{DDO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{DDO\_MAX} – V_{OL\_MAX}) = [(2V – 1.6V)/50Ω] * 1.6V = 12.8mW$

Total Power Dissipation per output pair = Pd_H + Pd_L = 32mW

LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the 8T39204.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8T39204 is the sum of the core power plus the power dissipated due to outputs switching.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

I_{DD_MAX} = 36mA

I_{DDO_MAX} = 110mA

- Maximum LVDS Power Dissipation = V_{DD_MAX} * (I_{DD_MAX} + I_{DDO_MAX}) = 3.465V * (36mA + 110mA) = 506.18mW

LVCMOS Output Power Dissipation

- Static Power Dissipation:
  Power (static)$_{\_MAX}$ = V_{DDOREF_MAX} * I_{DDREF_MAX} = 3.465V * 2mA = 6.93mW
  (I_{DDREF_MAX} = 2mA)
- Dynamic Power Dissipation at 250MHz:
  Power (Dynamic)$_{\_MAX}$ = C_{PD} * f_{MAX} * N * V_{DDOREF}^2 = 5.0pF * 250MHz * 1 * 3.465^2 = 15.01mW
- LVCMOS Power Dissipation = 6.93mW + 15.01mW = 21.94mW

Total Power Dissipation = 506.18mW + 21.94mW = 528.12mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37.88°C/W per Table 23. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.528W * 37.88°C/W = 105.01°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

LVDS Power Considerations (Application Frequency 156.25MHz)

This section provides information on power dissipation and junction temperature for the 8T39204.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8T39204 is the sum of the core power plus the power dissipated due to outputs switching.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

I_{DD_MAX} = 36mA

I_{DDO_MAX} = 70mA

- Maximum LVDS Power Dissipation = V_{DD_MAX} * (I_{DD_MAX} + I_{DDO_MAX}) = 3.465V * (36mA + 70mA) = 368.1mW

LVCMOS Output Power Dissipation

- Static Power Dissipation:
  Power (static)$_{\_MAX}$ = V_{DDOREF_MAX} * I_{DDREF_MAX} = 3.465V * 2mA = 6.93mW
  (I_{DDREF_MAX} = 2mA)
- Dynamic Power Dissipation at 156.25MHz:
  Power (Dynamic)$_{\_MAX}$ = C_{PD} * f_{MAX} * N * V_{DDOREF}^2 = 5.0pF * 156.25MHz * 1 * 3.465^2 = 9.34mW
- LVCMOS Power Dissipation = 6.93mW + 9.34mW = 16.31mW

Total Power Dissipation = 368.1mW + 16.31mW = 384.41mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37.88°C/W per Table 23. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.384W * 37.88°C/W = 99.56°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

HCSL Power Considerations

This section provides information on power dissipation and junction temperature for the 8T39204.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8T39204 is the sum of the core power plus the power dissipated due to outputs switching.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

I_{DD_MAX} = 37mA

I_{DDO_MAX} = 66mA (application frequency = 750MHz)

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + $I_{DDO\_MAX)}$ = 3.465V * (37mA + 66mA) = 356.90mW
- Power (outputs)$_{MAX}$ = 44.5mW/Loaded Output pair

If all outputs are loaded, the total power is 4 * 44.5mW = 178mW

Max HCSL Power Dissipation = 356.90mW + 178mW = 534.90mW

LVCMOS Output Power Dissipation

- Static Power Dissipation:
  Power (static)$_{\_MAX}$ = V_{DDOREF_MAX} * I_{DDREF_MAX} = 3.465V * 2mA = 6.93mW
  (I_{DDREF_MAX} = 2mA)
- Dynamic Power Dissipation at 250MHz:
  Power (Dynamic)$_{\_MAX}$ = C_{PD} * f_{MAX} * N * V_{DDOREF}^2 = 5.0pF * 250MHz * 1 * 3.465^2 = 15.01mW
- LVCMOS Power Dissipation = 6.93mW + 15.01mW = 21.938mW

Total Power Dissipation = 534.90mW + 21.938mW = 556.83mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37.88°C/W per Table 23. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.557W * 37.88°C/W = 107°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

HCSL Power Considerations (Application Frequency 156.25MHz)

This section provides information on power dissipation and junction temperature for the 8T39204.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8T39204 is the sum of the core power plus the power dissipated due to outputs switching.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

I_{DD_MAX} = 36mA

I_{DDO_MAX} = 33mA (application frequency = 156.25MHz)

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDO_MAX}) = 3.465V * (36mA + 33mA) = 239.33mW
- Power (outputs)$_{MAX}$ = 44.5mW/Loaded Output pair

If all outputs are loaded, the total power is 4 * 44.5mW = 178mW

Max HCSL Power Dissipation = 239.33mW + 178mW = 417.33mW

LVCMOS Output Power Dissipation

- Static Power Dissipation:
  Power (static)$_{MAX}$ = V_{DDOREF_MAX} * I_{DDREF_MAX} = 3.465V * 2mA = 6.93mW
  (I_{DDREF_MAX} = 2mA)
- Dynamic Power Dissipation at 156.25MHz:
  Power (Dynamic)$_{MAX}$ = C_{PD} * f_{MAX} * N * V_{DDOREF}^2 = 5.0pF * 156.25MHz * 1 * 3.465^2 = 9.38mW
- LVCMOS Power Dissipation = 6.93mW + 9.38mW = 16.31mW

Total Power Dissipation = 417.3mW + 16.31mW = 433.64mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37.88°C/W per Table 23. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

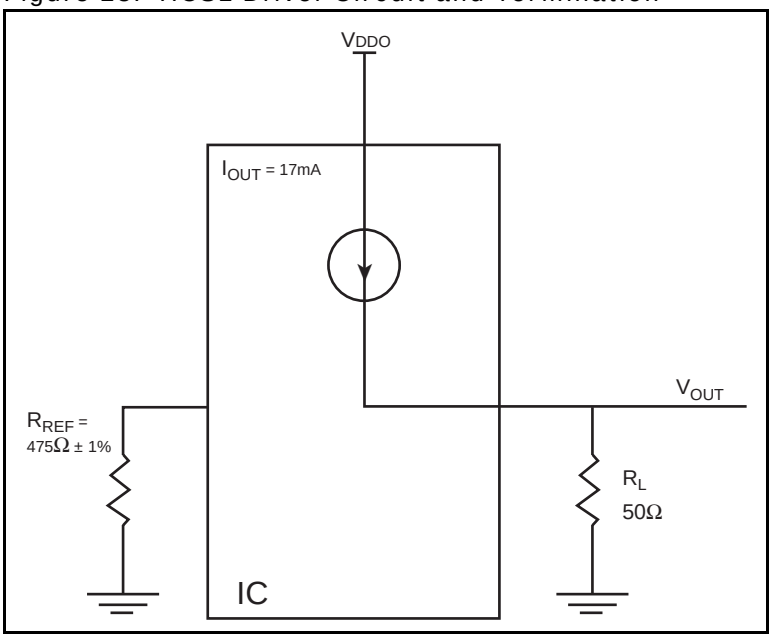
85°C + 0.434W * 37.88°C/W = 101.43°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair. HCSL output driver circuit and termination are shown in Figure 28.

Figure 28. HCSL Driver Circuit and Termination



HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DDO_MAX}.

Power= $(V_{DDO\_MAX} - V_{OUT}) * I_{OUT}$,
since $V_{OUT} - I_{OUT} * R_L$

$= (V_{DDO\_MAX} - I_{OUT} * R_L) * I_{OUT}$

$= (3.465V - 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = 44.5mW

Reliability Information

See Table 23.

Transistor Count

The transistor count for 8T39204 is 8654.

Package Outline Drawings

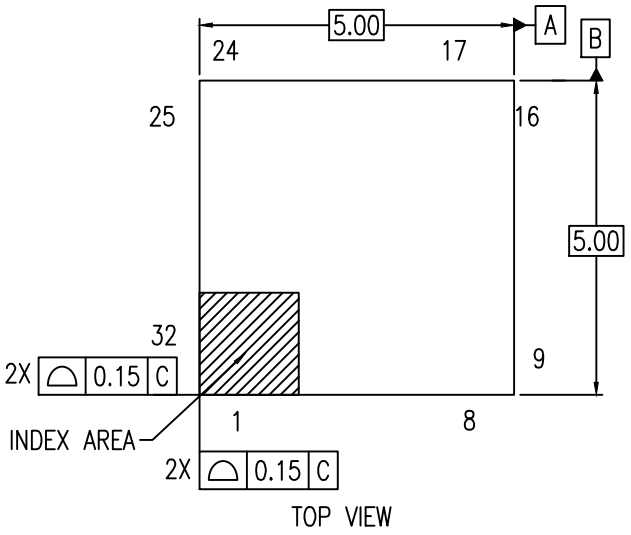
The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

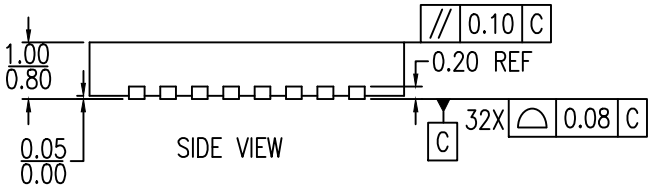
Orderable Part Number	Marking	Package Description	Carrier Type	Temperature Range
8T39204NLGI	IDT8T39204NLGI	32-VFQFPN, Lead-Free	Tray	-40°C to 85°C
8T39204NLGI8	IDT8T39204NLGI	32-VFQFPN, Lead-Free	Tape & Reel	-40°C to 85°C

Revision History

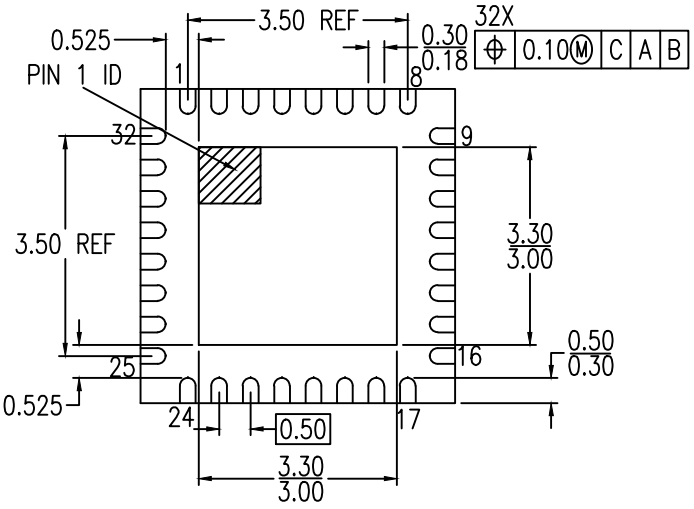
Revision Date	Description of Change
February 22, 2021	▪ Updated footnote [p] in Table 20, Table 21, and Table 22
February 19, 2021	▪ Increased maximum frequency for HCSL output
December 16, 2019	▪ Completed minor updates to Figure 16 and Figure 20. ▪ Linked the package outline drawings to the document; however, no technical changes ▪ Updated the ordering information
November 22, 2019	Initial release.



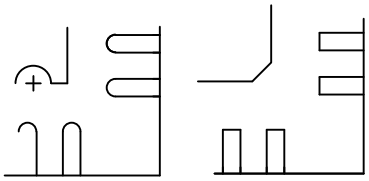
TOP VIEW



SIDE VIEW

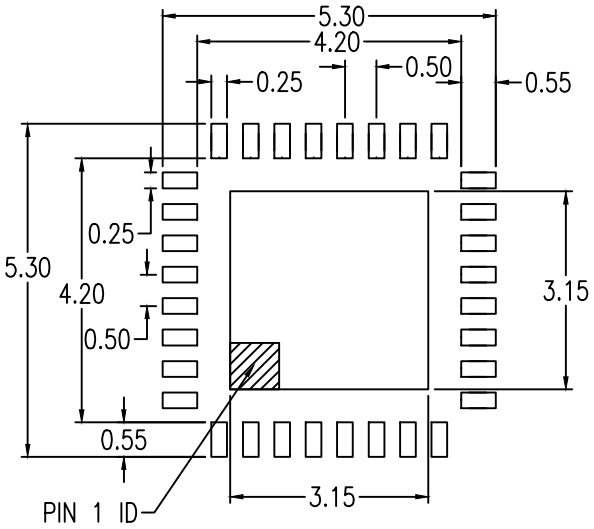


BOTTOM VIEW



PIN #1 ID OPTION

NOTE:
1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. COPLANARITY APPLIE TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 MM.
3. WARPAGE SHALL NOT EXCEED 0.10 MM.
4. PIN LOCATION IS UNDENTIFIED BY EITHER CHAMFER OR NOTCH.



RECOMMENDED LAND PATTERN DIMENSION

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
April 12, 2018	Rev 02	New Format
Feb 8, 2016	Rev 01	Added "k: Value

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