

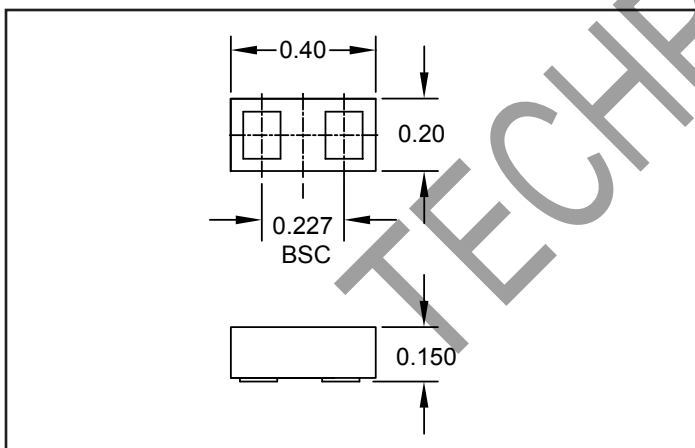
Description

ESD5V0 TVS diodes are designed to protect sensitive electronics from damage or latch-up due to ESD. They are designed to replace 01005 size multilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and other portable electronics. TVS diodes offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

ESD5V0B5-01005 features extremely good ESD protection characteristics highlighted by low dynamic resistance, low peak ESD clamping voltage, and high ESD withstand voltage (+/-15kV contact per IEC 61000-4-2). Low typical capacitance (6.5pF at VR=0V) minimizes loading on sensitive circuits. Each device will protect one data or power line operating at 5 Volts.

ESD5V0B5-01005 is in a 2-pin SLP0402P2X4F package measuring 0.4 x 0.2 mm with a nominal height of only 0.15mm. Leads are finished with NiAu. The small package gives the designer the flexibility to protect single lines in applications where arrays are not practical. The combination of small size and high ESD surge capability makes them ideal for use in portable applications such as cellular phones and wearables.

Package Dimension



Features

- High ESD withstand voltage: +/-15kV (contact) and +/-15kV (air) per IEC 61000-4-2
- Ultra-small 01005 package
- Protects one line
- Low ESD clamping voltage
- Working voltage: 5V
- Capacitance: 6.5pF Typical
- Low leakage current
- Low dynamic resistance
- Solid-state silicon-avalanche technology



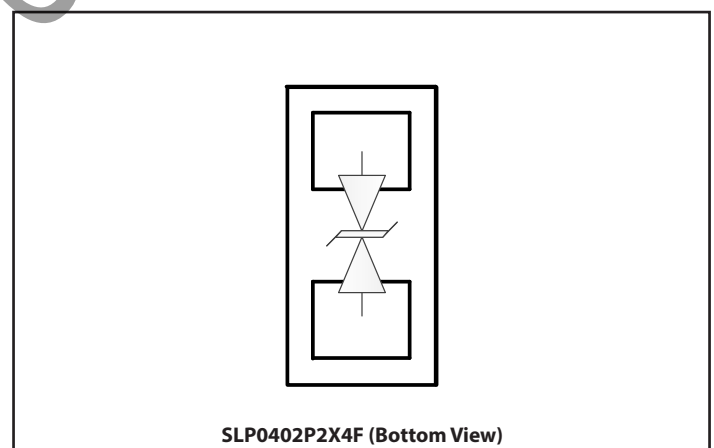
Mechanical Characteristics

- SLP0402P2X4F package
- Pb-Free, Halogen Free, RoHS/WEEE compliant
- Nominal Dimensions: 0.4 x 0.2 x 0.15 mm
- Lead Finish: NiAu
- Marking: Marking code
- Packaging: Tape and Reel

Applications

- Cellular Handsets & Accessories
- Keypads, Side Keys, Audio Ports
- Portable Instrumentation
- Notebook Computers
- Tablet PC

Schematic & Pin Configuration



Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 1.2/50μs)	P_{PK}	30	W
Peak Pulse Current (tp = 1.2/50μs)	I_{PP}	2	A
ESD per IEC 61000-4-2 (Air) ⁽¹⁾ ESD per IEC 61000-4-2 (Contact) ⁽¹⁾	V_{ESD}	±15 ±15	kV
Operating Temperature	T_J	-40 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

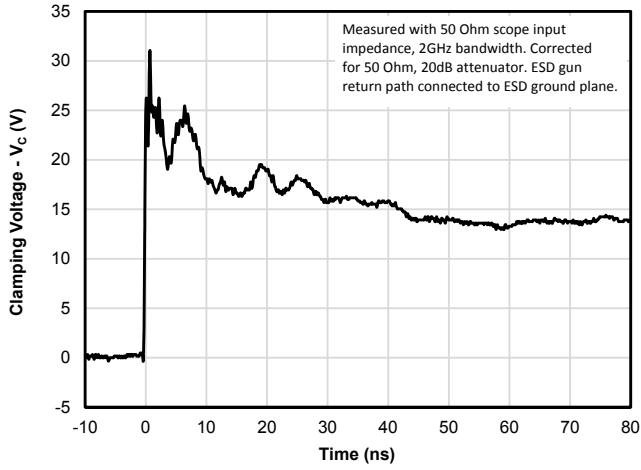
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	T = -40 to +125			5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	6.5	8	9.5	V
Reverse Leakage Current	I_R	$V_{RWM} = 5V$		5	25	nA
Clamping Voltage	V_C	$I_{PP} = 2A, tp = 8/20\mu s$			15	V
ESD Clamping Voltage ²	V_C	$I = 4A, tlp = 0.2/100ns$		11		V
		$I = 16A, tlp = 0.2/100ns$		18.5		
Dynamic Resistance ^{2,3}	R_{DYN}	$tlp = 0.2/100ns$		0.62		Ω
Junction Capacitance	C_J	$V_R = 0V, f = 1MHz$		6.5	9	pF

Notes

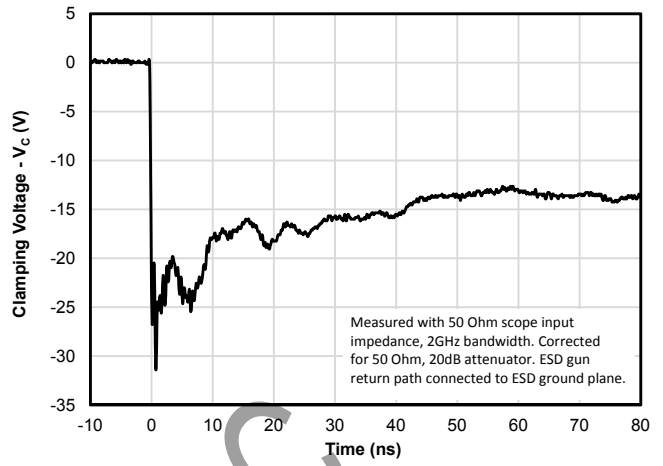
- 1) Measured with a 20dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.
- 2) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t1 = 70ns to t2 = 90ns.
- 3) Dynamic resistance calculated from $I_{TLP} = 4A$ to $I_{TLP} = 16A$

Typical Characteristics

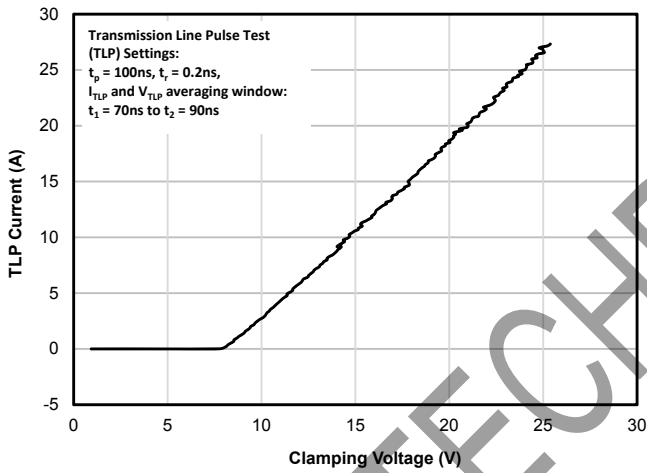
ESD Clamping (8kV Contact per IEC 61000-4-2)



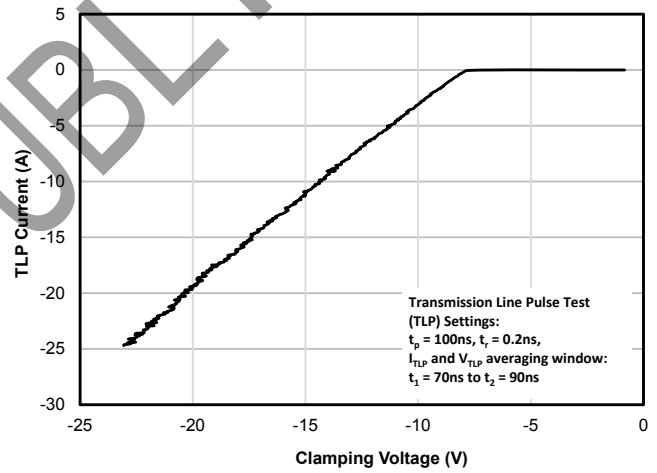
ESD Clamping (-8kV Contact per IEC 61000-4-2)



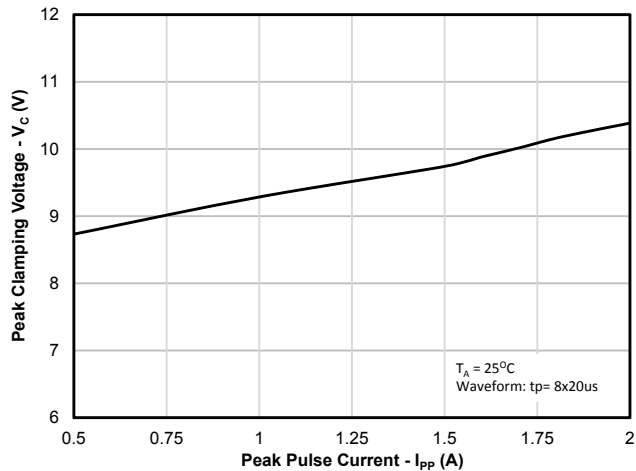
TLP Characteristic (Positive Pulse)



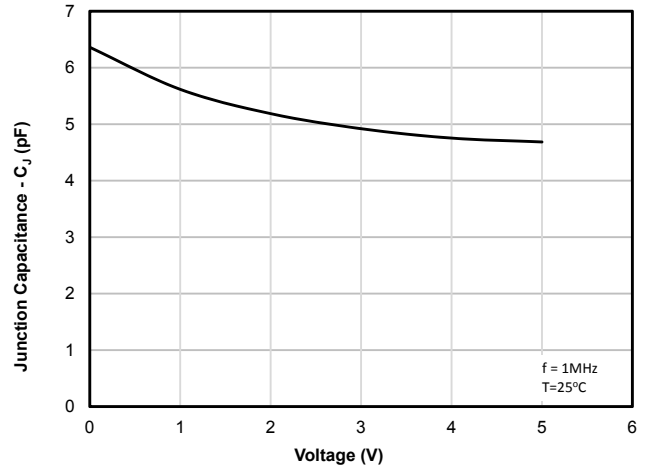
TLP Characteristic (Negative Pulse)



Clamping Characteristic (8/20us Waveform)



Capacitance vs. Reverse Voltage



Application Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable-solder joints. The figure at the right details TECHPUBLIC's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing-parameters will require some experimentation to get the desired solder application. techpublic's recommend edmounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

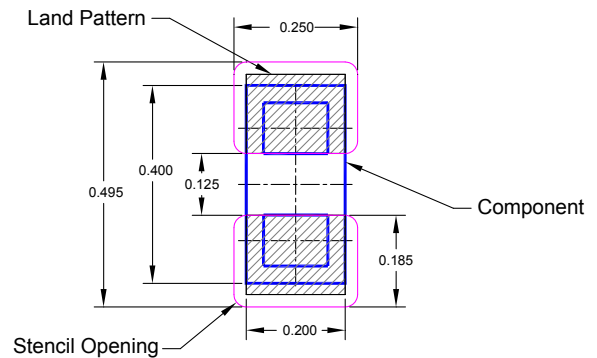
$$\text{Area Ratio} = (L * W) / (2 * (L + W) * T)$$

Where:

- L = Aperture Length
- W = Aperture Width
- T = Stencil Thickness

techpublic recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electro-polishedfinish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. For small pitch components, Semtech recommends a square aperture with rounded corners for consistent solder release. Due to the small aperture size, a solder paste with Type 4 or smaller particles are recommended.

Recommended Mounting Pattern

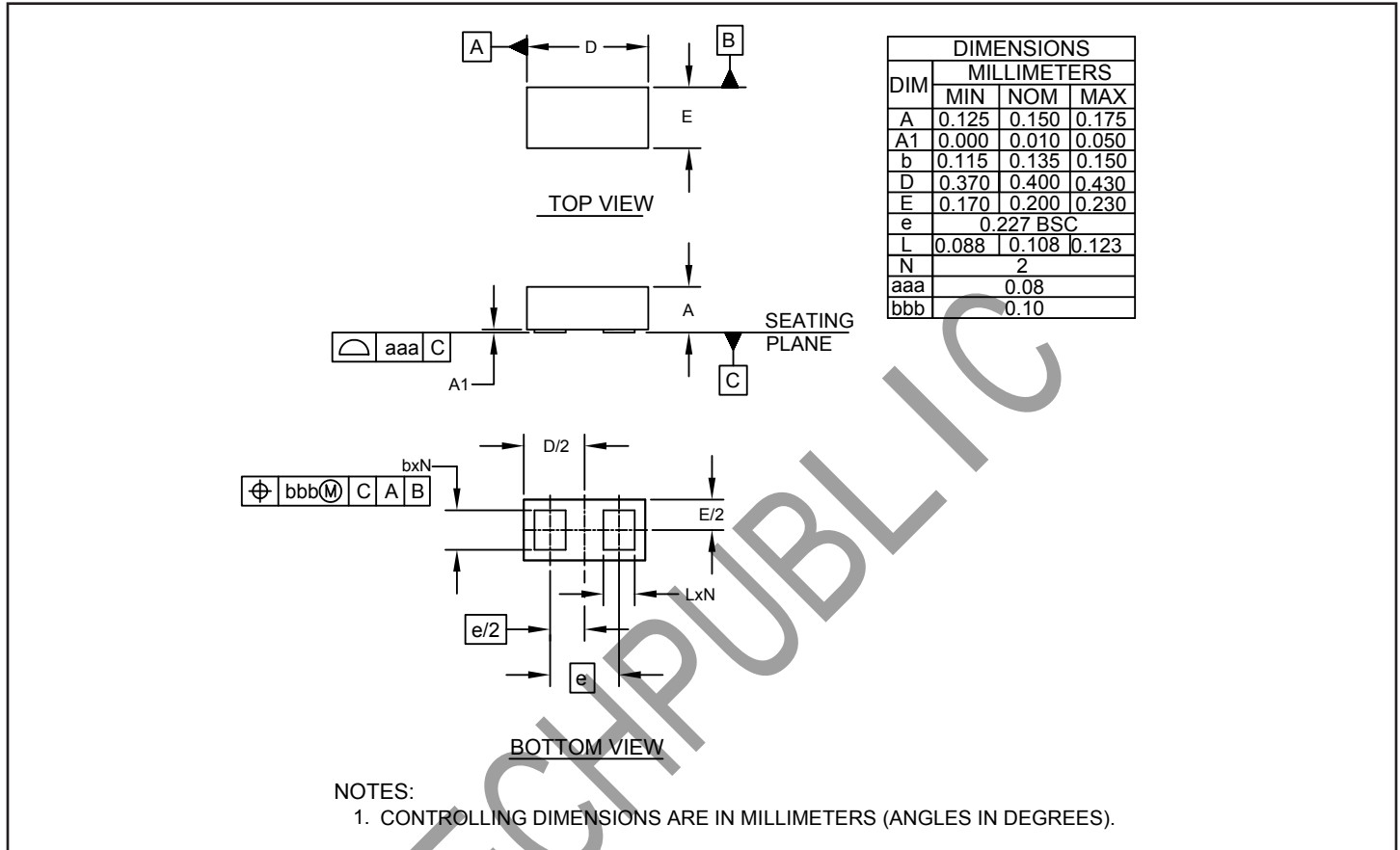


All Dimensions are in mm.

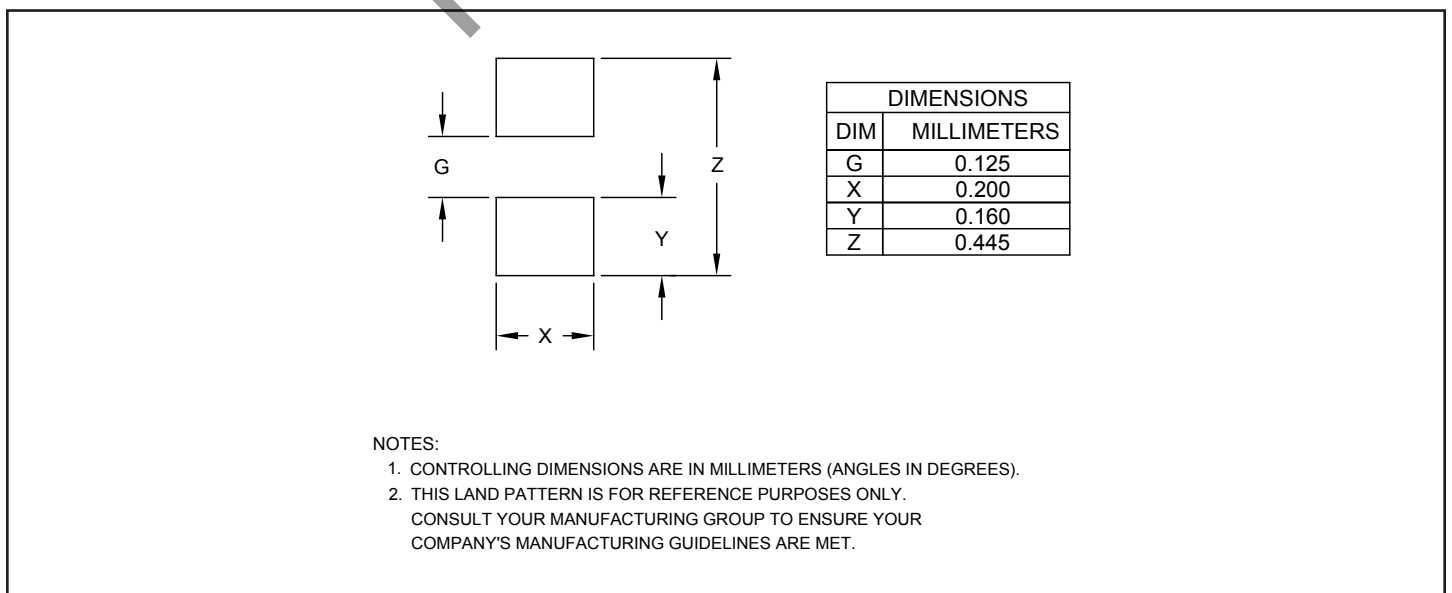
Land Pad.
 Stencil opening
 Component

Assembly Parameter	Recommendation
Solder Stencil Design	Laser cut, Electro-polished
Aperture shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Non-Solder mask defined
PCB Pad Finish	OSP OR NiAu

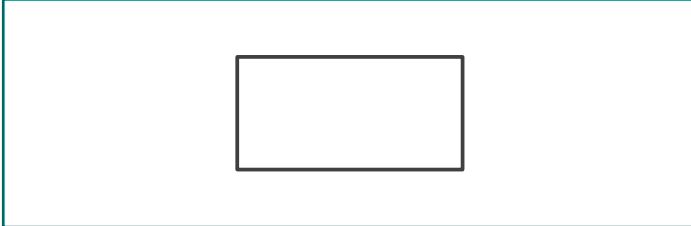
Outline Drawing - SLP0402P2X4F



Land Pattern - SLP0402P2X4F



Marking Code



Tape and Reel Specification

