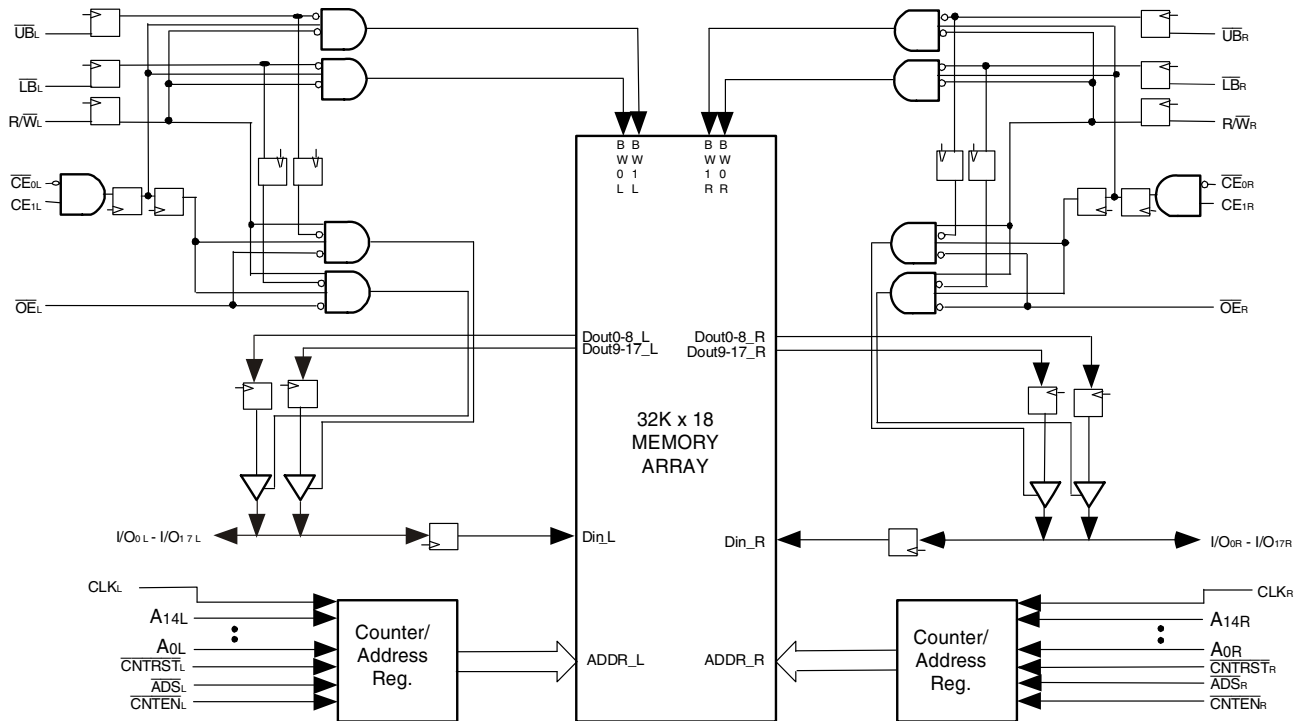


### Features:

- ◆ True Dual-Port memory cells which allow simultaneous access of the same memory location
- ◆ High-speed clock to data access
  - Commercial: 4.2/5/6ns (max.)
  - Industrial: 5ns (max)
- ◆ Pipelined output mode
- ◆ Counter enable and reset features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
  - 7.5ns cycle time, 133MHz operation (9.6 Gbps bandwidth)
  - Fast 4.2ns clock to data out
  - 1.8ns setup to clock and 0.7ns hold on all control, data, and address inputs @ 133MHz

- Data input, address, byte enable and control registers
- Self-timed write allows fast cycle time
- ◆ Separate byte controls for multiplexed bus and bus matching compatibility
- ◆ LVTTTL-compatible, single 3.3V ( $\pm 150\text{mV}$ ) power supply for core
- ◆ LVTTTL-compatible, selectable 3.3V ( $\pm 150\text{mV}$ )/2.5V ( $\pm 125\text{mV}$ ) power supply for I/Os and control signals on each port
- ◆ Industrial temperature range (-40°C to +85°C) is available for selected speeds
- ◆ Available in a 128-pin Thin Quad Plastic Flatpack (TQFP) and 208-pin fine pitch Ball Grid Array, and 256-pin Ball Grid Array
- ◆ Green parts available, see ordering information

### Functional Block Diagram



4833 tbl 01

Description:

The IDT70V3379 is a high-speed 32K x 18 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70V3379 has been optimized for applications having unidirectional or bidirectional data flow

in bursts. An automatic power down feature, controlled by  $\overline{CE}_0$  and  $CE_1$ , permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70V3379 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (VDD) remains at 3.3V.

Pin Configuration<sup>(1,2,3,4)</sup>

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17											
I/O <sub>8L</sub>	NC	V <sub>SS</sub>	NC	NC	NC	A <sub>12L</sub>	A <sub>8L</sub>	NC	V <sub>DD</sub>	CLK <sub>L</sub>	$\overline{CNTEN}_L$	A <sub>4L</sub>	A <sub>0L</sub>	OPT <sub>L</sub>	NC	V <sub>SS</sub>	A										
NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	NC	A <sub>13L</sub>	A <sub>9L</sub>	NC	$\overline{CE}_{0L}$	V <sub>SS</sub>	$\overline{ADS}_L$	A <sub>5L</sub>	A <sub>1L</sub>	V <sub>SS</sub>	V <sub>DDQR</sub>	I/O <sub>8L</sub>	NC	B										
V <sub>DDQL</sub>	I/O <sub>9R</sub>	V <sub>DDQR</sub>	V <sub>DD</sub>	NC	A <sub>14L</sub>	A <sub>10L</sub>	$\overline{UB}_L$	CE <sub>1L</sub>	V <sub>SS</sub>	R/ $\overline{WL}$	A <sub>6L</sub>	A <sub>2L</sub>	V <sub>DD</sub>	I/O <sub>8R</sub>	NC	V <sub>SS</sub>	C										
NC	V <sub>SS</sub>	I/O <sub>10L</sub>	NC	NC	A <sub>11L</sub>	A <sub>7L</sub>	$\overline{LB}_L$	V <sub>DD</sub>	$\overline{OE}_L$	$\overline{CNTFST}_L$	A <sub>3L</sub>	V <sub>DD</sub>	NC	V <sub>DDQL</sub>	I/O <sub>7L</sub>	I/O <sub>7R</sub>	D										
I/O <sub>11L</sub>	NC	V <sub>DDQR</sub>	I/O <sub>10R</sub>	70V3379 BF208 <sup>(5)</sup>  208-Pin fpBGA Top View <sup>(6)</sup>										I/O <sub>6L</sub>	NC	V <sub>SS</sub>	NC	E									
V <sub>DDQL</sub>	I/O <sub>11R</sub>	NC	V <sub>SS</sub>											V <sub>SS</sub>	I/O <sub>6R</sub>	NC	V <sub>DDQR</sub>	F									
NC	V <sub>SS</sub>	I/O <sub>12L</sub>	NC											NC	V <sub>DDQL</sub>	I/O <sub>5L</sub>	NC	G									
V <sub>DD</sub>	NC	V <sub>DDQR</sub>	I/O <sub>12R</sub>											V <sub>DD</sub>	NC	V <sub>SS</sub>	I/O <sub>5R</sub>	H									
V <sub>DDQL</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>											V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DDQR</sub>	J									
I/O <sub>14R</sub>	V <sub>SS</sub>	I/O <sub>13R</sub>	V <sub>SS</sub>											I/O <sub>3R</sub>	V <sub>DDQL</sub>	I/O <sub>4R</sub>	V <sub>SS</sub>	K									
NC	I/O <sub>14L</sub>	V <sub>DDQR</sub>	I/O <sub>13L</sub>											NC	I/O <sub>3L</sub>	V <sub>SS</sub>	I/O <sub>4L</sub>	L									
V <sub>DDQL</sub>	NC	I/O <sub>15R</sub>	V <sub>SS</sub>											V <sub>SS</sub>	NC	I/O <sub>2R</sub>	V <sub>DDQR</sub>	M									
NC	V <sub>SS</sub>	NC	I/O <sub>15L</sub>											I/O <sub>1R</sub>	V <sub>DDQL</sub>	NC	I/O <sub>2L</sub>	N									
I/O <sub>16R</sub>	I/O <sub>16L</sub>	V <sub>DDQR</sub>	NC											NC	NC	A <sub>12R</sub>	A <sub>8R</sub>	NC	V <sub>DD</sub>	CLK <sub>R</sub>	$\overline{CNTEN}_R$	A <sub>4R</sub>	NC	I/O <sub>1L</sub>	V <sub>SS</sub>	NC	P
V <sub>SS</sub>	NC	I/O <sub>17R</sub>	NC											NC	A <sub>13R</sub>	A <sub>9R</sub>	NC	$\overline{CE}_{0R}$	V <sub>SS</sub>	$\overline{ADS}_R$	A <sub>5R</sub>	A <sub>1R</sub>	V <sub>SS</sub>	V <sub>DDQL</sub>	I/O <sub>0R</sub>	V <sub>DDQR</sub>	R
NC	I/O <sub>17L</sub>	V <sub>DDQL</sub>	V <sub>SS</sub>											NC	A <sub>14R</sub>	A <sub>10R</sub>	$\overline{UB}_R$	CE <sub>1R</sub>	V <sub>SS</sub>	R/ $\overline{WR}$	A <sub>6R</sub>	A <sub>2R</sub>	V <sub>SS</sub>	NC	V <sub>SS</sub>	NC	T
V <sub>SS</sub>	NC	V <sub>DD</sub>	NC	NC	A <sub>11R</sub>	A <sub>7R</sub>	$\overline{LB}_R$	V <sub>DD</sub>	$\overline{OE}_R$	$\overline{CNTFST}_R$	A <sub>3R</sub>	A <sub>0R</sub>	V <sub>DD</sub>	OPT <sub>R</sub>	NC	I/O <sub>0L</sub>	U										

4833 drw 02

NOTES:

1. All V<sub>DD</sub> pins must be connected to 3.3V power supply.
2. All V<sub>DDQ</sub> pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V<sub>IH</sub> (3.3V), and 2.5V if OPT pin for that port is set to V<sub>IL</sub> (0V).
3. All V<sub>SS</sub> pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm, with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration<sup>(1,2,3,4)</sup> (con't.)

70V3379  
BC256<sup>(5)</sup>  
BCG256<sup>(5)</sup>

256-Pin BGA  
Top View<sup>(6)</sup>

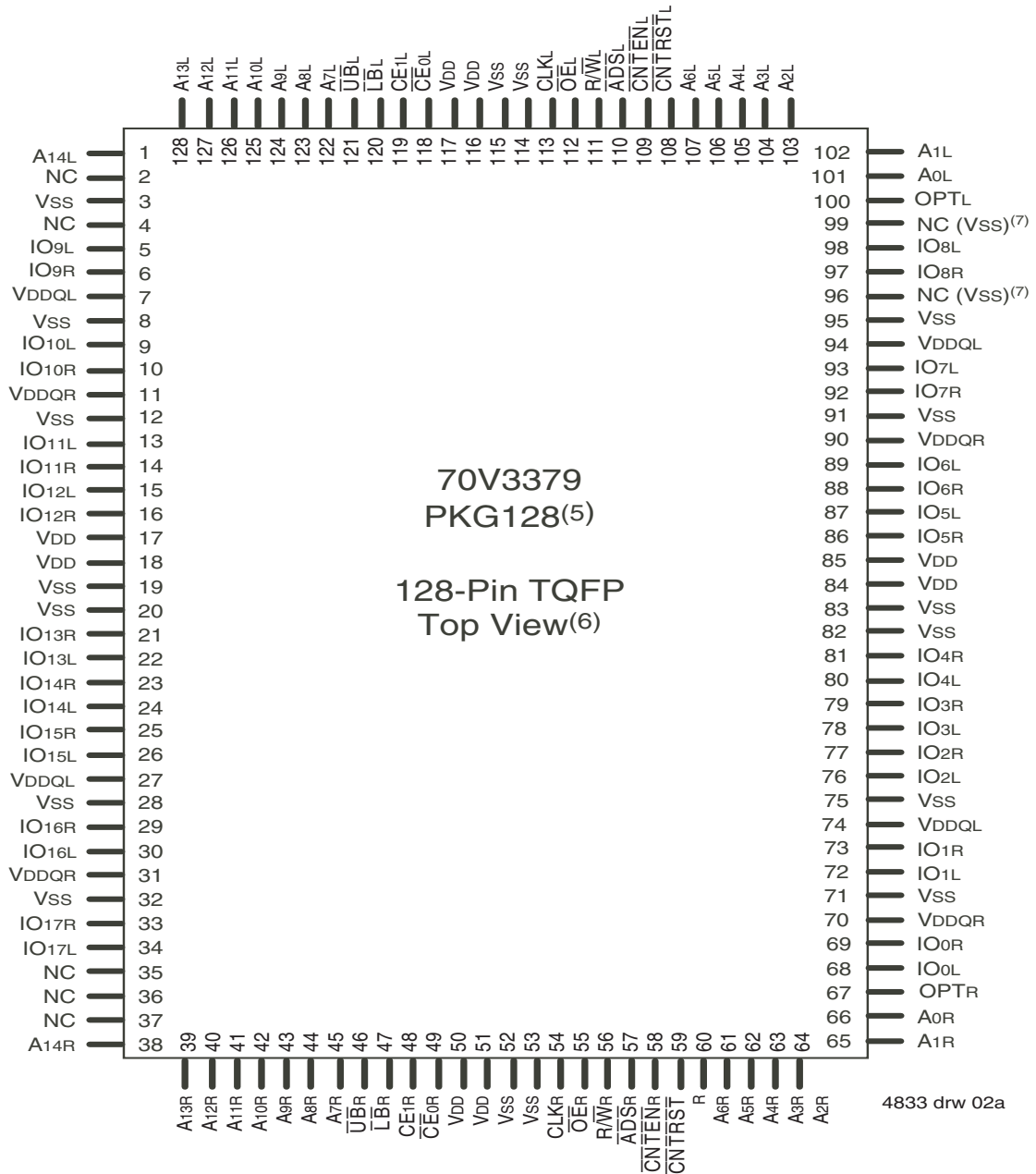
A1 NC	A2 NC	A3 NC	A4 NC	A5 A14L	A6 A11L	A7 A8L	A8 NC	A9 CE1L	A10 OE <sub>L</sub>	A11 CNTEN <sub>L</sub>	A12 A5L	A13 A2L	A14 A0L	A15 NC	A16 NC
B1 NC	B2 NC	B3 NC	B4 NC	B5 NC	B6 A12L	B7 A9L	B8 UB <sub>L</sub>	B9 CE0L	B10 R/W <sub>L</sub>	B11 CNTRST <sub>L</sub>	B12 A4L	B13 A1L	B14 VDD	B15 NC	B16 NC
C1 NC	C2 I/O9L	C3 VSS	C4 NC	C5 A13L	C6 A10L	C7 A7L	C8 NC	C9 LB <sub>L</sub>	C10 CLKL	C11 ADSL	C12 A6L	C13 A3L	C14 OPTL	C15 NC	C16 I/O8L
D1 NC	D2 I/O9R	D3 NC	D4 VDD	D5 VDDQL	D6 VDDQL	D7 VDDQR	D8 VDDQR	D9 VDDQL	D10 VDDQL	D11 VDDQR	D12 VDDQR	D13 VDD	D14 NC	D15 NC	D16 I/O8R
E1 I/O10R	E2 I/O10L	E3 NC	E4 VDDQL	E5 VDD	E6 VDD	E7 VSS	E8 VSS	E9 VSS	E10 VSS	E11 VDD	E12 VDD	E13 VDDQR	E14 NC	E15 I/O7L	E16 I/O7R
F1 I/O11L	F2 NC	F3 I/O11R	F4 VDDQL	F5 VDD	F6 VSS	F7 VSS	F8 VSS	F9 VSS	F10 VSS	F11 VSS	F12 VDD	F13 VDDQR	F14 I/O6R	F15 NC	F16 I/O6L
G1 NC	G2 NC	G3 I/O12L	G4 VDDQR	G5 VSS	G6 VSS	G7 VSS	G8 VSS	G9 VSS	G10 VSS	G11 VSS	G12 VSS	G13 VDDQL	G14 I/O5L	G15 NC	G16 NC
H1 NC	H2 I/O12R	H3 NC	H4 VDDQR	H5 VSS	H6 VSS	H7 VSS	H8 VSS	H9 VSS	H10 VSS	H11 VSS	H12 VSS	H13 VDDQL	H14 NC	H15 NC	H16 I/O5R
J1 I/O13L	J2 I/O14R	J3 I/O13R	J4 VDDQL	J5 VSS	J6 VSS	J7 VSS	J8 VSS	J9 VSS	J10 VSS	J11 VSS	J12 VSS	J13 VDDQR	J14 I/O4R	J15 I/O3R	J16 I/O4L
K1 NC	K2 NC	K3 I/O14L	K4 VDDQL	K5 VSS	K6 VSS	K7 VSS	K8 VSS	K9 VSS	K10 VSS	K11 VSS	K12 VSS	K13 VDDQR	K14 NC	K15 NC	K16 I/O3L
L1 I/O15L	L2 NC	L3 I/O15R	L4 VDDQR	L5 VDD	L6 VSS	L7 VSS	L8 VSS	L9 VSS	L10 VSS	L11 VSS	L12 VDD	L13 VDDQL	L14 I/O2L	L15 NC	L16 I/O2R
M1 I/O16R	M2 I/O16L	M3 NC	M4 VDDQR	M5 VDD	M6 VDD	M7 VSS	M8 VSS	M9 VSS	M10 VSS	M11 VDD	M12 VDD	M13 VDDQL	M14 I/O1R	M15 I/O1L	M16 NC
N1 NC	N2 I/O17R	N3 NC	N4 VDD	N5 VDDQR	N6 VDDQR	N7 VDDQL	N8 VDDQL	N9 VDDQR	N10 VDDQR	N11 VDDQL	N12 VDDQL	N13 VDD	N14 NC	N15 I/O0R	N16 NC
P1 NC	P2 I/O17L	P3 NC	P4 NC	P5 A13R	P6 A10R	P7 A7R	P8 NC	P9 LB <sub>R</sub>	P10 CLKR	P11 ADSR	P12 A6R	P13 A3R	P14 NC	P15 NC	P16 I/O0L
R1 NC	R2 NC	R3 NC	R4 NC	R5 NC	R6 A12R	R7 A9R	R8 UB <sub>R</sub>	R9 CE0R	R10 R/W <sub>R</sub>	R11 CNTRST <sub>R</sub>	R12 A4R	R13 A1R	R14 OPTR	R15 NC	R16 NC
T1 NC	T2 NC	T3 NC	T4 NC	T5 A14R	T6 A11R	T7 A8R	T8 NC	T9 CE1R	T10 OE <sub>R</sub>	T11 CNTEN <sub>R</sub>	T12 A5R	T13 A2R	T14 A0R	T15 NC	T16 NC

4833 drw 02c

NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration<sup>(1,2,3,4)</sup> (con't.)



NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 14mm x 20mm x 1.4mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.
7. In the 70V3379 (32K x 18) and 70V3389 (64K x 18), pins 96 and 99 are NC. The upgrade devices 70V3399 (128K x 18) and 70V3319 (256K x 18) assign these pins as VSS. Customers who plan to take advantage of the upgrade path should treat these pins as VSS on the 70V3379 and 70V3389. If no upgrade is needed, the pins can be treated as NC.

## Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$ , CE1L	$\overline{CE}_{0R}$ , CE1R	Chip Enables
R/ $\overline{WL}$	R/ $\overline{WR}$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A0L - A14L	A0R - A14R	Address
I/O0L - I/O17L	I/O0R - I/O17R	Data Input/Output
CLKL	CLKR	Clock
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset
UBL - LBL	UBR - LBR	Byte Enables (9-bit bytes)
VDD0L	VDD0R	Power (I/O Bus) (3.3V or 2.5V) <sup>(1)</sup>
OPTL	OPTR	Option for selecting VDD0x <sup>(1,2)</sup>
VDD		Power (3.3V) <sup>(1)</sup>
VSS		Ground (0V)

4833 tbl 01

**NOTES:**

- VDD, OPTx, and VDD0x must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
- OPTx selects the operating voltage levels for the I/Os and controls on that port. If OPTx is set to VIH (3.3V), then that port's I/Os and controls will operate at 3.3V levels and VDD0x must be supplied at 3.3V. If OPTx is set to VIL (0V), then that port's I/Os and controls will operate at 2.5V levels and VDD0x must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.

## Truth Table I—Read/Write and Enable Control<sup>(1,2,3)</sup>

$\overline{OE}$	CLK	$\overline{CE}_0$	CE1	$\overline{UB}$	$\overline{LB}$	R/ $\overline{W}$	Upper Byte I/O9-18	Lower Byte I/O0-8	MODE
X	↑	L	H	H	H	X	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	L	L	High-Z	DIN	Write to Lower Byte Only
X	↑	L	H	L	H	L	DIN	High-Z	Write to Upper Byte Only
X	↑	L	H	L	L	L	DIN	DIN	Write to Both Bytes
L	↑	L	H	H	L	H	High-Z	DOUT	Read Lower Byte Only
L	↑	L	H	L	H	H	DOUT	High-Z	Read Upper Byte Only
L	↑	L	H	L	L	H	DOUT	DOUT	Read Both Bytes
H	↑	L	H	L	L	X	High-Z	High-Z	Outputs Disabled

4833 tbl 02

**NOTES:**

- "H" = VIH, "L" = VIL, "X" = Don't Care.
- $\overline{ADS}$ ,  $\overline{CNTEN}$ ,  $\overline{CNTRST}$  = X.
- $\overline{OE}$  is an asynchronous input signal.

Truth Table II—Address Counter Control<sup>(1,2)</sup>

Address	Previous Address	Addr Used	CLK <sup>(6)</sup>	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNRST}$	I/O <sup>(3)</sup>	MODE
X	X	0	↑	X	X	L <sup>(4)</sup>	D <sub>IO</sub> (0)	Counter Reset to Address 0
An	X	An	↑	L <sup>(4)</sup>	X	H	D <sub>IO</sub> (n)	External Address Used
An	Ap	Ap	↑	H	H	H	D <sub>IO</sub> (p)	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1	↑	H	L <sup>(5)</sup>	H	D <sub>IO</sub> (p+1)	Counter Enabled—Internal Address generation

4833 tbl 03

NOTES:

- "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of  $\overline{RW}$ ,  $\overline{CE_0}$ , CE<sub>1</sub>,  $\overline{BEn}$  and  $\overline{OE}$ .
- Outputs are in Pipelined mode: the data out will be delayed by one cycle.
- $\overline{ADS}$  and  $\overline{CNRST}$  are independent of all other memory control signals including  $\overline{CE_0}$ , CE<sub>1</sub> and  $\overline{BEn}$ .
- The address counter advances if  $\overline{CNTEN} = V_{IL}$  on the rising edge of CLK, regardless of all other memory control signals including  $\overline{CE_0}$ , CE<sub>1</sub>,  $\overline{BEn}$ .

Recommended Operating Temperature and Supply Voltage<sup>(1)</sup>

Grade	Ambient Temperature	GND	V <sub>DD</sub>
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

4833 tbl 04

NOTE:

- This is the parameter T<sub>A</sub>. This is the "instant on" case temperature.

Recommended DC Operating Conditions with V<sub>DDQ</sub> at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage	3.15	3.3	3.45	V
V <sub>DDQ</sub>	I/O Supply Voltage <sup>(3)</sup>	2.375	2.5	2.625	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage <sup>(3)</sup> (Address & Control Inputs)	1.7	—	V <sub>DDQ</sub> + 125mV <sup>(2)</sup>	V
V <sub>IH</sub>	Input High Voltage - I/O <sup>(3)</sup>	1.7	—	V <sub>DDQ</sub> + 125mV <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.7	V

4833 tbl 05a

NOTES:

- V<sub>IL</sub> ≥ -1.5V for pulse width less than 10 ns.
- V<sub>TERM</sub> must not exceed V<sub>DDQ</sub> + 125mV.
- To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V<sub>IL</sub> (0V), and V<sub>DDQX</sub> for that port must be supplied as indicated above.

Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Commercial & Industrial	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	50	mA

4833 tbl 06

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>DD</sub> + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to ≤ 20mA for the period of V<sub>TERM</sub> ≥ V<sub>DD</sub> + 150mV.

Recommended DC Operating Conditions with V<sub>DDQ</sub> at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage	3.15	3.3	3.45	V
V <sub>DDQ</sub>	I/O Supply Voltage <sup>(3)</sup>	3.15	3.3	3.45	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage (Address & Control Inputs) <sup>(3)</sup>	2.0	—	V <sub>DDQ</sub> + 150mV <sup>(2)</sup>	V
V <sub>IH</sub>	Input High Voltage - I/O <sup>(3)</sup>	2.0	—	V <sub>DDQ</sub> + 150mV <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.8	V

4833 tbl 05b

NOTES:

- V<sub>IL</sub> ≥ -1.5V for pulse width less than 10 ns.
- V<sub>TERM</sub> must not exceed V<sub>DDQ</sub> + 150mV.
- To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V<sub>IH</sub> (3.3V), and V<sub>DDQX</sub> for that port must be supplied as indicated above.

Capacitance<sup>(1)</sup>

(TA = +25°C, F = 1.0MHz) TQFP ONLY

Symbol	Parameter	Conditions <sup>(2)</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	8	pF
C <sub>OUT</sub> <sup>(3)</sup>	Output Capacitance	V <sub>OUT</sub> = 3dV	10.5	pF

4833 tbl 07

NOTES:

1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C<sub>OUT</sub> also references C<sub>IO</sub>.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V<sub>DD</sub> = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V3379S		Unit
			Min.	Max.	
I <sub>LI</sub>	Input Leakage Current <sup>(1)</sup>	V <sub>DDQ</sub> = Max., V <sub>IN</sub> = 0V to V <sub>DDQ</sub>	—	10	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{CE_0}$ = V <sub>IH</sub> or CE <sub>1</sub> = V <sub>IL</sub> , V <sub>OUT</sub> = 0V to V <sub>DDQ</sub>	—	10	μA
V <sub>OL</sub> (3.3V)	Output Low Voltage <sup>(2)</sup>	I <sub>OL</sub> = +4mA, V <sub>DDQ</sub> = Min.	—	0.4	V
V <sub>OH</sub> (3.3V)	Output High Voltage <sup>(2)</sup>	I <sub>OH</sub> = -4mA, V <sub>DDQ</sub> = Min.	2.4	—	V
V <sub>OL</sub> (2.5V)	Output Low Voltage <sup>(2)</sup>	I <sub>OL</sub> = +2mA, V <sub>DDQ</sub> = Min.	—	0.4	V
V <sub>OH</sub> (2.5V)	Output High Voltage <sup>(2)</sup>	I <sub>OH</sub> = -2mA, V <sub>DDQ</sub> = Min.	2.0	—	V

4833 tbl 08

NOTES:

1. At V<sub>DD</sub> ≤ - 2.0V input leakages are undefined.
2. V<sub>DDQ</sub> is selectable (3.3V/2.5V) via OPT pins. Refer to p.4 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(3)</sup> ( $V_{DD} = 3.3V \pm 150mV$ )

Symbol	Parameter	Test Condition	Version	70V3379S4 Com'l Only		70V3379S5 Com'l & Ind		70V3379S6 Com'l Only		Unit	
				Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.		
IDD	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$ , Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	375	460	285	360	245	310	mA
			IND	S	—	—	285	415	—	—	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	S	145	190	105	145	95	125	mA
			IND	S	—	—	105	175	—	—	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A^* = V_{IL}$ and $\overline{CE}^*B^* = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	265	325	190	260	175	225	mA
			IND	S	—	—	190	300	—	—	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DDQ} - 0.2V$ , $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0^{(2)}$	COM'L	S	6	15	6	15	6	15	mA
			IND	S	—	—	6	30	—	—	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^*A^* \leq 0.2V$ and $\overline{CE}^*B^* \geq V_{DDQ} - 0.2V^{(5)}$ $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$ , Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	265	325	180	260	170	225	mA
			IND	S	—	—	180	300	—	—	

4833 tbl 09

NOTES:

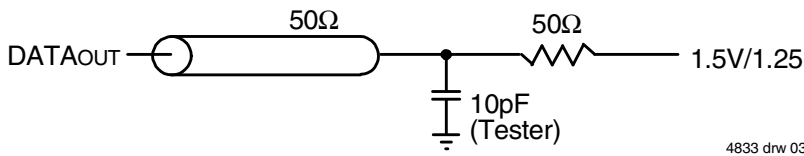
- At  $f = f_{MAX}$ , address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of  $1/t_{cyc}$ , using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$  means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$ ,  $T_A = 25^\circ C$  for Typ, and are not production tested.  $I_{DD} \text{ at } (f=0) = 120mA$  (Typ).
- $\overline{CE}_X = V_{IL}$  means  $\overline{CE}_{0X} = V_{IL}$  and  $CE_{1X} = V_{IH}$   
 $\overline{CE}_X = V_{IH}$  means  $\overline{CE}_{0X} = V_{IH}$  or  $CE_{1X} = V_{IL}$   
 $\overline{CE}_X \leq 0.2V$  means  $\overline{CE}_{0X} \leq 0.2V$  and  $CE_{1X} \geq V_{DDQ} - 0.2V$   
 $\overline{CE}_X \geq V_{DDQ} - 0.2V$  means  $\overline{CE}_{0X} \geq V_{DDQ} - 0.2V$  or  $CE_{1X} \leq 0.2V$   
 "X" represents "L" for left port or "R" for right port.



AC Test Conditions

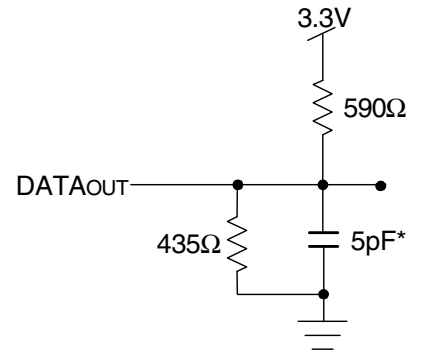
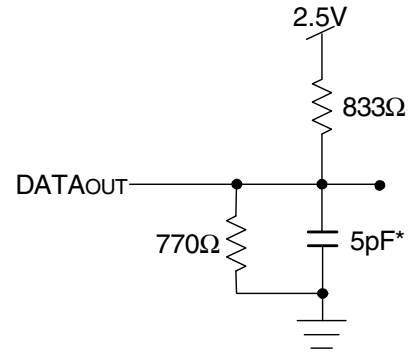
Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.35V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.35V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1, 2, and 3

4833 tbl 10



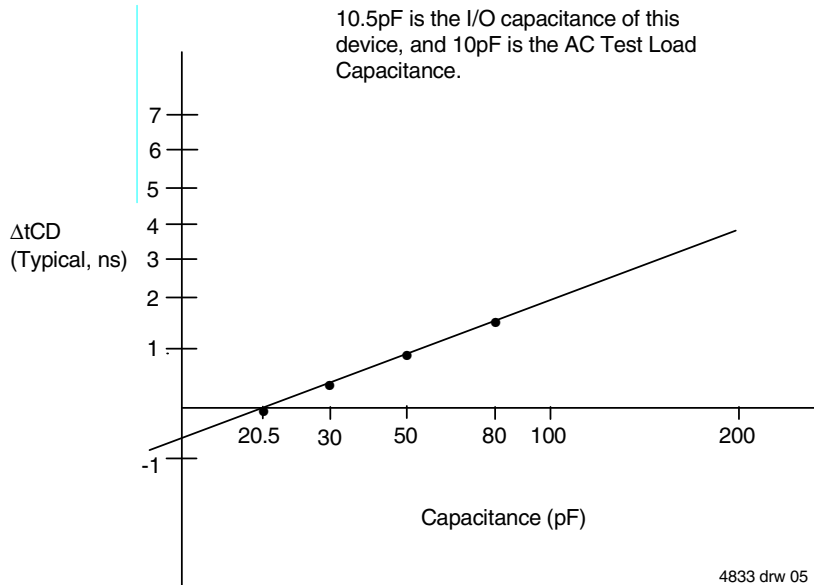
4833 drw 03

Figure 1. AC Output Test load.



4833 drw 04

Figure 2. Output Test Load  
(For tCKLZ, tCKHZ, tOLZ, and tOHZ).  
\*Including scope and jig.



4833 drw 05

Figure 3. Typical Output Derating (Lumped Capacitive Load).

## AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)<sup>(1,2)</sup>

(V<sub>DD</sub> = 3.3V ± 150mV, T<sub>A</sub> = 0°C to +70°C)

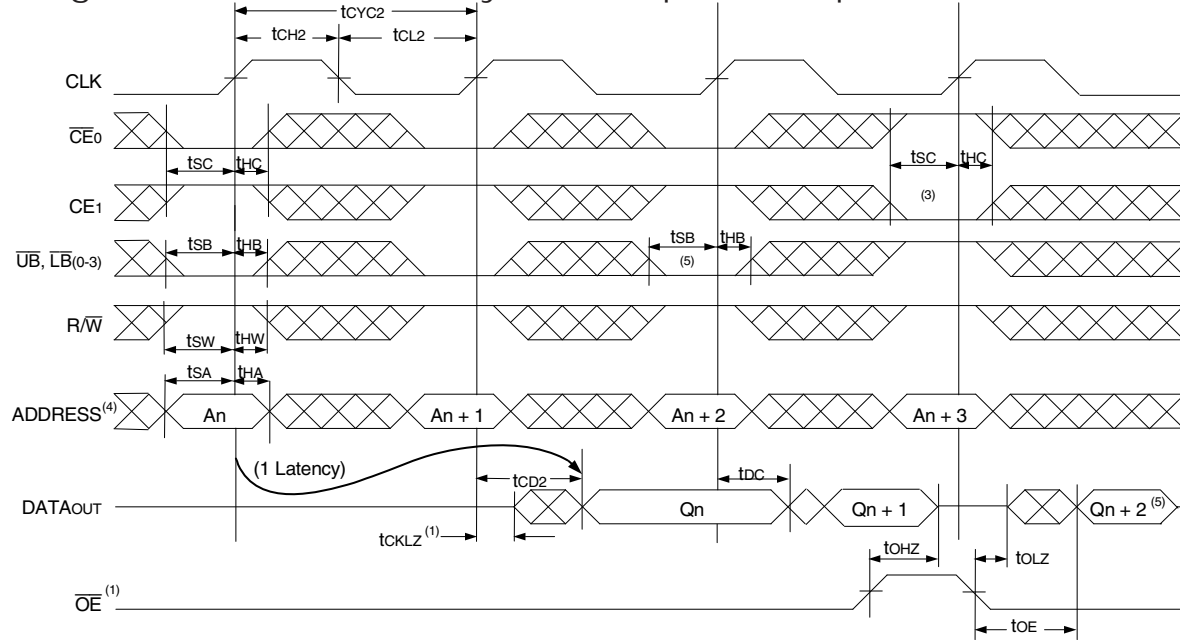
Symbol	Parameter	70V3379S4 Com'l Only		70V3379S5 Com'l & Ind		70V3379S6 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>CYC2</sub>	Clock Cycle Time (Pipelined)	7.5	—	10	—	12	—	ns
t <sub>CH2</sub>	Clock High Time (Pipelined)	3	—	4	—	5	—	ns
t <sub>CL2</sub>	Clock Low Time (Pipelined)	3	—	4	—	5	—	ns
t <sub>R</sub>	Clock Rise Time	—	3	—	3	—	3	ns
t <sub>F</sub>	Clock Fall Time	—	3	—	3	—	3	ns
t <sub>SA</sub>	Address Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HA</sub>	Address Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>SC</sub>	Chip Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HC</sub>	Chip Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>SB</sub>	Byte Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HB</sub>	Byte Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>SW</sub>	R/W Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HW</sub>	R/W Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>SD</sub>	Input Data Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HD</sub>	Input Data Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>SAD</sub>	$\overline{ADS}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HAD</sub>	$\overline{ADS}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>SCN</sub>	$\overline{CNTEN}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HCN</sub>	$\overline{CNTEN}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>SRST</sub>	$\overline{CNTRST}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HRST</sub>	$\overline{CNTRST}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>OE</sub> <sup>(1)</sup>	Output Enable to Data Valid	—	4	—	5	—	6	ns
t <sub>OLZ</sub>	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t <sub>OHZ</sub>	Output Enable to Output High-Z	1	4	1	4.5	1	5	ns
t <sub>CD2</sub>	Clock to Data Valid (Pipelined)	—	4.2	—	5	—	6	ns
t <sub>DC</sub>	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t <sub>CKHZ</sub>	Clock High to Output High-Z	1	3	1	4.5	1.5	6	ns
t <sub>CKLZ</sub>	Clock High to Output Low-Z	1	—	1	—	1	—	ns
<b>Port-to-Port Delay</b>								
t <sub>CO</sub>	Clock-to-Clock Offset	6	—	8	—	10	—	ns

4833 tbl 11

**NOTES:**

1. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ( $\overline{OE}$ ).
2. These values are valid for either level of V<sub>DD0</sub> (3.3V/2.5V). See page 4 for details on selecting the desired I/O voltage levels for each port.

### Timing Waveform of Read Cycle for Pipelined Operation<sup>(2)</sup>

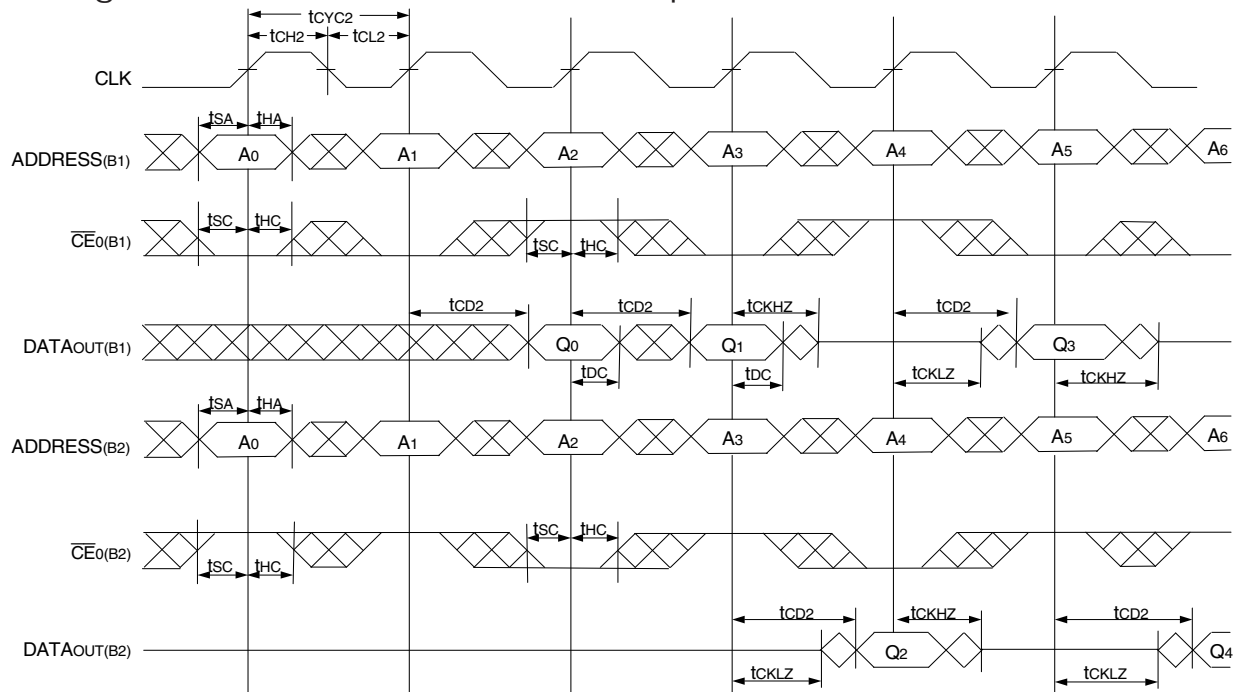


**NOTES:**

1.  $\overline{OE}$  is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2.  $\overline{ADS} = V_{IL}$ ,  $\overline{CNTEN}$  and  $\overline{CNTRST} = V_{IH}$ .
3. The output is disabled (High-Impedance state) by  $\overline{CE}_0 = V_{IH}$ ,  $CE_1 = V_{IL}$ ,  $\overline{UB}$ ,  $\overline{LB} = V_{IH}$  following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If  $\overline{UB}$  or  $\overline{LB}$  was HIGH, then the appropriate Byte of DATAout for  $Q_n + 2$  would be disabled (High-Impedance state).

4833 drw 06

### Timing Waveform of a Multi-Device Pipelined Read<sup>(1,2)</sup>

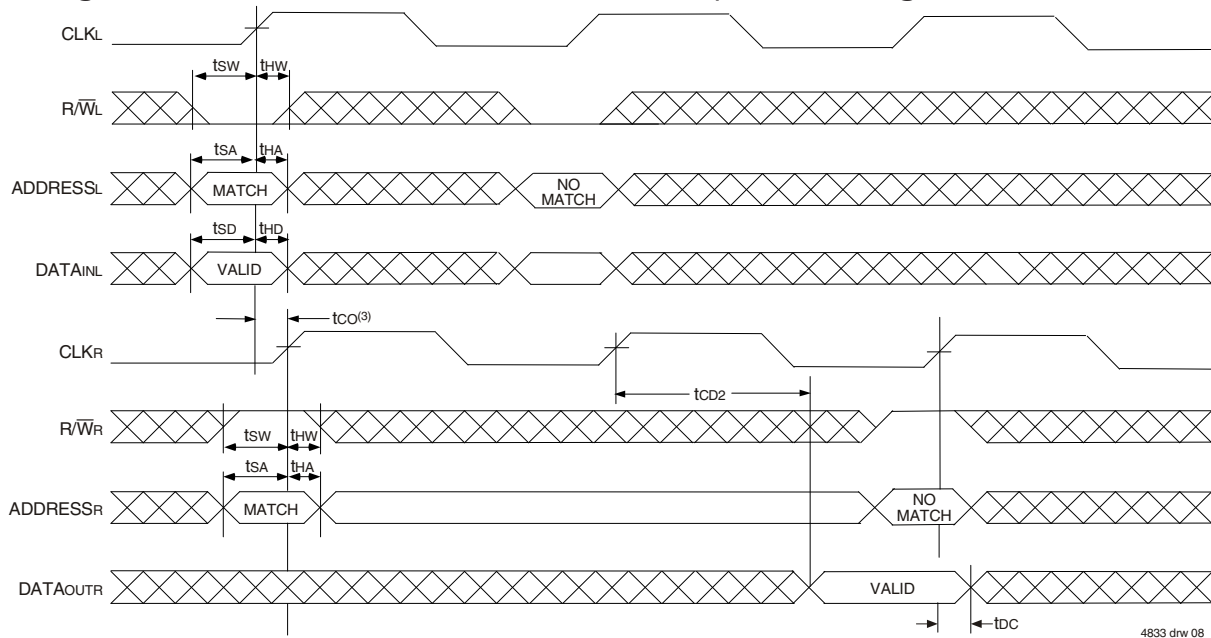


**NOTES:**

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V3379 for this waveform, and are setup for depth expansion in this example.  $ADDRESS_{(B1)} = ADDRESS_{(B2)}$  in this situation.
2.  $\overline{UB}$ ,  $\overline{LB}$ ,  $\overline{OE}$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1(B1)$ ,  $CE_1(B2)$ ,  $R/\overline{W}$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ .

4833 drw 07

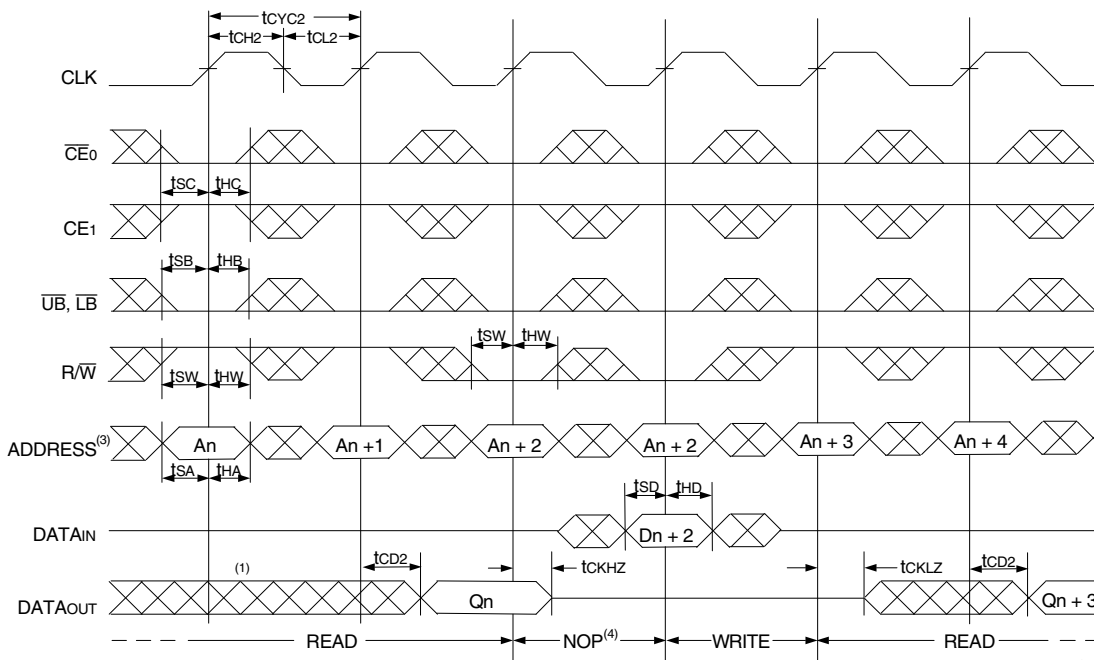
Timing Waveform of Left Port Write to Pipelined Right Port Read<sup>(1,2)</sup>



NOTES:

1.  $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ .
2.  $\overline{OE} = V_{IL}$  for the Right Port, which is being read from.  $\overline{OE} = V_{IH}$  for the Left Port, which is being written to.
3. If  $t_{CO} \leq$  minimum specified, then data from right port read is not valid until following right port clock cycle (ie, time from write to valid read on opposite port will be  $t_{CO} + 2 t_{CYC2} + t_{CD2}$ ). If  $t_{CO} >$  minimum, then data from right port read is available on first right port clock cycle (ie, time from write to valid read on opposite port will be  $t_{CO} + t_{CYC} + t_{CD2}$ ).

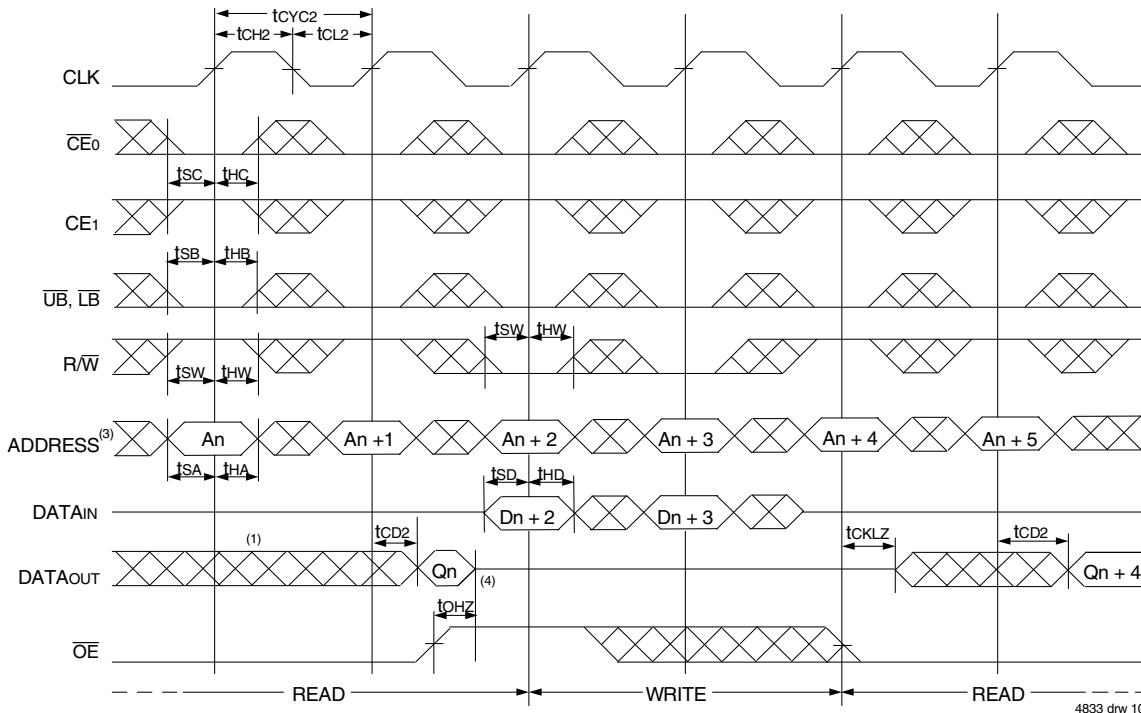
Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(2)</sup>



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2.  $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ . "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.

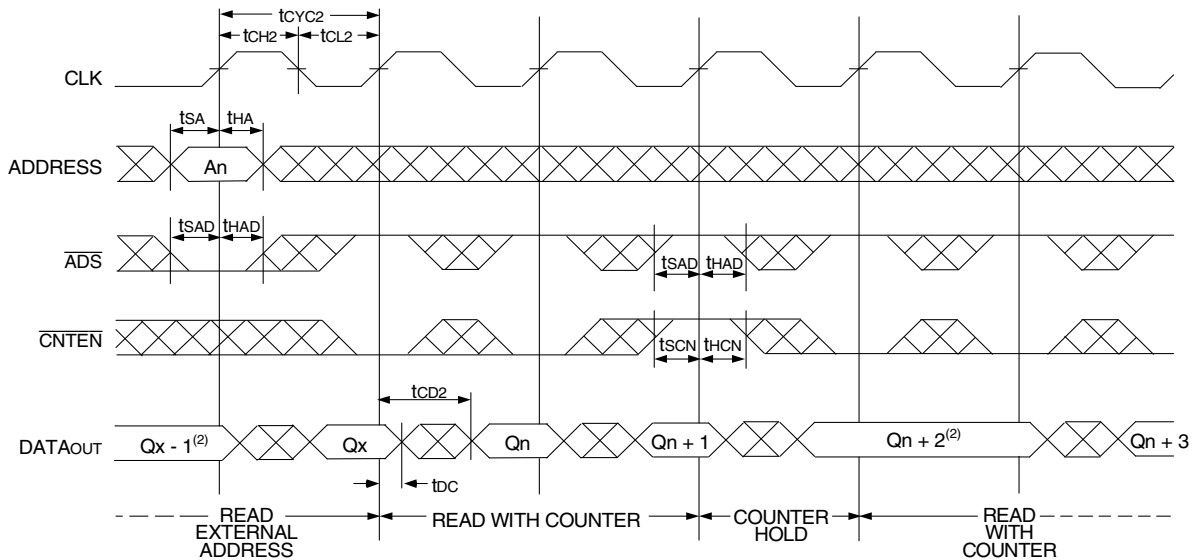
Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE}$  Controlled)<sup>(2)</sup>



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2.  $\overline{CE0}$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $\overline{ADS} = V_{IL}$ ;  $\overline{CE1}$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ .
3. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

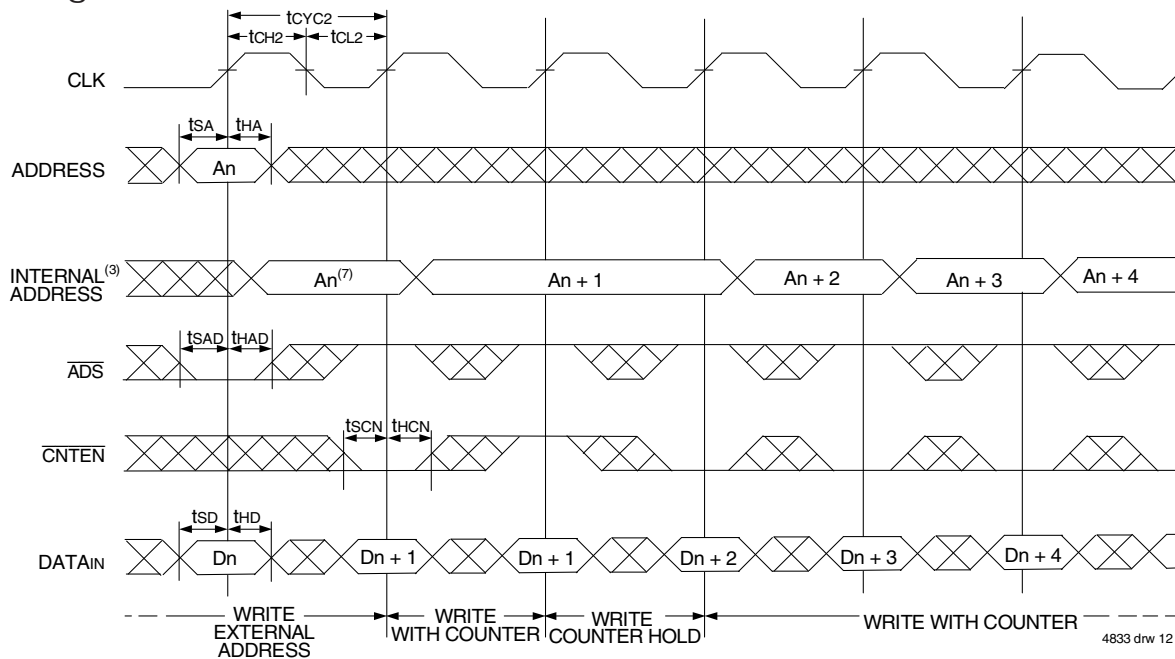
Timing Waveform of Pipelined Read with Address Counter Advance<sup>(1)</sup>



NOTES:

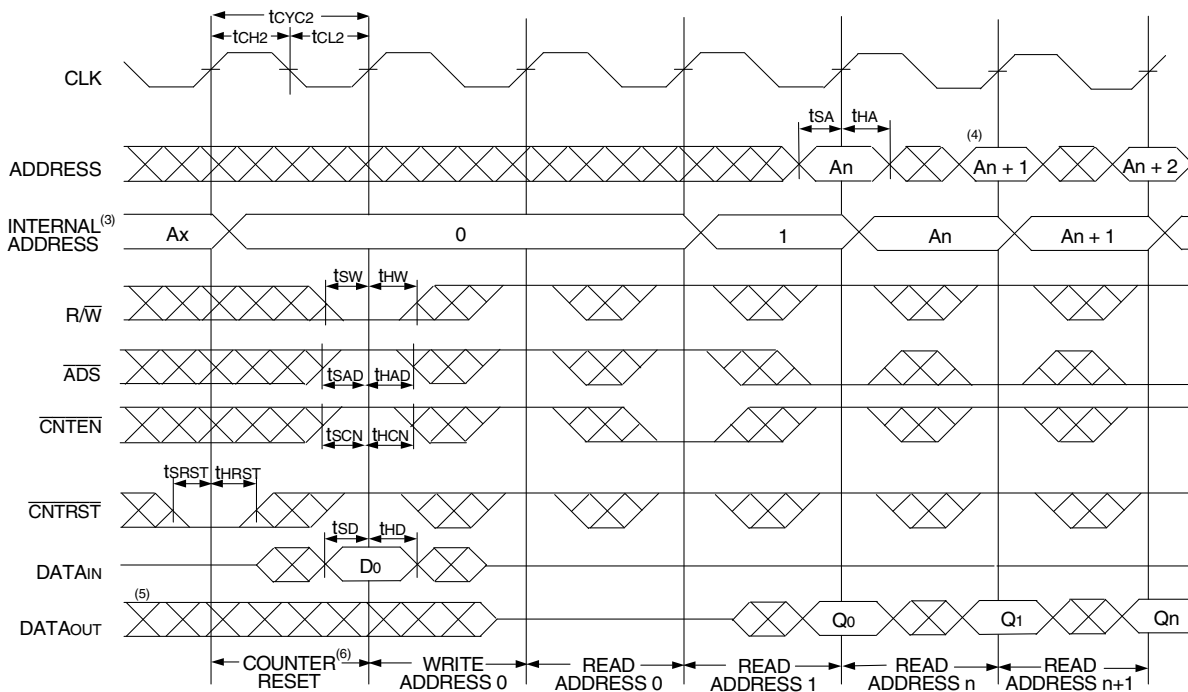
1.  $\overline{CE0}$ ,  $\overline{OE}$ ,  $\overline{UB}$ ,  $\overline{LB} = V_{IL}$ ;  $\overline{CE1}$ ,  $\overline{R/W}$ , and  $\overline{CNTRST} = V_{IH}$ .
2. If there is no address change via  $\overline{ADS} = V_{IL}$  (loading a new address) or  $\overline{CNTEN} = V_{IL}$  (advancing the address), i.e.  $\overline{ADS} = V_{IH}$  and  $\overline{CNTEN} = V_{IH}$ , then the data output remains constant for subsequent clocks.

### Timing Waveform of Write with Address Counter Advance<sup>(1)</sup>



4833 drw 12

### Timing Waveform of Counter Reset<sup>(2)</sup>



4833 drw 13

**NOTES:**

- $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $R/\overline{W} = V_{IL}$ ;  $CE_1$  and  $\overline{CNTRST} = V_{IH}$ .
- $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB} = V_{IL}$ ;  $CE_1 = V_{IH}$ .
- The "Internal Address" is equal to the "External Address" when  $\overline{ADS} = V_{IL}$  and equals the counter output when  $\overline{ADS} = V_{IH}$ .
- Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
- Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
- No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle: Addr 0 will be accessed. Extra cycles are shown here simply for clarification.
- $\overline{CNTEN} = V_{IL}$  advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1' Address is written to during this cycle.

### Functional Description

The IDT70V3379 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on  $\overline{CE_0}$  or a LOW on  $CE_1$  for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V3379s for depth expansion configurations. Two cycles are required with  $\overline{CE_0}$  LOW and  $CE_1$  HIGH to reactivate the outputs.

### Depth and Width Expansion

The IDT70V3379 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V3379 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 36-bits or wider.

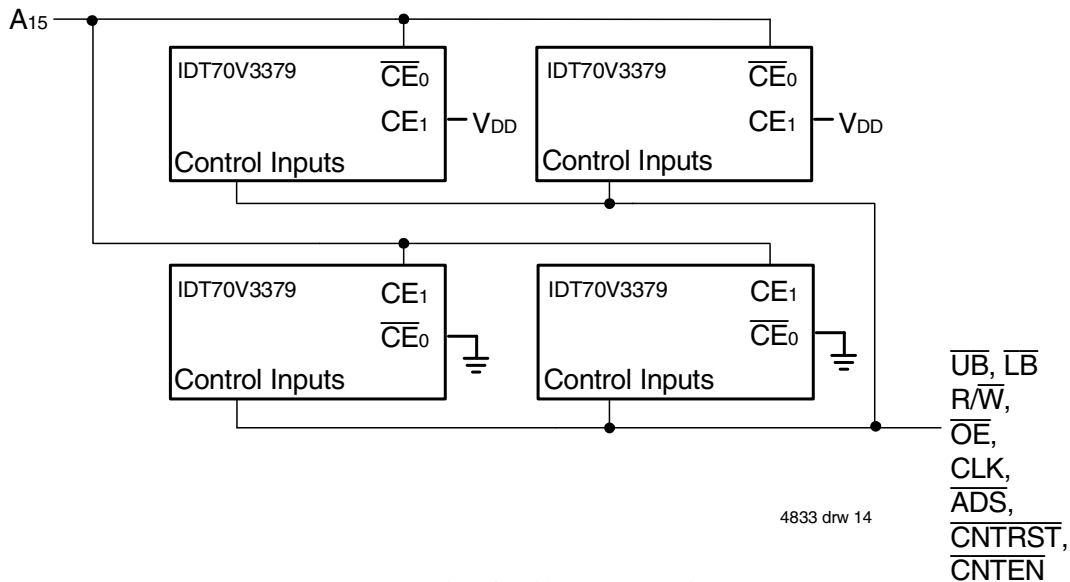
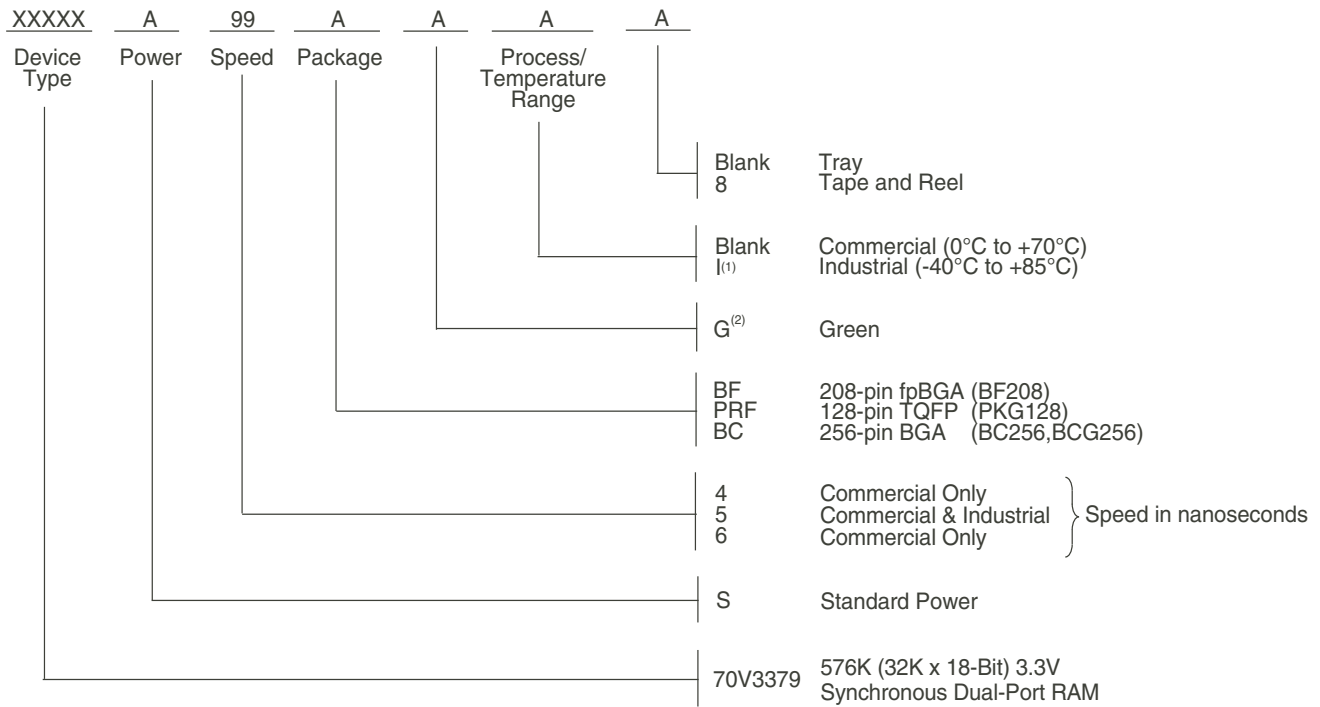


Figure 4. Depth and Width Expansion with IDT70V3379

### Ordering Information



4833 drw 15a

**NOTES:**

- Contact your local sales office for Industrial temp range in other speeds, packages and powers.
  - Green parts available. For specific speeds, packages and powers contact your local sales office.
- LEAD FINISH (SnPb) parts are Obsolete. Product Discontinuation Notice - PDN# SP-17-02  
Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

### Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
4	70V3379S4BC	BC256	CABGA	C
	70V3379S4BC8	BC256	CABGA	C
	70V3379S4BCG	BCG256	CABGA	C
	70V3379S4BF	BF208	CABGA	C
	70V3379S4BF8	BF208	CABGA	C
	70V3379S4PRFG	PKG128	TQFP	C
	70V3379S4PRFG8	PKG128	TQFP	C
5	70V3379S5BC	BC256	CABGA	C
	70V3379S5BC8	BC256	CABGA	C
	70V3379S5BF	BF208	CABGA	C
	70V3379S5BF8	BF208	CABGA	C
	70V3379S5BF1	BF208	CABGA	I
	70V3379S5BF18	BF208	CABGA	I
6	70V3379S6BC	BC256	CABGA	C
	70V3379S6BC8	BC256	CABGA	C
	70V3379S6BF	BF208	CABGA	C
	70V3379S6BF8	BF208	CABGA	C



## Datasheet Document History

01/18/98:	Initial Public Release
03/15/99:	Page 10 Additional Notes
04/28/99:	Added fpBGA package
06/08/99:	Page 2 Changed package body height from 1.5mm to 1.4mm
06/11/99:	Page 5 Deleted note 6 for Table II
07/14/99:	Page 2 Corrected pin to T3 to VDDQL
08/04/99:	Page 6 Improved power numbers
10/04/99:	Upgraded speed to 133MHz, added 2.5V I/O capability
11/12/99:	Replaced IDT logo
02/28/00:	Added new BGA package, added full 2.5V interface capability
05/01/00:	Page 2 Added ball pitch Page 3 Renamed pins Page 6 Made corrections to Truth Table Page 9 Changed $\Omega$ numbers in figure 2
06/07/00:	Page 4 Added information to pin and pin notes Page 6 Increased storage temperature parameter Clarified TA Parameter Page 8 DC Electrical parameters—changed wording from "open" to "disabled" Removed note 7 on DC Electrical Characteristics table
01/10/01:	Page 1 Changed 64K to 32K in block drawing Removed Preliminary status
04/10/01:	Added Industrial Temperature Ranges and removed related notes
12/12/01:	Page 2, 3 & 4 Added date revision to pin configurations Page 6 Removed industrial temp footnote from table 04 Page 8 & 10 Removed industrial temp for 6ns from DC & AC Electrical Characteristics Page 16 Removed industrial temp from 6ns in ordering information Added industrial temp footnote Page 1 & 17 Replaced <sup>TM</sup> logo with <sup>®</sup> logo Page 1 Added green availability to features
01/05/06:	Page 16 Added green indicator to Ordering Information
02/08/06:	Page 5 Changed footnote 2 for Truth Table I from $\overline{ADS}$ , $\overline{CNTEN}$ , $\overline{CNTRST} = V_{IH}$ to $\overline{ADS}$ , $\overline{CNTEN}$ , $\overline{CNTRST} = X$
07/25/08:	Page 8 Corrected a typo in the DC Chars table
01/19/09:	Page 16 Removed "IDT" from orderable part number
08/11/15:	Page 2 & 3 Removed date from all of the pin configurations 206-pin fpBGA, 128-pin TQFP & 256-pin PGA Page 16 Added Tape & Reel to Ordering Information Product Discontinuation Notice - PDN# SP-17-02
02/13/18:	Last time buy expires June 15, 2018
07/17/19:	Page 2, 3 & 4 Updated package codes BF-208 to BF208, BC-256 to BC256, BCG256 and PK-128 to PKG128 Page 16 Added Orderable Part Information table

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.