RENESAS

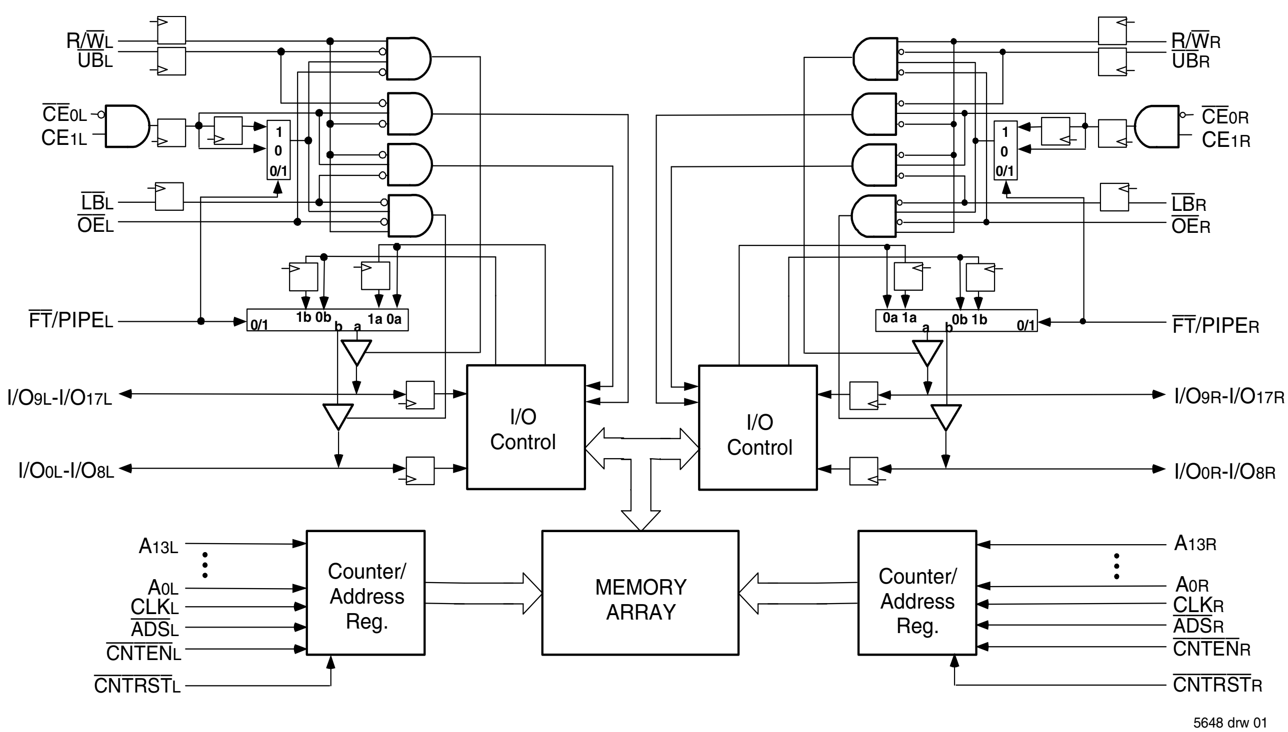
HIGH-SPEED 3.3V 16K x 18 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM

70V9369L

Features:

- **True Dual-Ported memory cells which allow simultaneous access of the same memory location**
- **High-speed clock to data access**
  - *Commercial: 9ns (max.)*
- **Low-power operation**
  - *IDT70V9369L*
    Active: 500mW (typ.)
    Standby: 1.5mW (typ.)
- **Flow-Through or Pipelined output mode on either port via the FT/PIPE pins**
- **Counter enable and reset features**
- **Dual chip enables allow for depth expansion without additional logic**
- **Full synchronous operation on both ports**
  - *4ns setup to clock and 1ns hold on all control, data, and address inputs*
  - *Data input, address, and control registers*
  - *Fast 9ns clock to data out in the Pipelined output mode*
  - *Self-timed write allows fast cycle time*
  - *15ns cycle time, 67MHz operation in Pipelined output mode*
- **Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility**
- **LVTTL- compatible, single 3.3V (±0.3V) power supply**
- **Available in a 100-pin Thin Quad Flatpack (TQFP)**
- **Green parts available, see ordering information**

Functional Block Diagram



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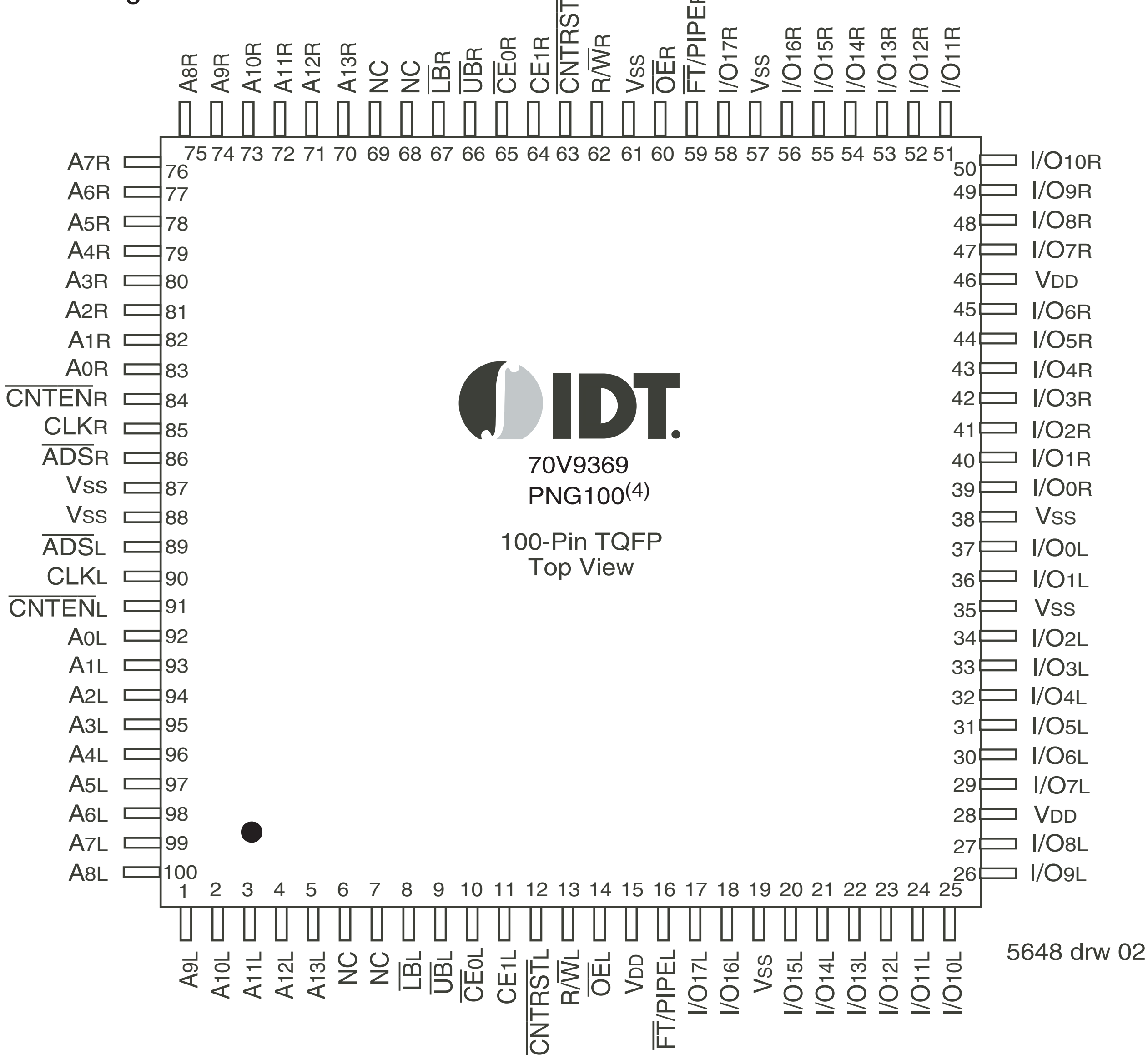
DSC-5648/7

Description:

The IDT70V9369 is a high-speed 16K x 18 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT70V9369 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1, permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using CMOS high-performance technology, these devices typically operate on only 500mW of power.

Pin Configuration[1,2,3]



NOTES:
1. All V_{DD} pins must be connected to power supply.
2. All V_{SS} pins must be connected to ground.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables[2]
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{13L}	A_{0R} - A_{13R}	Address
I/O_{0L} - I/O_{17L}	I/O_{0R} - I/O_{17R}	Data Input/Output
CLK_L	CLK_R	Clock
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select[1]
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select[1]
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset
$\overline{FT}/PIPE_L$	$\overline{FT}/PIPE_R$	Flow-Through / Pipeline
V_{DD}		Power (3.3V)
V_{SS}		Ground (0V)

5648 tbl 01

NOTES:
1. $\overline{LB}$ and $\overline{UB}$ are single buffered regardless of state of $\overline{FT}$/PIPE.
2. $\overline{CE}_0$ and CE_1 are single buffered when $\overline{FT}/PIPE = V_{IL}$,
   $\overline{CE}_0$ and CE_1 are double buffered when $\overline{FT}/PIPE = V_{IH}$, i.e., the signals take two cycles to deselect.

Truth Table I—Read/Write and Enable Control[1,2,3]

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$\overline{UB}$	$\overline{LB}$	$R/\overline{W}$	Upper Byte I/O_{9-17}[4]	Lower Byte I/O_{0-8}[5]	MODE
X	↑	H	X	X	X	X	High-Z	High-Z	Deselected–Power Down
X	↑	X	L	X	X	X	High-Z	High-Z	Deselected–Power Down
X	↑	L	H	H	H	X	High-Z	High-Z	Both Bytes Deselected
X	↑	L	H	L	H	L	$DATA_{IN}$	High-Z	Write to Upper Byte Only
X	↑	L	H	H	L	L	High-Z	$DATA_{IN}$	Write to Lower Byte Only
X	↑	L	H	L	L	L	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes
L	↑	L	H	L	H	H	$DATA_{OUT}$	High-Z	Read Upper Byte Only
L	↑	L	H	H	L	H	High-Z	$DATA_{OUT}$	Read Lower Byte Only
L	↑	L	H	L	L	H	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes
H	X	L	H	L	L	X	High-Z	High-Z	Outputs Disabled

5648 tbl 02

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = X.
3. $\overline{OE}$ is an asynchronous input signal.

Truth Table II—Address Counter Control(1,2,6)

Address	Previous Internal Address	Internal Address Used	CLK(6)	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNTRST}$	I/O(3)	MODE
An	X	An	↑	L(4)	X	H	$D_{I/O}$ (n)	External Address Used
X	An	An + 1	↑	H	L(5)	H	$D_{I/O}$(n+1)	Counter Enabled—Internal Address generation
X	An + 1	An + 1	↑	H	H	H	$D_{I/O}$(n+1)	External Address Blocked—Counter disabled (An + 1 reused)
X	X	A0	↑	X	X	L(4)	$D_{I/O}$(0)	Counter Reset to Address 0

5648 tbl 03

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{CE}_0$, $\overline{LB}$, $\overline{UB}$, and $\overline{OE}$ = V_{IL}; CE_1 and R/$\overline{W}$ = V_{IH}.
3. Outputs configured in Flow-Through Output mode; if outputs are in Pipelined mode the data out will be delayed by one cycle.
4. $\overline{ADS}$ and $\overline{CNTRST}$ are independent of all other signals including $\overline{CE}_0$, CE_1, $\overline{UB}$ and $\overline{LB}$.
5. The address counter advances if $\overline{CNTEN}$ = V_{IL} on the rising edge of CLK, regardless of all other signals including $\overline{CE}_0$, CE_1, $\overline{UB}$ and $\overline{LB}$.
6. While an external address is being loaded ($\overline{ADS}$ = V_{IL}), R/$\overline{W}$ = V_{IH} is recommended to ensure data is not written arbitrarily.

Recommended Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature(1)	GND	V_{DD}
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

5648 tbl 04

NOTE:
1. This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
Vss	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0V	—	V_{DD}+0.3V(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

5648 tbl 05

NOTES:
1. $V_{IL} \geq$ -1.5V for pulse width less than 10 ns.
2. V_{TERM} must not exceed V_{DD} +0.3V.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T_{BIAS}(3)	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{JN}	Junction Temperature	+150	°C
I_{OUT}	DC Output Current	50	mA

5648 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} +0.3V.
3. Ambient Temperature Under DC Bias. No AC Conditions. Chip deselect.

Capacitance(1)

(TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	9	pF
C_{OUT}(2)	Output Capacitance	V_{OUT} = 0V	10	pF

5648 tbl 07

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. C_{OUT} also references $C_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	70V9369L Min.	70V9369L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current(1)	V_{DD} = 3.6V, V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{DD}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	V

5648 tbl 08

NOTE:
1. At $V_{DD} \leq$ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range(3) (V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V9369L6 Com'l Only Typ.(4)	70V9369L6 Com'l Only Max.	70V9369L7 Com'l & Ind Typ.(4)	70V9369L7 Com'l & Ind Max.	70V9369L9 Com'l Only Typ.(4)	70V9369L9 Com'l Only Max.	70V9369L12 Com'l Only Typ.(4)	70V9369L12 Com'l Only Max.	Unit
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL}, Outputs Disabled, f = f_{MAX}(1)	COM'L	L	220	350	200	290	180	225	150	205	mA
			IND	L	—	—	200	335	—	—	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f_{MAX}(1)	COM'L	L	70	130	65	100	50	65	40	50	mA
			IND	L	—	—	65	115	—	—	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}(5) Active Port Outputs Disabled, f=f_{MAX}(1)	COM'L	L	150	250	140	210	110	150	100	140	mA
			IND	L	—	—	140	240	—	—	—	—	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD}$ - 0.2V, $V_{IN} \geq V_{DD}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0(2)	COM'L	L	0.4	5	0.4	5	0.4	5	0.4	5	mA
			IND	L	—	—	0.4	15	—	—	—	—	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$"A" $\leq$ 0.2V and $\overline{CE}$"B" $\geq V_{DD}$ - 0.2V(5) $V_{IN} \geq V_{DD}$ - 0.2V or $V_{IN} \leq$ 0.2V, Active Port, Outputs Disabled, f = f_{MAX}(1)	COM'L	L	140	240	130	200	100	140	90	130	mA
			IND	L	—	—	130	230	—	—	—	—	

5648 tbl 09

NOTES:
1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{DD} = 3.3V, T_A = 25°C for Typ, and are not production tested. $I_{DD DC}$(f=0) = 90mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X \leq$ 0.2V means $\overline{CE}_{0X} \leq$ 0.2V and $CE_{1X} \geq V_{DD}$ - 0.2V
   $\overline{CE}_X \geq V_{DD}$ - 0.2V means $\overline{CE}_{0X} \geq V_{DD}$ - 0.2V or $CE_{1X} \leq$ 0.2V
   "X" represents "L" for left port or "R" for right port.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2, and 3

5648 tbl 10

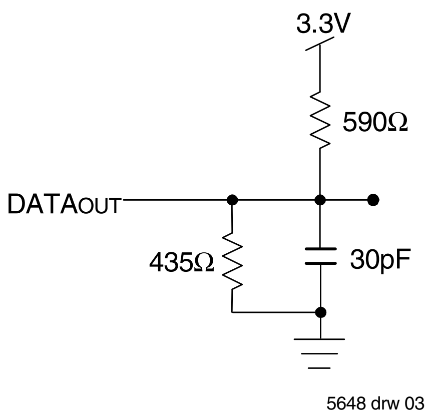


Figure 1. AC Output Test load.

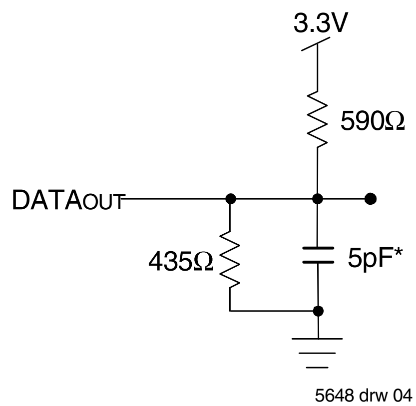


Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.

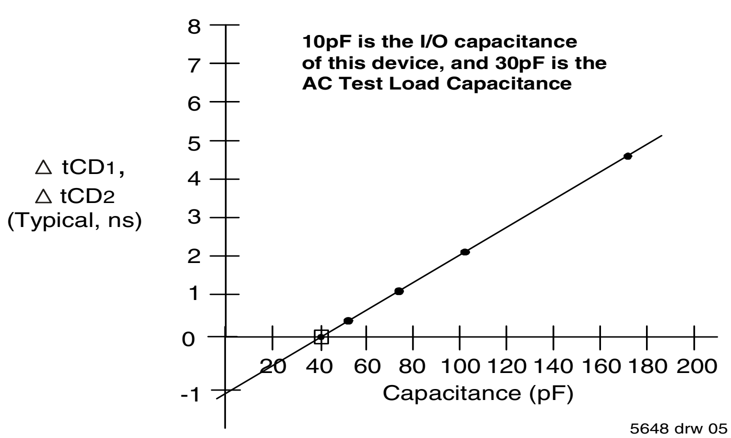


Figure 3. Typical Output Derating (Lumped Capacitive Load).

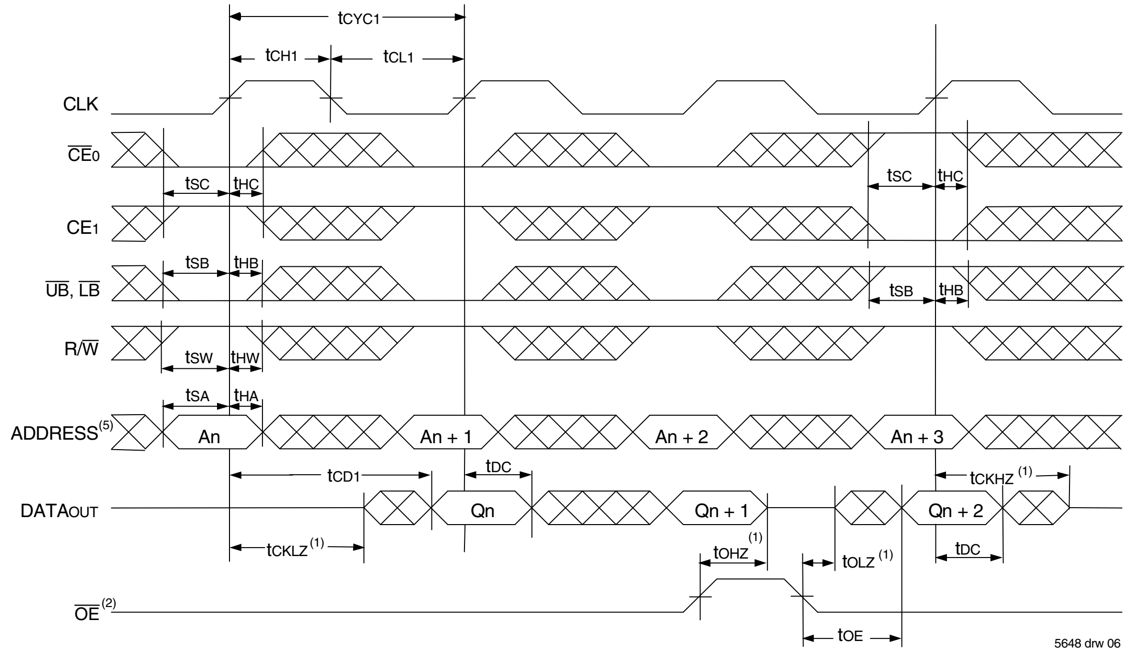
AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)(3) (V_{DD} = 3.3V ± 0.3V)

		70V9369L6 Com'l Only		70V9369L7 Com'l Only & Ind		70V9369L9 Com'l Only		70V9369L12 Com'l Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{CYC1}	Clock Cycle Time (Flow-Through)(2)	19	—	22	—	25	—	30	—	ns
t_{CYC2}	Clock Cycle Time (Pipelined)(2)	10	—	12	—	15	—	20	—	ns
t_{CH1}	Clock High Time (Flow-Through)(2)	6.5	—	7.5	—	12	—	12	—	ns
t_{CL1}	Clock Low Time (Flow-Through)(2)	6.5	—	7.5	—	12	—	12	—	ns
t_{CH2}	Clock High Time (Pipelined)(2)	4	—	5	—	6	—	8	—	ns
t_{CL2}	Clock Low Time (Pipelined)(2)	4	—	5	—	6	—	8	—	ns
t_R	Clock Rise Time	—	3	—	3	—	3	—	3	ns
t_F	Clock Fall Time	—	3	—	3	—	3	—	3	ns
t_{SA}	Address Setup Time	3.5	—	4	—	4	—	4	—	ns
t_{HA}	Address Hold Time	0	—	0	—	1	—	1	—	ns
t_{SC}	Chip Enable Setup Time	3.5	—	4	—	4	—	4	—	ns
t_{HC}	Chip Enable Hold Time	0	—	0	—	1	—	1	—	ns
t_{SW}	R/W Setup Time	3.5	—	4	—	4	—	4	—	ns
t_{HW}	R/W Hold Time	0	—	0	—	1	—	1	—	ns
t_{SD}	Input Data Setup Time	3.5	—	4	—	4	—	4	—	ns
t_{HD}	Input Data Hold Time	0	—	0	—	1	—	1	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	3.5	—	4	—	4	—	4	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	0	—	0	—	1	—	1	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	3.5	—	4	—	4	—	4	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0	—	0	—	1	—	1	—	ns
t_{SRST}	$\overline{CNTRST}$ Setup Time	3.5	—	4	—	4	—	4	—	ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	0	—	0	—	1	—	1	—	ns
t_{OE}	Output Enable to Data Valid	—	6.5	—	7.5	—	9	—	12	ns
t_{OLZ}	Output Enable to Output Low-Z(1)	2	—	2	—	2	—	2	—	ns
t_{OHZ}	Output Enable to Output High-Z(1)	1	7	1	7	1	7	1	7	ns
t_{CD1}	Clock to Data Valid (Flow-Through)(2)	—	15	—	18	—	20	—	25	ns
t_{CD2}	Clock to Data Valid (Pipelined)(2)	—	6.5	—	7.5	—	9	—	12	ns
t_{DC}	Data Output Hold After Clock High	2	—	2	—	2	—	2	—	ns
t_{CKHZ}	Clock High to Output High-Z(1)	2	9	2	9	2	9	2	9	ns
t_{CKLZ}	Clock High to Output Low-Z(1)	2	—	2	—	2	—	2	—	ns
Port-to-Port Delay										
t_{CWDD}	Write Port Clock High to Read Data Delay	—	24	—	28	—	35	—	40	ns
t_{CCS}	Clock-to-Clock Setup Time	—	9	—	10	—	15	—	15	ns

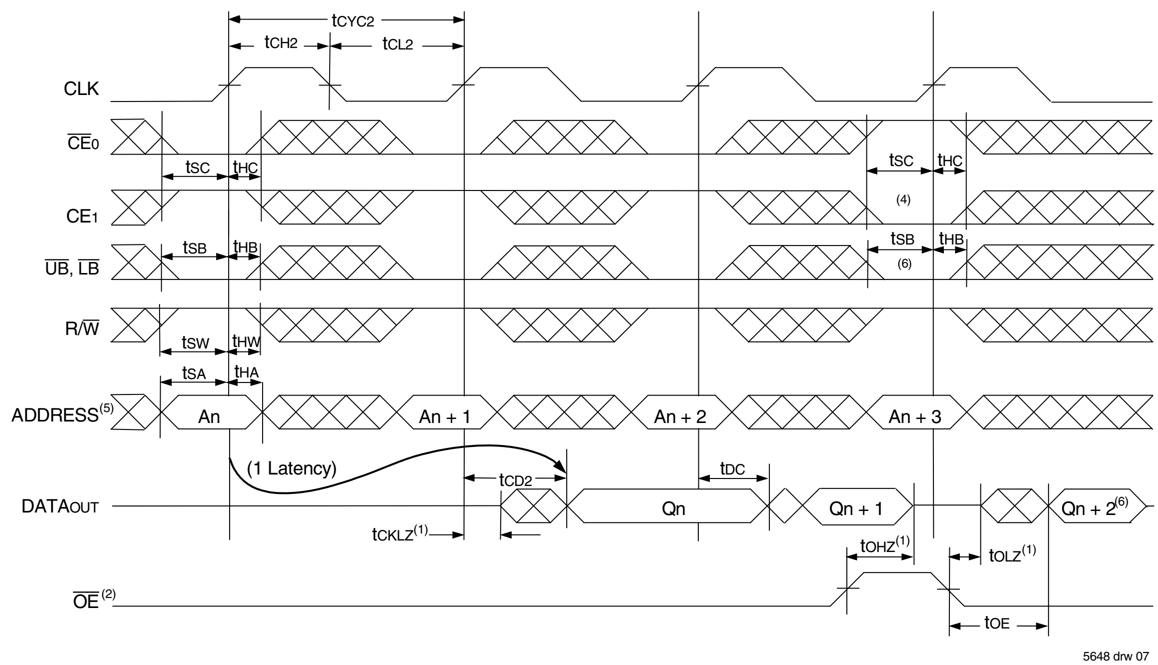
5648 tbl 11

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both the Left and Right ports when $\overline{FT}$/PIPE = V_{IH}. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}$/PIPE = V_{IL} for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$), $\overline{FT}$/PIPER, and $\overline{FT}$/PIPEL.

Timing Waveform of Read Cycle for Flow-Through Output ($\overline{FT}$/PIPE"X" = VIL)(3,7)

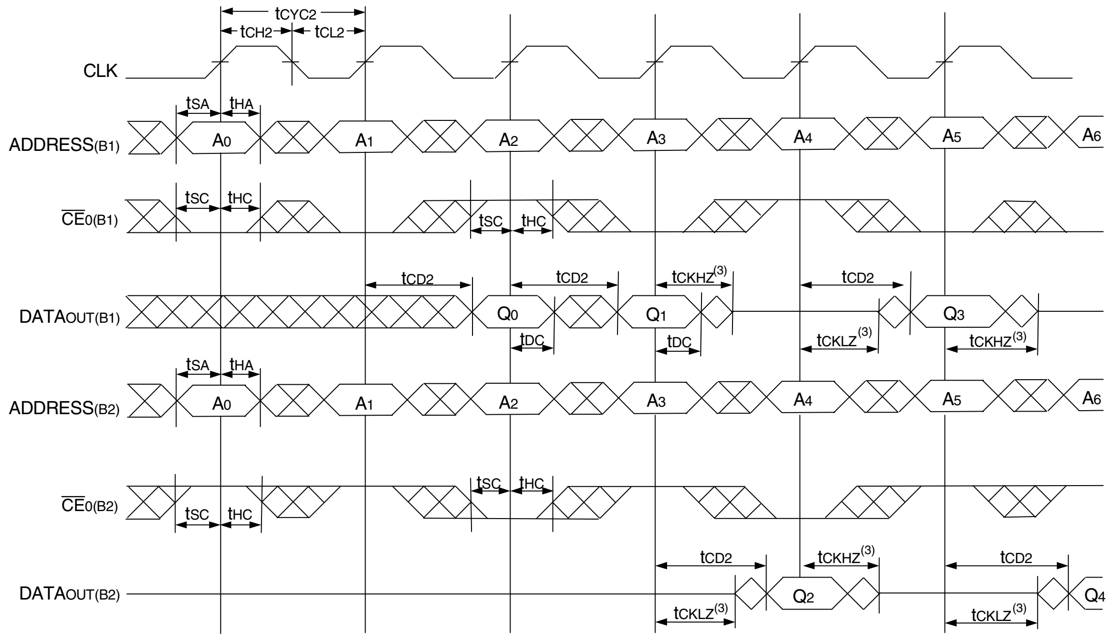


Timing Waveform of Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE"X" = VIH)(3,7)



NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{ADS}$ = VIL and $\overline{CNTRST}$ = VIH.
4. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = VIH, CE1 = VIL, $\overline{UB}$ = VIH, or $\overline{LB}$ = VIH following the next rising edge of the clock. Refer to Notes under Pin Names Table.
5. Addresses do not have to be accessed sequentially since ADS = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. If $\overline{UB}$ or $\overline{LB}$ was HIGH, then the Upper Byte and/or Lower Byte of DATAOUT for Qn + 2 would be disabled (High-Impedance state).
7. "X' here denotes Left or Right port. The diagram is with respect to that port.

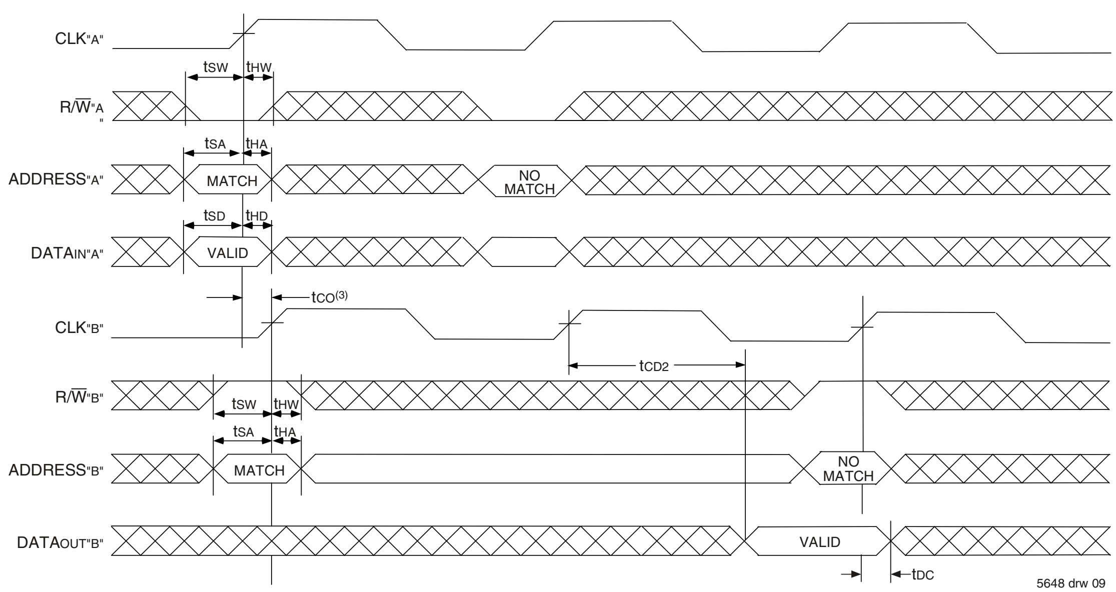
Timing Waveform of a Bank Select Pipelined Read[1,2]



NOTES:

1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT70V9369 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{UB}$, $\overline{LB}$, $\overline{OE}$, and $\overline{ADS}$ = V_{IL}; CE1(B1), CE1(B2), R/$\overline{W}$ and $\overline{CNTRST}$ = V_{IH}.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V_{IL}; CE_1 and $\overline{CNTRST}$ = V_{IH}.
5. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
6. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}.
   If t_{CCS} > maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD1}$. t_{CWDD} does not apply in this case.
7. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite from Port "A".

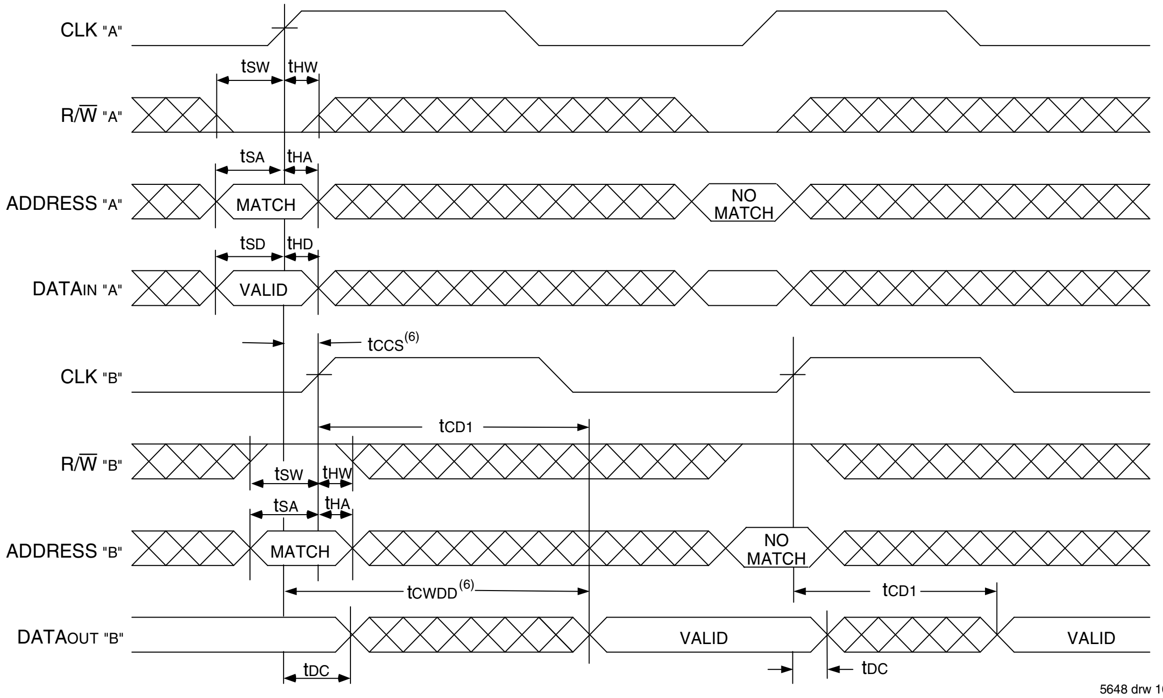
Timing Waveform of Left Port Write to Pipelined Right Port Read[1,2,4]



NOTES:

1. $\overline{CE}_0$, $\overline{BE}_n$, and $\overline{ADS}$ = V_{IL}; CE_1 and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for Port "B", which is being read from. $\overline{OE}$ = V_{IH} for Port "A", which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + 2t_{CYC2} + t_{CD2}$). If t_{CO} > minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + t_{CYC2} + t_{CD2}$).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A"

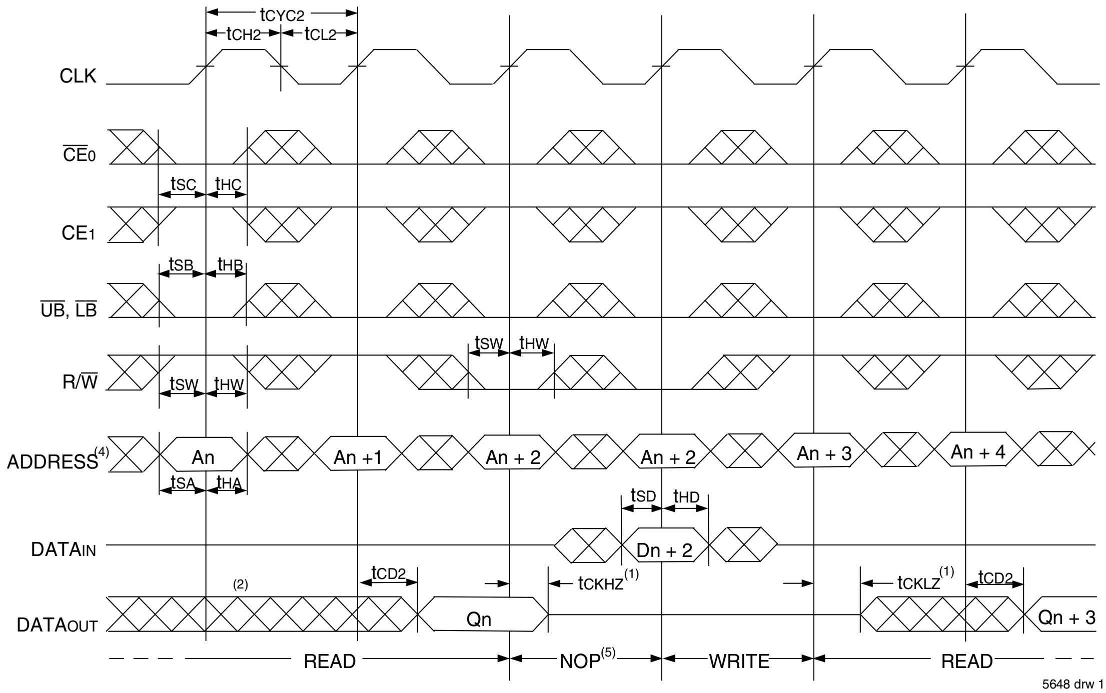
Timing Waveform with Port-to-Port Flow-Through Read(4,5,7)



NOTES:

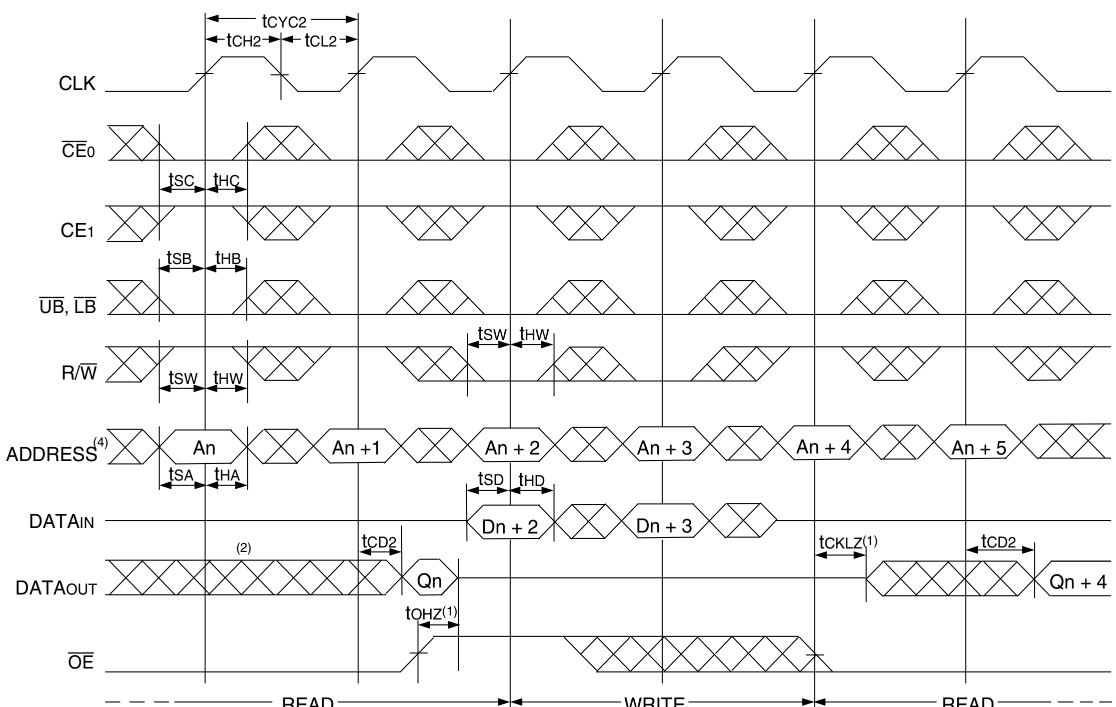
1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT70V9369 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{UB}$, $\overline{LB}$, $\overline{OE}$, and $\overline{ADS}$ = V_{IL}; $CE_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$ and $\overline{CNTRST}$ = V_{IH}.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V_{IL}; CE_1 and $\overline{CNTRST}$ = V_{IH}.
5. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
6. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}.
   If t_{CCS} > maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD1}$. t_{CWDD} does not apply in this case.
7. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite from Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = VIL)(3)



5648 drw 11

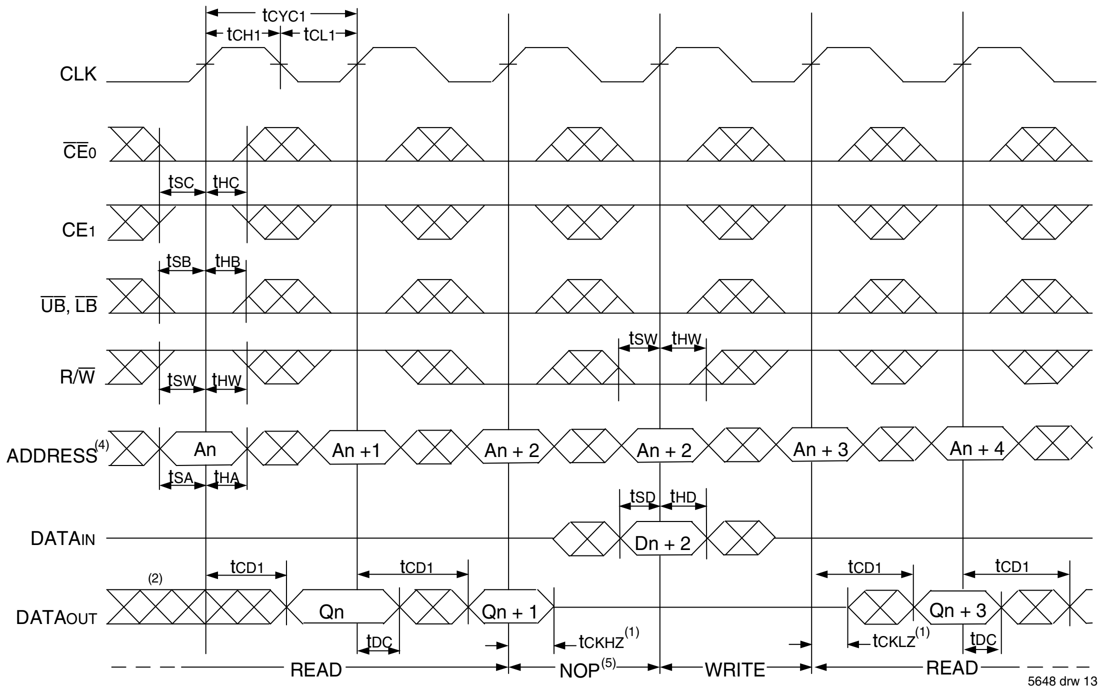
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)(3)



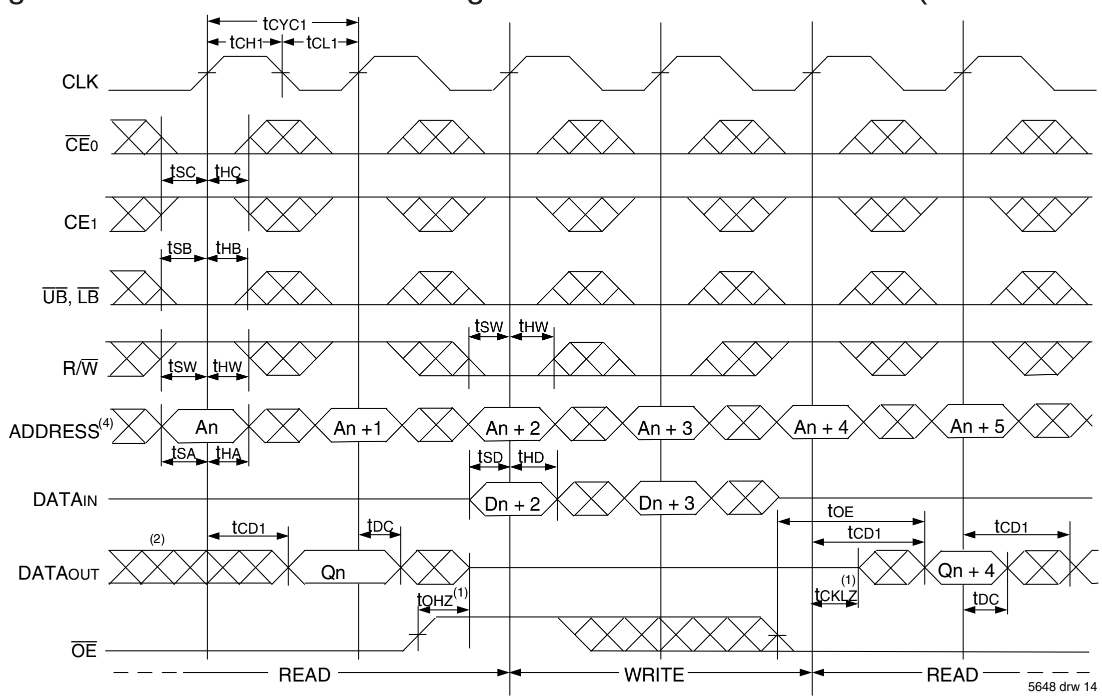
5648 drw 12

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = VIL; CE1 and $\overline{CNTRST}$ = VIH. "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{\text{OE}}$ = VIL)(3)

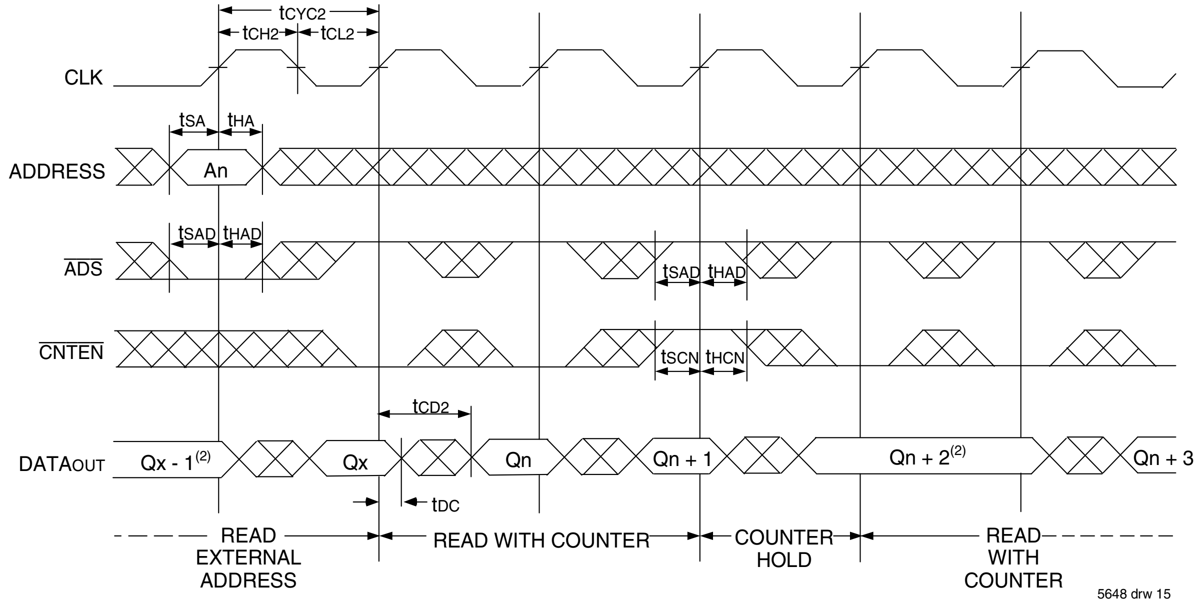


Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{\text{OE}}$ Controlled)(3)

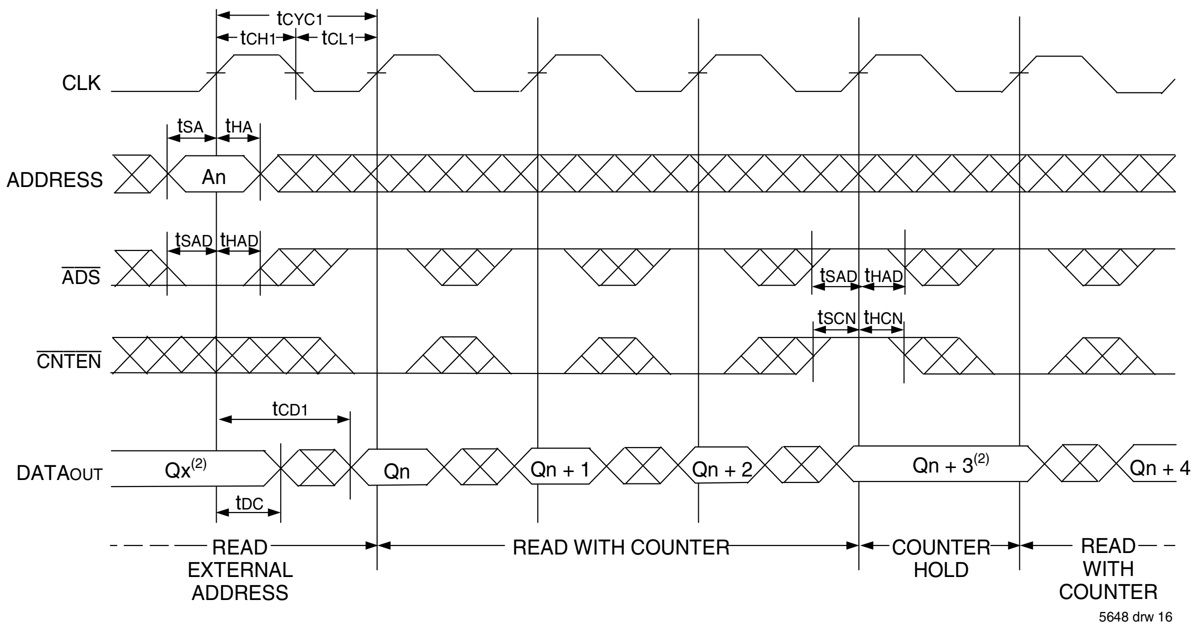


NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{\text{CE}}$0, $\overline{\text{UB}}$, $\overline{\text{LB}}$, and $\overline{\text{ADS}}$ = VIL; CE1 and $\overline{\text{CNTRST}}$ = VIH. "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since $\overline{\text{ADS}}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance[(1)]



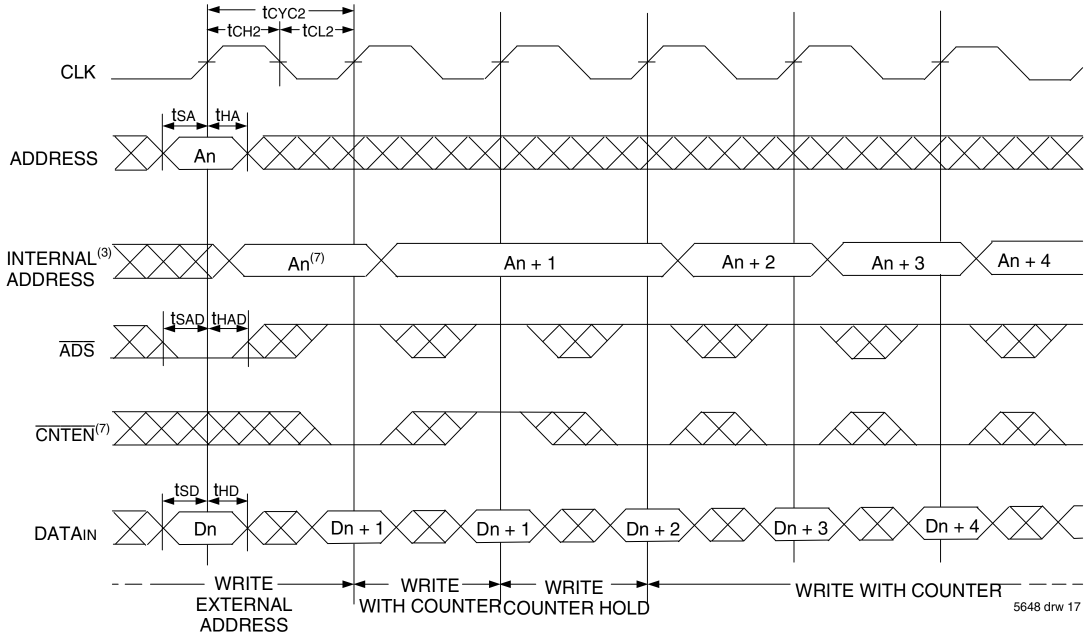
Timing Waveform of Flow-Through Read with Address Counter Advance[(1)]



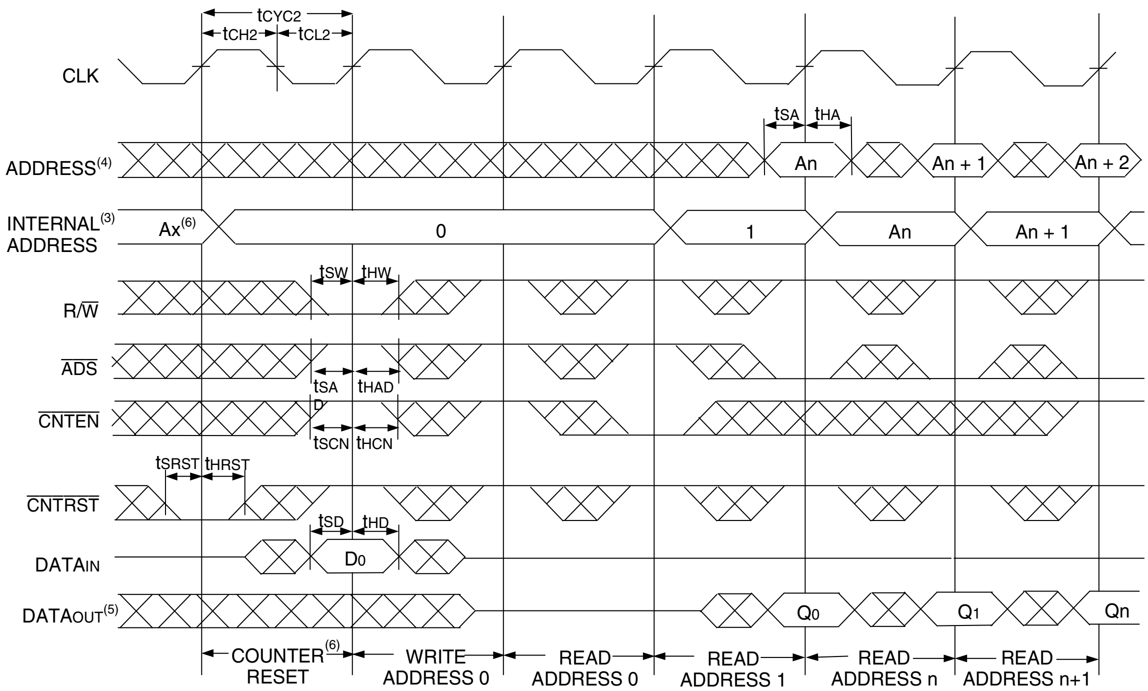
NOTES:

1. $\overline{CE}_0$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$ = V_{IL}; CE_1, R/$\overline{W}$, and $\overline{CNTRST}$ = V_{IH}.
2. If there is no address change via $\overline{ADS}$ = V_{IL} (loading a new address) or $\overline{CNTEN}$ = V_{IL} (advancing the address), i.e. $\overline{ADS}$ = V_{IH} and $\overline{CNTEN}$ = V_{IH}, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)(1)



Timing Waveform of Counter Reset (Pipelined Outputs)(2)



NOTES:

1. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{CNTRST}$ = V_{IH}.
2. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$ = V_{IL}; CE_1 = V_{IH}.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle. $ADDR_0$ will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN}$ = V_{IL} advances Internal Address from ‘An’ to ‘An +1’. The transition shown indicates the time required for the counter to advance. The ‘An +1’ Address is written to during this cycle.

Functional Description

The IDT70V9369 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to staff the operation of the address counters for fast interleaved memory applications.

$\overline{CE}_0 = V_{IL}$ and $CE_1 = V_{IH}$ for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V9369's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{CE}_0 = V_{IL}$ and $CE_1 = V_{IH}$ to re-activate the outputs.

Depth and Width Expansion

The IDT70V9369 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V9369 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 36-bit or wider applications.

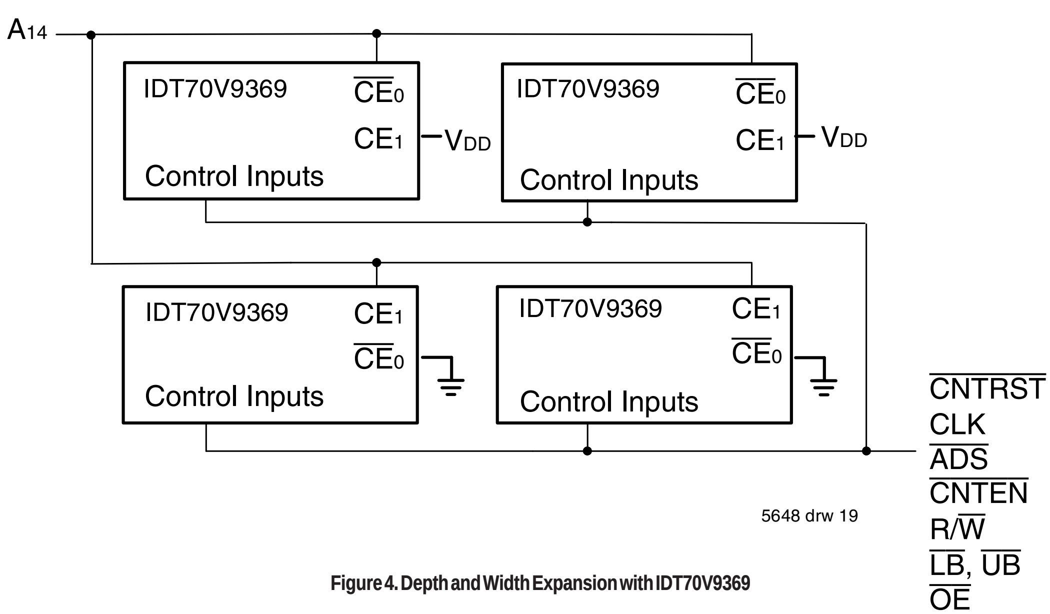
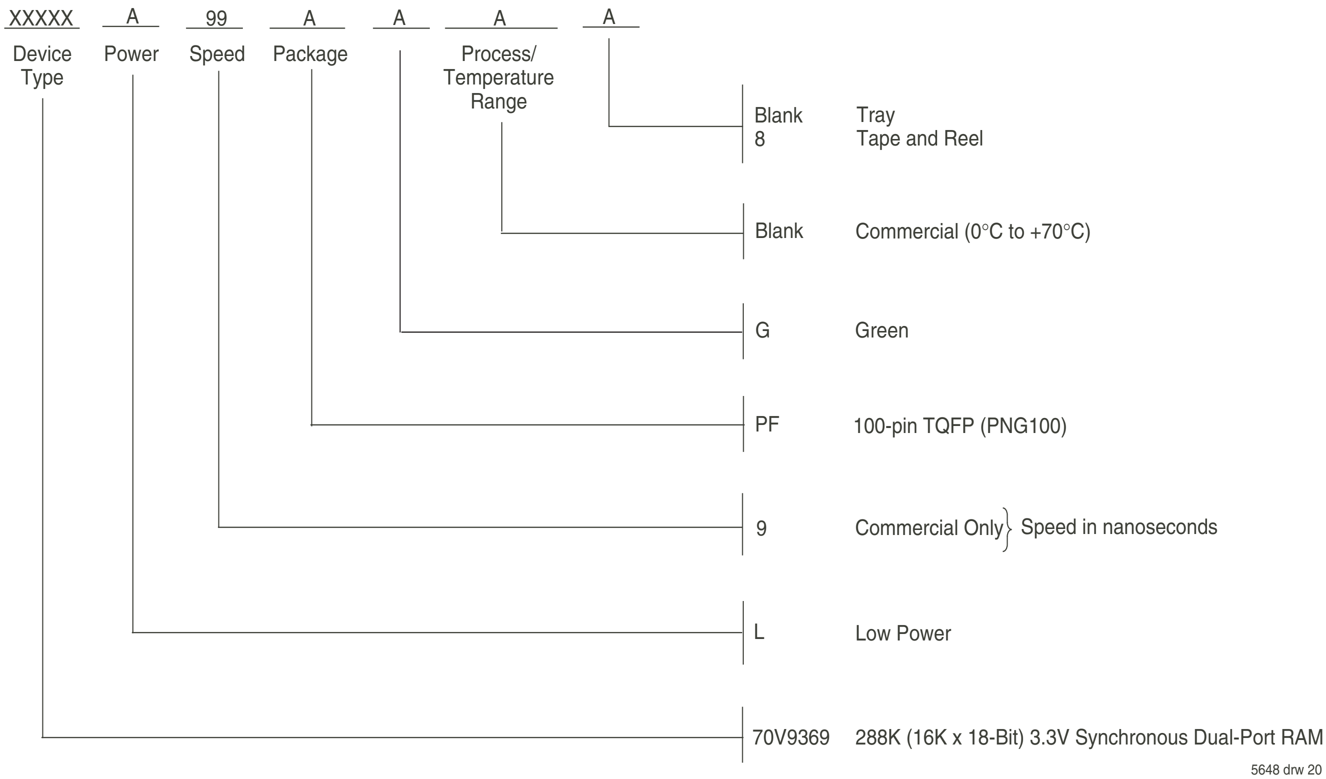


Figure 4. Depth and Width Expansion with IDT70V9369

Ordering Information



NOTES:

LEAD FINISH (SnPb) parts are Obsolete. Product Discontinuation Notice - PDN# SP-17-02

Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
9	70V9369L9PFG	PNG100	TQFP	C
	70V9369L9PFG8	PNG100	TQFP	C

Datasheet Document History

01/08/02:		Initial Public Release
10/11/04:		Removed "Preliminary" status
	Page 4	Updated Truth Table II
		Updated Absolute Maximum Ratings
		Updated Capacitance table
	Page 5	Added 6ns speed grade and 7ns I-temp, removed 9ns I-temp and updated DC power numbers in the DC Electrical Characteristics Table
	Page 7	Added 6ns speed grade and 7ns I-temp and removed 9ns I-temp AC timing numbers from the AC Electrical Characteristics Table
		Updated t_{OE} for 7ns and 9ns speed grades
	Page 9	Added Timing Waveform of Left Port Write to Pipelined Right Port Read
	Page 16	Added 6ns speed grade and 7ns I-temp and removed 9ns I-temp to ordering information
	Page 1 & 16	Replaced old TM logo with new TM logo
10/23/08:	Page 16	Removed "IDT" from orderable part number
07/26/10:	Page 1	Added green parts availability to features
	Page 16	Added green indicator to ordering information
	Page 7	In order to correct the header notes of the AC Elect Chars Table and align them with the Industrial temp range values located in the table, the commercial T_A header note has been removed
	Pages 8-12	In order to correct the footnotes of timing diagrams, $\overline{CNTEN}$ has been removed to reconcile the footnotes witht he $\overline{CNTEN}$ logic definition found in Truth Table II - Address Counter Control
06/20/15:	Page 2	Removed IDT in reference to fabrication
	Page 2	Removed date for the 100-PIN TQFP configuration
	Page 2 & 16	The package code PN100-1 changed to PN100 to match standard package codes
	Page 6	Corrected typo in the Typical Output Derating drawing
	Page 16	Added Tape and Reel indicator to Ordering Information
02/22/18:		Product Discontinuation Notice - PDN# SP-17-02
		Last time buy expires June 15, 2018
11/14/19:	Page 2	Rotated PNG100 TQFP pin configuration to accurately reflect pin 1 orientation
	Page 16	Added Orderable Part Information table

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