USB2517/USB2517I

USB 2.0 Hi-Speed 7-Port Hub Controller

General Description

The 7-Port Hub is a low power, OEM configurable, MTT (multi transaction translator) hub controller IC with 7 downstream ports for embedded USB solutions. The 7-port hub is fully compliant with the USB 2.0 Specification and will attach to an upstream port as a Full-Speed Hub or as a Full-/Hi-Speed Hub. The 7-Port Hub supports Low-Speed, Full-Speed, and Hi-Speed (if operating as a Hi-Speed Hub) downstream devices on all of the enabled downstream ports.

General Features

- Hub Controller IC with 7 downstream ports
- High-performance multiple transaction translator MultiTRAK™ Technology provides one transaction translator per port
- Enhanced OEM configuration options available through either a single serial I^2C EEPROM, or SMBus Slave Port
- 64-Pin (9x9 mm) QFN, RoHS compliant package
- Supports commercial (0ºC to +70ºC) and industrial (-40ºC to +85ºC) temperature ranges

Hardware Features

- Low power operation
- Full Power Management with individual or ganged power control of each downstream port
- On-chip Power On Reset (POR)
- Internal 1.8V Voltage Regulator
- Fully integrated USB termination and Pull-up/Pull-down resistors
- On Board 24MHz Crystal Driver, Resonator, or External 24/MHz clock input
- USB host/device speed indicator. Per-port 3-color LED drivers indicate the speed of USB host and device connection - hi-speed (480 Mbps), full-speed (12 Mbps), low-speed (1.5 Mbps)
- Enhanced EMI rejection and ESD protection performance

OEM Selectable Features

- Customizable Vendor ID, Product ID, and Device ID
- Select whether the hub is part of a compound device (When any downstream port is permanently hardwired to a USB peripheral device, the hub is part of a compound device.)
- Flexible port mapping and disable sequence. Ports can be disabled/reordered in any order to support multiple product SKUs. Hub will automatically reorder the remaining ports to match the Host controller's numbering scheme
- Programmable USB differential-pair pin location
  - Eases PCB layout by aligning USB signal lines directly to connectors
- Programmable USB signal drive strength. Recover USB signal integrity due to compromised system environments using 4-level driving strength resolution
- Select the presence of a permanently hardwired USB peripheral device on a port by port basis
- Configure the delay time for filtering the over-current sense inputs
- Configure the delay time for turning on downstream port power
- Indicate the maximum current that the 347-port hub consumes from the USB upstream port
- Indicate the maximum current required for the hub controller
- Support Custom String Descriptor up to 31 characters in length for:
  - Product String
  - Manufacturer String
  - Serial Number String
- Pin Selectable Options for Default Configuration
  - Select Downstream Ports as Non-Removable Ports
  - Select Downstream Ports as Disabled Ports
  - Select Downstream Port Power Control and Over-Current Detection on a Ganged or Individual Basis
  - Select USB Signal Drive Strength
  - Select USB Differential Pair Pin location

Applications

- LCD monitors and TVs
- Multi-function USB peripherals
- PC mother boards
- Set-top boxes, DVD players, DVR/PVR
- Printers and scanners
- PC media drive bay
- Portable hub boxes
- Mobile PC docking
- Embedded systems

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1.0 ACRONYMS & DEFINITIONS

EEPROMM: Electrically Erasable Programmable Read-Only Memory (a type of non-volatile memory)

EMI: Electromagnetic Interference

ESD: Electrostatic Discharge

I^2C: Inter-Integrated Circuit

LCD: Liquid Crystal Display

LED: Light Emitting Diode

OCS: Over-current sense

PCB: Printed Circuit Board

PHY: Physical Layer

PLL: Phase-Locked Loop

PVR: Personal Video Recorder (also known as a Digital Video Recorder)

QFN: Quad Flat No Leads

RoHS: Restriction of Hazardous Substances Directive

SCK: Serial Clock

SD: Secure Digital

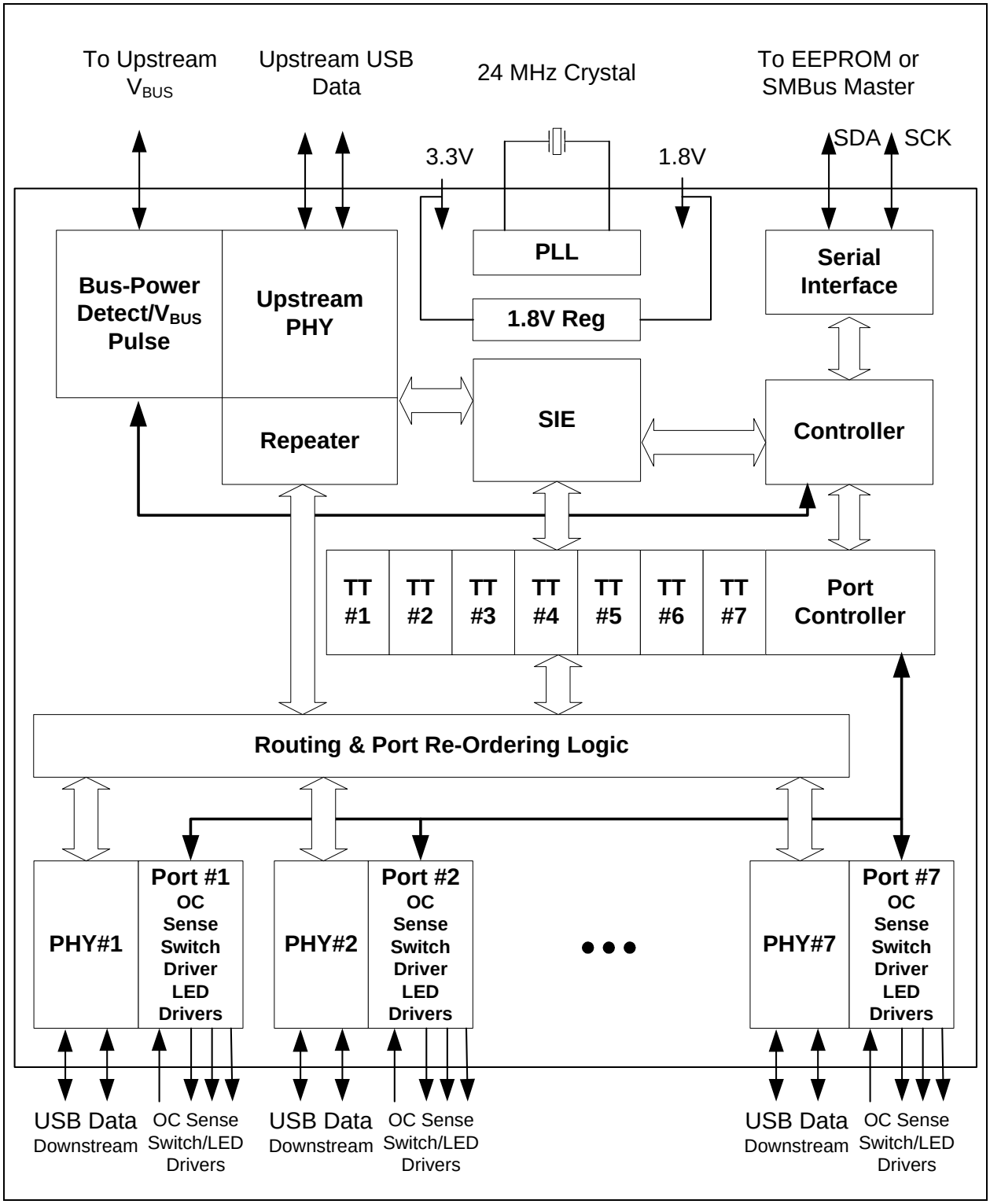
SIE: Serial Interface Engine

SMBus: System Management Bus

TT: Transaction Translator

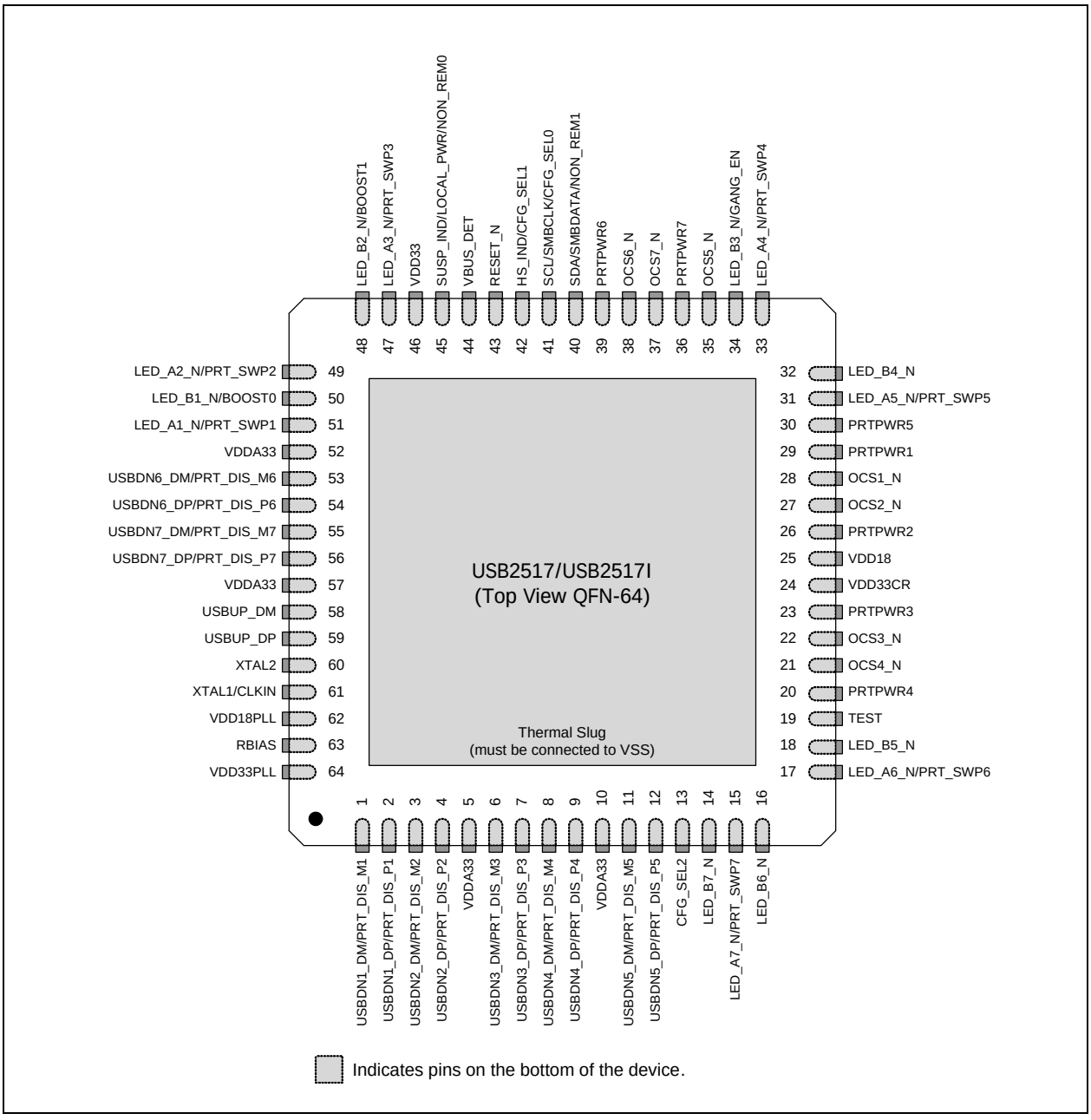
2.0 BLOCK DIAGRAM

FIGURE 2-1: USB2517/USB2517I BLOCK DIAGRAM



3.0 PIN CONFIGURATION

FIGURE 3-1: USB2517I 64-PIN QFN DIAGRAM



4.0 PIN TABLE

4.1 64-Pin List

TABLE 4-1: USB2517I 64-PIN TABLE

Upstream USB 2.0 Interfaces (3 pins)			
USBUP_DP	**USBUP_DM**	**VBUS_DET**	
Downstream 7-Port USB 2.0 Interfaces (43 Pins)			
USBDN1_DP/ PRT_DIS_P1	USBDN2_DP/ PRT_DIS_P2	USBDN3_DP/ PRT_DIS_P3	USBDN4_DP/ PRT_DIS_P4
USBDN5_DP/ PRT_DIS_P5	USBDN6_DP/ PRT_DIS_P6	USBDN7_DP/ PRT_DIS_P7	USBDN1_DM/ PRT_DIS_M1
USBDN2_DM/ PRT_DIS_M2	USBDN3_DM/ PRT_DIS_M3	USBDN4_DM/ PRT_DIS_M4	USBDN5_DM/ PRT_DIS_M5
USBDN6_DM/ PRT_DIS_M6	USBDN7_DM/ PRT_DIS_M7	LED_A1_N/ PRT_SWP1	LED_A2_N/ PRT_SWP2
LED_A3_N/ PRT_SWP3	LED_A4_N/ PRT_SWP4	LED_A5_N/ PRT_SWP5	LED_A6_N/ PRT_SWP6
LED_A7_N/ PRT_SWP7	LED_B1_N/ BOOST0	LED_B2_N/ BOOST1	LED_B3_N/ GANG_EN
LED_B4_N	LED_B5_N	LED_B6_N	LED_B7_N
PRTPWR1	PRTPWR2	PRTPWR3	PRTPWR4
PRTPWR5	PRTPWR6	PRTPWR7	OCS1_N
OCS2_N	OCS3_N	OCS4_N	OCS5_N
OCS6_N	OCS7_N	RBIAS	
Serial Port Interface (4 Pins)			
SDA/ SMBDATA/ NON_REM1	SCL/ SMBCLK/ CFG_SEL0	HS_IND/ CFG_SEL1	CFG_SEL2
MISC (5 Pins)			
XTAL1/CLKIN	XTAL2	SUSP_IND/ LOCAL_PWR/ NON_REM0	RESET_N
TEST			

TABLE 4-1: USB2517I 64-PIN TABLE (CONTINUED)

Analog Power (6 Pins)			
VDD18PLL	VDD33PLL	(4) VDDA33	
Digital Power, Ground (3 Pins)			
VDD33	VDD18	VDD33CR	
Total 64			

5.0 PIN DESCRIPTIONS AND BUFFER TYPE DESCRIPTIONS

5.1 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “N” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “N” is not present before the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

TABLE 5-1: USB2517/USB2517I PIN DESCRIPTIONS

Symbol	64 QFN	Buffer Type	Description
Upstream USB Interfaces			
USBUP_DP USBUP_DM	59 58	IO-U	USB Bus Data These pins connect to the upstream USB bus data signals (Host port, or upstream hub).
VBUS_DET	44	I/O12	Detect Upstream VBUS Power Detects state of Upstream VBUS power. The MCHP Hub monitors VBUS_DET to determine when to assert the internal D+ pull-up resistor (signaling a connect event). When designing a detachable hub, this pin must be connected to the VBUS power pin of the USB port that is upstream from the hub. For self-powered applications with a permanently attached host, this pin must be connected to 3.3V or 5.0V (typically VDD33).
Downstream 7-Port USB 2.0 Interfaces			
USBDN[7:1]_DP/ PRT_DIS_P[7:1] & USBDN[7:1]_DM/ PRT_DIS_M[7:1]	56 54 12 9 7 4 2 55 53 11 8 6 3 1	IO-U	Hi-Speed USB Data & Port Disable Strap Option USBDN_DP[7:1] / USBDN_DM[7:1]: These pins connect to the downstream USB peripheral devices attached to the hub’s port. Downstream Port Disable Strap option: PRT_DIS_P[7:1] / PRT_DIS_M[7:1]: If the strap is enabled by package and configuration settings (see Table 5-2), this pin will be sampled at RESET_N negation to determine if the port is disabled. To disable, pull up with 10K resistor to 3.3V.
PRTPWR[7:1]	36 39 30 20 23 26 29	O12	USB Power Enable Enables power to USB peripheral devices downstream. **Note:** The hub supports active high power controllers only!

TABLE 5-1: USB2517/USB2517I PIN DESCRIPTIONS (CONTINUED)

Symbol	64 QFN	Buffer Type	Description
LED_A[7:1]_N/ PRT_SWP[7:1]	15 17 31 33 47 49 51	I/O12	Port LED Indicators & Port Swap strapping option Indicator LED for ports 1-7. Will be active low when LED support is enabled via EEPROM or SMBus.
			If this strap is enabled by package and configuration settings (see Table 5-2), this pin will be sampled at RESET_N negation to determine the electrical connection polarity of the downstream USB Port pins (USB_DP and USB_DM). Also, the active state of the LED will be determined as follows: '0' = Port Polarity is normal, LED is active high. '1' = Port Polarity (USB_DP and USB_DM) is swapped, LED is active low.
LED_B[7:4]_N	14 16 18 32	I/O12	Enhanced Indicator Port 4-7 LED Enhanced Indicator LED for ports 4-7. Will be active low when LED support is enabled via EEPROM or SMBus.
LED_B3_N/ GANG_EN	34	I/O12	Enhanced Port 3 LED, Gang Power, and Over-current Strap Option Enhanced Indicator LED for port 3. Will be active low when LED support is enabled via EEPROM or SMBus.
			GANG_EN: Selects between Gang or Individual Port power and Over-current sensing. If this strap is enabled by package and configuration settings (see Table 5-2), this pin will be sampled at RESET_N negation to determine the mode as follows: '0' = Individual sensing & switching, and LED_B3_N is active high. '1' = Ganged sensing & switching, and LED_B3_N is active low.

TABLE 5-1: USB2517/USB2517I PIN DESCRIPTIONS (CONTINUED)

Symbol	64 QFN	Buffer Type	Description
LED_B[2:1]_N/ BOOST[1:0]	48 50	I/O12	Enhanced Port [2:1] LED & PHY Boost strapping option Enhanced Indicator LED for ports 1 & 2. Will be active low when LED support is enabled via EEPROM or SMBus.
			BOOST[1:0]: If this strap is enabled by package and configuration settings (see Table 5-2), this pin will be sampled at RESET_N negation to determine if all PHY ports (upstream and downstream) operate at a normal or boosted electrical level. Also, the active state of the LEDs will be determined as follows: See Section 7.2.1.26, "Register F6h: Boost_Up" and Section 7.2.1.28, "Register F8h: Boost_4:0". BOOST[1:0] = BOOST_IOUT[1:0] BOOST[1:0] = ‘00’, LED_B2_N is active high, LED_B1_N is active high. BOOST[1:0] = ‘01’, LED_B2_N is active high, LED_B1_N is active low. BOOST[1:0] = ‘10’, LED_B2_N is active low, LED_B1_N is active high. BOOST[1:0] = ‘11’, LED_B2_N is active low, LED_B1_N is active low.
OCS[7:1]_N	37 38 35 21 22 27 28	IPU	Over-current Sense Input from external current monitor indicating an over-current condition. {Note: Contains internal pull-up to 3.3V supply}
RBIAS	63	I-R	USB Transceiver Bias A 12.0kΩ (+/- 1%) resistor is attached from the ground to this pin to set the transceiver’s internal bias settings.

TABLE 5-1: USB2517/USB2517I PIN DESCRIPTIONS (CONTINUED)

Symbol	64 QFN	Buffer Type	Description
Serial Port Interface			
SDA/ SMBDATA/ NON_REM1	40	I/OSD12	Serial Data / SMB Data NON_REM1: Non-removable port strap option. If this strap is enabled by package and configuration settings (see Table 5-2) this pin will be sampled (in conjunction with SUSP_IND/ LOCAL_PWR/NON_REM0) at RESET_N negation to determine if ports [3:1] contain permanently attached (non-removable) devices: NON_REM[1:0] = ‘00’, All ports are removable, NON_REM[1:0] = ‘01’, Port 1 is non-removable, NON_REM[1:0] = ‘10’, Ports 1 & 2 are non-removable, NON_REM[1:0] = ‘11’, Ports 1, 2 & 3 are non-removable.
SCL/ SMBCLK/ CFG_SEL0	41	I/OSD12	Serial Clock (SCL) SMBus Clock (SMBCLK) Configuration Select_SEL0: The logic state of this multifunctional pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in Table 5-2, "USB2517I SMBUS or EEPROM Interface Behavior".
HS_IND/ CFG_SEL1	42	I/O12	Hi-Speed Upstream port indicator & Configuration Programming Select HS_IND: High Speed Indicator for upstream port connection speed. The active state of the LED will be determined as follows: CFG_SEL1 = ‘0’, HS_IND is active high, CFG_SEL1 = ‘1’, HS_IND is active low, ‘Asserted’ = Hub is connected at HS ‘Negated’ = Hub is connected at FS CFG_SEL1: The logic state of this pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in Table 5-2, "USB2517I SMBUS or EEPROM Interface Behavior".
CFG_SEL2	13	I	Configuration Programming Select This pin is not available in all packages; it is held to a logic ‘0’ when not available. The logic state of this pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in Table 5-2, "USB2517I SMBUS or EEPROM Interface Behavior".

TABLE 5-1: USB2517/USB2517I PIN DESCRIPTIONS (CONTINUED)

Symbol	64 QFN	Buffer Type	Description
			MISC
XTAL1/ CLKIN	61	ICLKx	Crystal Input/External Clock Input 24MHz crystal or external clock input. This pin connects to either one terminal of the crystal or to an external 24MHz clock when a crystal is not used.
XTAL2	60	OCLKx	Crystal Output 24MHz Crystal This is the other terminal of the crystal. It can be treated as a no connect when an external clock source is used to drive XTAL1/ CLKIN. This output must not be used to drive any external circuitry other than the crystal circuit.
RESET_N	43	IS	RESET Input The system can reset the chip by driving this input low. The minimum active low pulse is 1 µs. When the RESET_N pin is pulled to VDD33, the internal POR (Power on Reset) is enabled and no external reset circuitry is required. The internal POR holds the internal logic in reset until the power supplies are stable.
SUSP_IND/ LOCAL_PWR/ NON_REM0	45	I/O12	Active/Suspend status LED or Local-Power & Non-Removable Strap Option Suspend Indicator: Indicates the USB state of the hub. ‘negated’ = Unconfigured or configured and in USB suspend ‘asserted’ = Hub is configured, and is active (i.e., not in suspend)
			Local Power: Detects availability of local self-power source. Low = Self/local power source is NOT available (i.e., Hub gets all power from the upstream USB VBus). High = Self/local power source is available. NON_REM0 Strap Option: If this strap is enabled by package and configuration settings (see Table 5-2, "USB2517I SMBUS or EEPROM Interface Behavior"), this pin will be sampled (in conjunction with NON_REM1) at RESET_N negation to determine if ports [3:1] contain permanently attached (non-removable) devices. Also, the active state of the LED will be determined as follows: NON_REM[1:0] = ‘00’, All ports are removable, and the LED is active high NON_REM[1:0] = ‘01’, Port 1 is non-removable, and the LED is active low NON_REM[1:0] = ‘10’, Ports 1 & 2 are non-removable, and the LED is active high NON_REM[1:0] = ‘11’, Ports 1, 2 & 3 are non-removable, and the LED is active low

TABLE 5-1: USB2517/USB2517I PIN DESCRIPTIONS (CONTINUED)

Symbol	64 QFN	Buffer Type	Description
TEST	19	IPD	TEST pin XNOR continuity tests all signal pins on the hub. Please contact your MCHP representative for a detailed description of how this test mode is enabled and utilized.
Power, Ground, No Connect			
VDD18	25		VDD Core +1.8V core power. This pin must have a 1.0µF (or greater) ±20% (ESR <0.1Ω) capacitor to VSS.
VDD33PLL	64		VDD 3.3 PLL Regulator Reference +3.3V power supply for the Digital I/O. If the internal PLL 1.8V regulator is enabled, then this pin acts as the regulator input.
VDD18PLL	62		VDD PLL +1.8V Filtered analog power for internal PLL. This pin must have a 1.0µF (or greater) ±20% (ESR <0.1Ω) capacitor to VSS.
VDD33	46		VDD I/O +3.3V Digital I/O power
VDDA33	5 10 52 57		VDD Analog I/O +3.3V Filtered analog PHY power which is shared between adjacent ports.
VDD33CR	24		VDDIO/VDD 3.3 Core Regulator Reference +3.3V power supply for the Digital I/O. If the internal core regulator is enabled, then VDD33CR acts as the regulator input.
Ground	VSS	Slug	Ground

TABLE 5-2: USB2517I SMBUS OR EEPROM INTERFACE BEHAVIOR

CFG_SEL2	CFG_SEL1	CFG_SEL0	SMBus or EEPROM Interface Behavior
0	0	0	Internal Default Configuration • Strap Option sare Enabled
0	0	1	Configured as an SMBus slave for external download of user-defined descriptors • SMBus slave address is ‘0101100’ • Strap Options are Disabled • All Settings are Controlled by Registers
0	1	0	Internal Default Configuration • Strap Options are Enabled • Bus Power Operation • LED Mode = USB

TABLE 5-2: USB2517I SMBUS OR EEPROM INTERFACE BEHAVIOR (CONTINUED)

CFG_SEL2	CFG_SEL1	CFG_SEL0	SMBus or EEPROM Interface Behavior
0	1	1	2-Wire I^2C EEPROMS are supported • Strap Options are Disabled • All Settings are Controlled by Registers
1	0	0	Internal Default Configuration • Strap Options are Disabled • Dynamic Power Switching is Enabled
1	0	1	Internal Default Configuration • Strap Options are Disabled • Dynamic Power Switching is Enabled • LED Mode = USB
1	1	0	Internal Default Configuration • Strap Options are Disabled
1	1	1	Internal Default Configuration • Strap Options are Disabled • LED Mode = USB • Ganged Power Switching • Ganged Over-Current Sensing

5.2 Buffer Type Descriptions

TABLE 5-3: USB2517/USB2517I BUFFER TYPE DESCRIPTIONS

Buffer	Description
I	Input.
IPD	Input with internal weak pull-down resistor.
IPU	Input with internal weak pull-up resistor.
IS	Input with Schmitt trigger.
O12	Output 12mA.
I/O12	Input/Output buffer with 12mA sink and 12mA source.
I/OSD12	Open drain...12mA sink with Schmitt trigger, and must meet I^2C-Bus Specification Version 2.1 requirements.
ICLKx	XTAL clock input.
OCLKx	XTAL clock output.
I-R	RBIAS.
IO-U	Analog Input/Output Defined in USB specification.

6.0 LED USAGE DESCRIPTION

6.1 LED Functionality

The hub supports 2 different (mutually exclusive) LED modes. The USB Mode provides 14 LED's that conform to the USB 2.0 specification functional requirements for Green and Amber LED's. The LED Mode "Speed indicator" provides the downstream device connection speed.

6.1.1 USB MODE 14-WIRE

The LED_A[7:1]_N pins are used to provide Green LED support as defined in the USB 2.0 specification. The LED_B[7:1]_N pins are used to provide Amber LED support as defined in the USB 2.0 specification. The USB Specification defines the LED's as port status indicators for the downstream ports. Please note that no indication of port speed is possible in this mode. The pins are utilized as follows:

- LED_A1_N = Port 1 green LED
- LED_A2_N = Port 2 green LED
- LED_A3_N = Port 3 green LED
- LED_A4_N = Port 4 green LED
- LED_A5_N = Port 5 green LED
- LED_A6_N = Port 6 green LED
- LED_A7_N = Port 7 green LED
- LED_B1_N = Port 1 amber LED
- LED_B2_N = Port 2 amber LED
- LED_B3_N = Port 3 amber LED
- LED_B4_N = Port 4 amber LED
- LED_B5_N = Port 5 amber LED
- LED_B6_N = Port 6 amber LED
- LED_B7_N = Port 7 amber LED

6.1.2 LED MODE SPEED INDICATION

The LED_A[7:1]_N pins are used to provide connection status as well as port speed by using dual color LED's. This scheme requires that the LED's be in the same package, and that a third color is produced so that the user perceives both LED's as being driven "simultaneously".

The LED_A[7:1] pins used in this mode are connected to 7 dual color LED's (each LED pair in a single package). These pins indicate the USB speed of each attached downstream device.

Each dual color LED provides two separate colors (commonly Green and Red). If each of these separate colors are pulsed on and off at a rapid rate, a user will see a third color (in this example, Orange). Using this method, 4 different "color" states are possible (Green, Red, Orange, and Off).

FIGURE 6-1: DUAL COLOR LED IMPLEMENTATION EXAMPLE

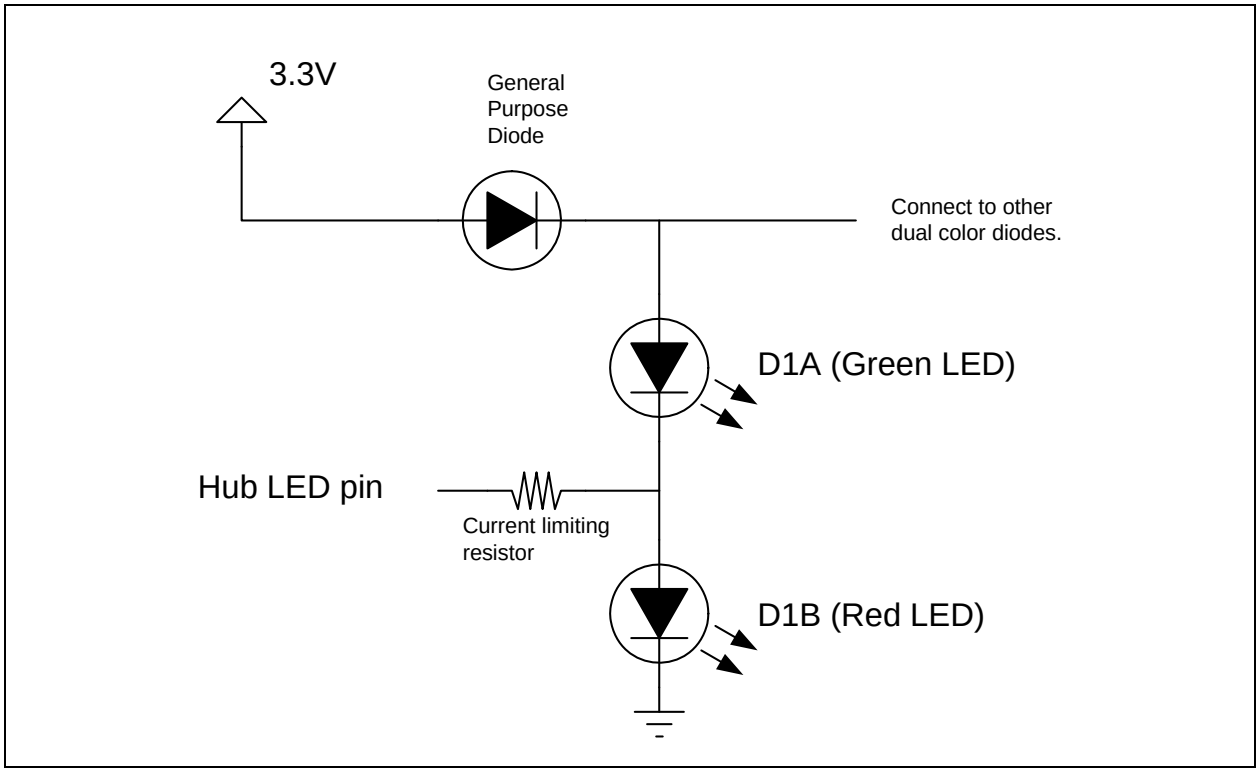


Figure 6-1 shows a simple example of how this LED circuit will be implemented. The circuit should be replicated for each of the 7 LED pins on the HUB. In this circuit, when the LED pin is driven to a logic low state, the Green LED will light up. When the LED pin is driven to a Logic High state the Red LED will light up. When a 1 KHz square wave is driven out on the LED pin, the Green and Red LED's will both alternately light up giving the effect of the color Orange. When nothing is driven out on the LED pin (i.e. the pin floats to a "tri-state" condition), neither the Green nor Red LED will light up, this is the "Off" state.

The assignment is as follows:

- LED_A1_N = LED D1 (Downstream Port 1)
- LED_A2_N = LED D2 (Downstream Port 2)
- LED_A3_N = LED D3 (Downstream Port 3)
- LED_A4_N = LED D4 (Downstream Port 4)
- LED_A5_N = LED D5 (Downstream Port 5)
- LED_A6_N = LED D6 (Downstream Port 6)
- LED_A7_N = LED D7 (Downstream Port 7)

The usage is as follows:

- LED_Ax_N Driven to Logic Low = LS device attached (Green LED)
- LED_Ax_N Driven to Logic High = FS device attached (Red LED)
- LED_Ax_N Pulsed @ 1 KHz= HS device attached (Orange color by pulsing Red & Green).
- LED_Ax_N is tri-state= No devices are attached, or the hub is in suspend, LED's are off.

7.0 CONFIGURATION OPTIONS

7.1 7-Port Hub

The USB 2.0 7-Port Hub is fully compliant to the Universal Serial Bus Specification Revision 2.0 from April 27, 2000 (12/7/2000 and 5/28/2002 Errata). Please reference Chapter 11 (Hub Specification) for general details regarding Hub operation and functionality.

For performance reasons, the 7-Port Hub provides 1 Transaction Translator (TT) per port (defined as Multi-TT configuration), divided into 4 non-periodic buffers per TT.

7.1.1 HUB CONFIGURATION OPTIONS

The MCHP Hub supports a large number of features (some are mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. There are three principal ways to configure the Hub: SMBus, EEPROM, or by internal default settings (with or without pin strapping option overrides). In all cases, the configuration method will be determined by the CFG_SEL2, CFG_SEL1 and CFG_SEL0 pins immediately after RESET_N negation.

7.1.1.1 Power Switching Polarity

Note:	The hub will support active high power controllers only!

7.1.2 VBUS DETECT

According to Section 7.2.1 of the USB 2.0 Specification, a downstream port can never provide power to its D+ or D- pull up resistors unless the upstream port's VBUS is in the asserted (powered) state. The VBUS_DET pin on the Hub monitors the state of the upstream VBUS signal and will not pull up the D+ resistor if VBUS is not active. If VBUS goes from an active to an inactive state (not powered), the Hub will remove power from the D+ pull up resistor within 10 seconds.

7.2 EEPROM Interface

The MCHP Hub can be configured via a 2-wire (I^2C) EEPROM (256x8). (Please see Table 5-2, "USB2517I SMBUS or EEPROM Interface Behavior" for specific details on how to enable configuration via an I^2C EEPROM).

The internal state machine will (when configured for EEPROM support) read the external EEPROM for configuration data. The Hub will then "attach" to the upstream USB host.

Note:	The Hub does not have the capacity to write, or "Program," an external EEPROM. The Hub only has the capability to read external EEPROMs. The external EEPROM will be read (even if it is blank or non-populated), and the Hub will be "configured" with the values that are read.

Please see Internal Register Set (Common to EEPROM and SMBus) for a list of data fields available.

7.2.1 INTERNAL REGISTER SET (COMMON TO EEPROM AND SMBUS)

TABLE 7-1: INTERNAL DEFAULT, EEPROM AND SMBUS REGISTER MEMORY MAP

Reg Addr	R/W	Register Name	Abbr	Internal Default ROM	SMBus and EEPROM POR Values
00h	R/W	VID LSB	VIDL	24h	0x00
01h	R/W	VID MSB	VIDM	04h	0x00
02h	R/W	PID LSB	PIDL	17h	0x00
03h	R/W	PID MSB	PIDM	25h	0x00
04h	R/W	DID LSB	DIDL	00h	0x00
05h	R/W	DID MSB	DIDM	00h	0x00

TABLE 7-1: INTERNAL DEFAULT, EEPROM AND SMBUS REGISTER MEMORY MAP

Reg Addr	R/W	Register Name	Abbr	Internal Default ROM	SMBus and EEPROM POR Values
06h	R/W	Config Data Byte 1	CFG1	9Bh	0x00
07h	R/W	Config Data Byte 2	CFG2	20h	0x00
08h	R/W	Config Data Byte 3	CFG3	00h	0x00
09h	R/W	Non-Removable Devices	NRD	00h	0x00
0Ah	R/W	Port Disable (Self)	PDS	00h	0x00
0Bh	R/W	Port Disable (Bus)	PDB	00h	0x00
0Ch	R/W	Max Power (Self)	MAXPS	01h	0x00
0Dh	R/W	Max Power (Bus)	MAXPB	32h	0x00
0Eh	R/W	Hub Controller Max Current (Self)	HCMCS	01h	0x00
0Fh	R/W	Hub Controller Max Current (Bus)	HCMCB	32h	0x00
10h	R/W	Power-on Time	PWRT	32h	0x00
11h	R/W	LANG_ID_H	LANGIDH	00h	0x00
12h	R/W	LANG_ID_L	LANGIDL	00h	0x00
13h	R/W	MFR_STR_LEN	MFRSL	00h	0x00
14h	R/W	PRD_STR_LEN	PRDSL	00h	0x00
15h	R/W	SER_STR_LEN	SERSL	00h	0x00
16h-53h	R/W	MFR_STR	MANSTR	00h	0x00
54h-91h	R/W	PROD_STR	PRDSTR	00h	0x00
92h-Cfh	R/W	SER_STR	SERSTR	00h	0x00
D0h-F5h	R/W	Reserved	N/A	00h	0x00
F6h	R/W	Boost_Up	BOOSTUP	00h	0x00
F7h	R/W	Boost_7:5	BOOST75	00h	0x00
F8h	R/W	Boost_4:0	BOOST40	00h	0x00
F9h	R/W	Reserved	N/A	00h	0x00
FAh	R/W	Port Swap	PRTSP	00h	0x00
FBh	R/W	Port Remap 12	PRTR12	00h	0x00
FCh	R/W	Port Remap 34	PRTR34	00h	0x00
FDh	R/W	Port Remap 56	PRTR56	00h	0x00

TABLE 7-1: INTERNAL DEFAULT, EEPROM AND SMBUS REGISTER MEMORY MAP

Reg Addr	R/W	Register Name	Abbr	Internal Default ROM	SMBus and EEPROM POR Values
FEh	R/W	Port Remap 7	PRTR7	00h	0x00
FFh	R/W	Status/Command **Note:** SMBus register only	STCD	00h	0x00

7.2.1.1 Register 00h: Vendor ID (LSB)

Bit Number	Bit Name	Description
7:0	VID_LSB	Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the OEM using either the SMBus or EEPROM interface options.

7.2.1.2 Register 01h: Vendor ID (MSB)

Bit Number	Bit Name	Description
7:0	VID_MSB	Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the OEM using either the SMBus or EEPROM interface options.

7.2.1.3 Register 02h: Product ID (LSB)

Bit Number	Bit Name	Description
7:0	PID_LSB	Least Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options.

7.2.1.4 Register 03h: Product ID (MSB)

Bit Number	Bit Name	Description
7:0	PID_MSB	Most Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options.

7.2.1.5 Register 04h: Device ID (LSB)

Bit Number	Bit Name	Description
7:0	DID_LSB	Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options.

7.2.1.6 Register 05h: Device ID (MSB)

Bit Number	Bit Name	Description
7:0	DID_MSB	Most Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options.

7.2.1.7 Register 06h: CONFIG_BYTE_1

Bit Number	Bit Name	Description
7	SELF_BUS_PWR	Self or Bus Power: Selects between Self- and Bus-Powered operation. The Hub is either Self-Powered (draws less than 2mA of upstream bus power) or Bus-Powered (limited to a 100mA maximum of upstream power prior to being configured by the host controller). When configured as a Bus-Powered device, the MCHP Hub consumes less than 100mA of current prior to being configured. After configuration, the Bus-Powered MCHP Hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100mA per externally available downstream port) must consume no more than 500mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 specifications are not violated. When configured as a Self-Powered device, <1mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500mA of current. This field is set by the OEM using either the SMBus or EEPROM interface options. Please see the description under Dynamic Power for the self/bus power functionality when dynamic power switching is enabled. 0 = Bus-Powered operation 1 = Self-Powered operation **Note:** If Dynamic Power Switching is enabled, this bit is ignored and the LOCAL_PWR pin is used to determine if the hub is operating from self or bus power.
6	Reserved	Reserved
5	HS_DISABLE	High Speed Disable: Disables the capability to attach as either a High/Full-speed device, and forces attachment as Full-speed only (i.e. no Hi-Speed support). 0 = High-/Full-Speed 1 = Full-Speed-Only (Hi-Speed disabled!)
4	MTT_ENABLE	Multi-TT enable: Enables one transaction translator per port operation. Selects between a mode where only one transaction translator is available for all ports (Single-TT), or each port gets a dedicated transaction translator (Multi-TT) {Note: The host may force single-TT mode only}. 0 = single TT for all ports 1 = one TT per port (multiple TT's supported)
3	EOP_DISABLE	EOP Disable: Disables EOP generation of EOF1 when in Full-Speed mode. During FS operation only, this permits the Hub to send EOP if no downstream traffic is detected at EOF1. See Section 11.3.1 of the USB 2.0 Specification for additional details. Note: generation of an EOP at the EOF1 point may prevent a Host controller (operating in FS mode) from placing the USB bus in suspend. 0 = EOP generation is normal 1 = EOP generation is disabled

Bit Number	Bit Name	Description
2:1	CURRENT_SNS	Over-current Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs). The ability to support current sensing on a port or ganged basis is hardware implementation dependent. 00 = Ganged sensing (all ports together) 01 = Individual port-by-port 1x = Over-current sensing not supported (must only be used with Bus-Powered configurations!)
0	PORT_PWR	Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port- by-port basis (individual). The ability to support power enabling on a port or ganged basis is hardware implementation dependent. 0 = Ganged switching (all ports together) 1 = Individual port-by-port switching

7.2.1.8 Register 07h: Configuration Data Byte 2

Bit Number	Bit Name	Description
7	DYNAMIC	Dynamic Power Enable: Controls the ability of the Hub to automatically change from Self-Powered operation to Bus-Powered operation if the local power source is removed or is unavailable (and from Bus-Powered to Self-Powered if the local power source is restored). {Note: If the local power source is available, the Hub will always switch to Self-Powered operation.} When Dynamic Power switching is enabled, the Hub detects the availability of a local power source by monitoring the external LOCAL_PWR pin. If the Hub detects a change in power source availability, the Hub immediately disconnects and removes power from all downstream devices and disconnects the upstream port. The Hub will then re-attach to the upstream port as either a Bus-Powered Hub (if local-power is unavailable) or a Self-Powered Hub (if local power is available). 0 = No Dynamic auto-switching 1 = Dynamic Auto-switching capable
6	Reserved	Reserved
5:4	OC_TIMER	Over-Current Timer: Over-Current Timer delay. 00 = 0.1ms 01 = 4ms 10 = 8ms 11 = 16ms

Bit Number	Bit Name	Description
3	COMPOUND	Compound Device: Allows the OEM to indicate that the Hub is part of a compound (see the USB Specification for definition) device. The applicable port(s) must also be defined as having a "Non-Removable Device". **Note:** When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. 0 = No 1 = Yes, Hub is part of a compound device
2:0	Reserved	Reserved

7.2.1.9 Register 08h: Configuration Data Byte 3

Bit Number	Bit Name	Description
7:4	Reserved	Reserved
3	PRTMAP_EN	Port Re-mapping enable: Selects the method used by the hub to assign port numbers and disable ports. ‘0’ = Standard Mode ‘1’ = Port Re-map mode
2:1	LED_MODE	LED Mode Selection: The LED_A[47:1]_N and LED_B[47:1]_N pins support several different modes of operation. ‘00’ = USB Mode ‘01’ = Speed Indication Mode ‘10’ = Same as ‘00’, USB Mode ‘11’ = Same as ‘00’, USB Mode Warning: Do not enable an LED mode that requires LED pins that are not available in the specific package being used in the implementation! **Note:** The Hub will only report that it supports LED's to the host when USB mode is selected. All other modes will be reported as No LED Support.
0	STRING_EN	Enables String Descriptor Support ‘0’ = String Support Disabled ‘1’ = String Support Enabled

7.2.1.10 Register 09h: Non-Removable Device

Bit Number	Bit Name	Description
7:0	NR_DEVICE	Non-Removable Device: Indicates which port(s) include non-removable devices. ‘0’ = port is removable, ‘1’ = port is non-removable. Informs the Host if one of the active ports has a permanent device that is undetachable from the Hub. (Note: The device must provide its own descriptor data.) When using the internal default option, the NON_REM[1:0] pins will designate the appropriate ports as being non- removable. Bit 7= 1; Port 7 non-removable Bit 6= 1; Port 6 non-removable Bit 5= 1; Port 5 non-removable Bit 4= 1; Port 4 non-removable Bit 3= 1; Port 3 non-removable Bit 2= 1; Port 2 non-removable Bit 1= 1; Port 1 non-removable Bit 0 is Reserved, always = ‘0’

7.2.1.11 Register 0Ah: Port Disable For Self Powered Operation

Bit Number	Bit Name	Description
7:0	PORT_DIS_SP	Port Disable Self-Powered: Disables 1 or more contiguous ports. ‘0’ = port is available, ‘1’ = port is disabled. During Self-Powered operation when remapping mode is disabled (PRTMAP_EN='0'), this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a Host Controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB Host, and will reorder the active ports in order to ensure proper function. Bit 7= 1; Port 7 is disabled Bit 6= 1; Port 6 is disabled Bit 5= 1; Port 5 is disabled Bit 4= 1; Port 4 is disabled Bit 3= 1; Port 3 is disabled Bit 2= 1; Port 2 is disabled Bit 1= 1; Port 1 is disabled Bit 0 is Reserved, always = ‘0’

7.2.1.12 Register 0Bh: Port Disable For Bus Powered Operation

Bit Number	Bit Name	Description
7:0	PORT_DIS_BP	Port Disable Bus-Powered: Disables 1 or more contiguous ports. '0' = port is available, '1' = port is disabled. During Self-Powered operation when remapping mode is disabled (PRT-MAP_EN='0'), this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a Host Controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB Host, and will reorder the active ports in order to ensure proper function. When using the internal default option, the PRT_DIS_P[7:1] and PRT_DIS_M[7:1] pins will disable the appropriate ports. Bit 7= 1; Port 7 is disabled Bit 6= 1; Port 6 is disabled Bit 5= 1; Port 5 is disabled Bit 4= 1; Port 4 is disabled Bit 3= 1; Port 3 is disabled Bit 2= 1; Port 2 is disabled Bit 1= 1; Port 1 is disabled Bit 0 is Reserved, always = '0'

7.2.1.13 Register 0Ch: Max Power For Self Powered Operation

Bit Number	Bit Name	Description
7:0	MAX_PWR_SP	Max Power Self_Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0mA in its descriptors. **Note:** The USB 2.0 Specification does not permit this value to exceed 100mA.

7.2.1.14 Register 0Dh: Max Power For Bus Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	MAX_PWR_BP	Max Power Bus_Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0mA in its descriptors.

7.2.1.15 Register 0Eh: Hub Controller Max Current For Self Powered Operation

Bit Number	Bit Name	Description
7:0	HC_MAX_C_SP	Hub Controller Max Current Self-Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. **Note:** The USB 2.0 Specification does not permit this value to exceed 100mA. A value of 50 (decimal) indicates 100mA, which is the default value.

7.2.1.16 Register 0Fh: Hub Controller Max Current For Bus Powered Operation

Bit Number	Bit Name	Description
7:0	HC_MAX_C_BP	Hub Controller Max Current Bus-Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value will include the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value will NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. A value of 50 (decimal) would indicate 100mA, which is the default value.

7.2.1.17 Register 10h: Power-On Time

Bit Number	Bit Name	Description
7:0	POWER_ON_TIME	Power On Time: The length of time that it takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is stable on that port.

7.2.1.18 Register 11h: Language ID High

Bit Number	Bit Name	Description
7:0	LANG_ID_H	USB LANGUAGE ID (Upper 8 bits of a 16 bit ID field)

7.2.1.19 Register 12h: Language ID Low

Bit Number	Bit Name	Description
7:0	LANG_ID_L	USB LANGUAGE ID (Lower 8 bits of a 16 bit ID field)

7.2.1.20 Register 13h: Manufacturer String Length

Bit Number	Bit Name	Description
7:0	MFR_STR_LEN	Manufacturer String Length Maximum string length is 31 characters

7.2.1.21 Register 14h: Product String Length

Bit Number	Bit Name	Description
7:0	PRD_STR_LEN	Product String Length Maximum string length is 31 characters

7.2.1.22 Register 15h: Serial String Length

Bit Number	Bit Name	Description
7:0	SER_STR_LEN	Serial String Length Maximum string length is 31 characters

7.2.1.23 Register 16h-53h: Manufacturer String

Bit Number	Bit Name	Description
7:0	MFR_STR	Manufacturer String, UNICODE UTF-16LE per USB 2.0 Specification Maximum string length is 31 characters (62 bytes) **Note:** The string consists of individual 16 Bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Some EEPROM programmers may transpose the MSB and LSB, thus reversing the Byte order. Please pay careful attention to the byte ordering or your selected programming tools.

7.2.1.24 Register 54h-91h: Product String

Bit Number	Bit Name	Description
7:0	PRD_STR	Product String, UNICODE UTF-16LE per USB 2.0 Specification Maximum string length is 31 characters (62 bytes) **Note:** The string consists of individual 16 Bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Some EEPROM programmers may transpose the MSB and LSB, thus reversing the Byte order. Please pay careful attention to the byte ordering or your selected programming tools.

7.2.1.25 Register 92h-CFh: Serial String

Bit Number	Bit Name	Description
7:0	SER_STR	Serial String, UNICODE UTF16LE per USB 2.0 Specification Maximum string length is 31 characters (62 bytes) **Note:** The string consists of individual 16 Bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Some EEPROM programmers may transpose the MSB and LSB, thus reversing the Byte order. Please pay careful attention to the byte ordering or your selected programming tools.

7.2.1.26 Register F6h: Boost_Up

Bit Number	Bit Name	Description
7:2	Reserved	Reserved
1:0	BOOST_IOUT	USB electrical signaling drive strength Boost Bit for Upstream Port. ‘00’ = Normal electrical drive strength = No boost ‘01’ = Elevated electrical drive strength = Low (approximately 4% boost) ‘10’ = Elevated electrical drive strength = Medium (approximately 8% boost) ‘11’ = Elevated electrical drive strength = High (approximately 12% boost) **Note:** “Boost” could result in non-USB Compliant parameters (one example would be Test J/K levels), the OEM should use a ‘00’ value unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.

7.2.1.27 Register F7h: Boost_7:5 (Reset = 0x00)

Bit Number	Bit Name	Description
7:6	Reserved	Reserved
5:4	BOOST_IOUT_7	USB electrical signaling drive strength Boost Bit for Downstream Port ‘7’. ‘00’ = Normal electrical drive strength ‘01’ = Elevated electrical drive strength (+4% boost) ‘10’ = Elevated electrical drive strength (+8% boost) ‘11’ = Elevated electrical drive strength (+12% boost)
3:2	BOOST_IOUT_6	USB electrical signaling drive strength Boost Bit for Downstream Port ‘6’. ‘00’ = Normal electrical drive strength ‘01’ = Elevated electrical drive strength (+4% boost) ‘10’ = Elevated electrical drive strength (+8% boost) ‘11’ = Elevated electrical drive strength (+12% boost)
1:0	BOOST_IOUT_5	USB electrical signaling drive strength Boost Bit for Downstream Port ‘5’. ‘00’ = Normal electrical drive strength ‘01’ = Elevated electrical drive strength (+4% boost) ‘10’ = Elevated electrical drive strength (+8% boost) ‘11’ = Elevated electrical drive strength (+12% boost)

7.2.1.28 Register F8h: Boost_4:0

Bit Number	Bit Name	Description
7:6	BOOST_IOUT_4	USB electrical signaling drive strength Boost Bit for Downstream Port ‘4’. ‘00’ = Normal electrical drive strength = No boost ‘01’ = Elevated electrical drive strength = Low (approximately 4% boost) ‘10’ = Elevated electrical drive strength = Medium (approximately 8% boost) ‘11’ = Elevated electrical drive strength = High (approximately 12% boost) **Note:** “Boost” could result in non-USB Compliant parameters (one example would be Test J/K levels), the OEM should use a ‘00’ value unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.
5:4	BOOST_IOUT_3	USB electrical signaling drive strength Boost Bit for Downstream Port ‘3’. ‘00’ = Normal electrical drive strength = No boost ‘01’ = Elevated electrical drive strength = Low (approximately 4% boost) ‘10’ = Elevated electrical drive strength = Medium (approximately 8% boost) ‘11’ = Elevated electrical drive strength = High (approximately 12% boost) **Note:** “Boost” could result in non-USB Compliant parameters (one example would be Test J/K levels), the OEM should use a ‘00’ value unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.
3:2	BOOST_IOUT_2	USB electrical signaling drive strength Boost Bit for Downstream Port ‘2’. ‘00’ = Normal electrical drive strength = No boost ‘01’ = Elevated electrical drive strength = Low (approximately 4% boost) ‘10’ = Elevated electrical drive strength = Medium (approximately 8% boost) ‘11’ = Elevated electrical drive strength = High (approximately 12% boost) **Note:** “Boost” could result in non-USB Compliant parameters (one example would be Test J/K levels), the OEM should use a ‘00’ value unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.
1:0	BOOST_IOUT_1	USB electrical signaling drive strength Boost Bit for Downstream Port ‘1’. ‘00’ = Normal electrical drive strength = No boost ‘01’ = Elevated electrical drive strength = Low (approximately 4% boost) ‘10’ = Elevated electrical drive strength = Medium (approximately 8% boost) ‘11’ = Elevated electrical drive strength = High (approximately 12% boost) **Note:** “Boost” could result in non-USB Compliant parameters (one example would be Test J/K levels), the OEM should use a ‘00’ value unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.

7.2.1.29 Register FAh: Port Swap

Bit Number	Bit Name	Description
7:0	PRTSP	Port Swap: Swaps the Upstream and Downstream USB DP and DM Pins for ease of board routing to devices and connectors. ‘0’ = USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin. ‘1’ = USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin. Bit 7= ‘1’; Port 7 DP/DM is swapped. Bit 6= ’1’; Port 6 DP/DM is swapped. Bit 5= ’1’; Port 5 DP/DM is swapped. Bit 4= ‘1’; Port 4 DP/DM is swapped. Bit 3= ‘1’; Port 3 DP/DM is swapped. Bit 2= ‘1’; Port 2 DP/DM is swapped. Bit 1= ‘1’; Port 1 DP/DM is swapped. Bit 0= ‘1’; Upstream Port DP/DM is swapped

7.2.1.30 Register FBh: Port Remap 12

<table>
<tr><th>Bit Number</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>7:0</td><td>PRTR12</td><td>
Port remap register for ports 1 & 2
When a hub is enumerated by a USB Host Controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The Host Controller will number the downstream ports of the hub starting with the number '1', up to the number of ports that the hub recognizes.
The host's port number is referred to as "Logical Port Number" and the physical port on the hub is the “Physical Port Number". When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).
Note: The OEM must ensure that Contiguous Logical Port Numbers are used, starting from #1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a Host will communicate with the ports.
TABLE 7-2: PORT REMAP REGISTER FOR PORTS 1 & 2
<table>
<tr><td>Bit [7:4]</td><td>‘0000’</td><td>Physical Port 2 is Disabled</td></tr>
<tr><td></td><td>‘0001’</td><td>Physical Port 2 is mapped to Logical Port 1</td></tr>
<tr><td></td><td>‘0010’</td><td>Physical Port 2 is mapped to Logical Port 2</td></tr>
<tr><td></td><td>‘0011’</td><td>Physical Port 2 is mapped to Logical Port 3</td></tr>
<tr><td></td><td>‘0100’</td><td>Physical Port 2 is mapped to Logical Port 4</td></tr>
<tr><td></td><td>‘0101’</td><td>Physical Port 2 is mapped to Logical Port 5</td></tr>
<tr><td></td><td>‘0110’</td><td>Physical Port 2 is mapped to Logical Port 6</td></tr>
<tr><td></td><td>‘0111’</td><td>Physical Port 2 is mapped to Logical Port 7</td></tr>
<tr><td></td><td>‘1000’ to ‘1111’</td><td>Reserved, will default to ‘0000’ value</td></tr>
<tr><td>Bit [3:0]</td><td>‘0000’</td><td>Physical Port 1 is Disabled</td></tr>
<tr><td></td><td>‘0001’</td><td>Physical Port 1 is mapped to Logical Port 1</td></tr>
<tr><td></td><td>‘0010’</td><td>Physical Port 1 is mapped to Logical Port 2</td></tr>
<tr><td></td><td>‘0011’</td><td>Physical Port 1 is mapped to Logical Port 3</td></tr>
<tr><td></td><td>‘0100’</td><td>Physical Port 1 is mapped to Logical Port 4</td></tr>
<tr><td></td><td>‘0101’</td><td>Physical Port 1 is mapped to Logical Port 5</td></tr>
<tr><td></td><td>‘0110’</td><td>Physical Port 1 is mapped to Logical Port 6</td></tr>
<tr><td></td><td>‘0111’</td><td>Physical Port 1 is mapped to Logical Port 7</td></tr>
<tr><td></td><td>‘1000’ to ‘1111’</td><td>Reserved, will default to ‘0000’ value</td></tr>
</table>
</td></tr>
</table>

7.2.1.31 Register FCh: Port Remap 34

<table>
<tr><th>Bit Number</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>7:0</td><td>PRTR34</td><td>Port remap register for ports 3 & 4

When a hub is enumerated by a USB Host Controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The Host Controller will number the downstream ports of the hub starting with the number '1', up to the number of ports that the hub recognizes.

The host's port number is referred to as "Logical Port Number" and the physical port on the hub is the “Physical Port Number". When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).
Note: The OEM must ensure that Contiguous Logical Port Numbers are used, starting from #1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a Host will communicate with the ports.

TABLE 7-3: PORT REMAP REGISTER FOR PORTS 3 & 4
<table>
<tr><td>Bit [7:4]</td><td>‘0000’</td><td>Physical Port 4 is Disabled</td></tr>
<tr><td></td><td>‘0001’</td><td>Physical Port 4 is mapped to Logical Port 1</td></tr>
<tr><td></td><td>‘0010’</td><td>Physical Port 4 is mapped to Logical Port 2</td></tr>
<tr><td></td><td>‘0011’</td><td>Physical Port 4 is mapped to Logical Port 3</td></tr>
<tr><td></td><td>‘0100’</td><td>Physical Port 4 is mapped to Logical Port 4</td></tr>
<tr><td></td><td>‘0101’</td><td>Physical Port 4 is mapped to Logical Port 5</td></tr>
<tr><td></td><td>‘0110’</td><td>Physical Port 4 is mapped to Logical Port 6</td></tr>
<tr><td></td><td>‘0111’</td><td>Physical Port 4 is mapped to Logical Port 7</td></tr>
<tr><td></td><td>‘01011 000’ to ‘1111’</td><td>Reserved, will default to ‘0000’ value</td></tr>
<tr><td>Bit [3:0]</td><td>‘0000’</td><td>Physical Port 3 is Disabled</td></tr>
<tr><td></td><td>‘0001’</td><td>Physical Port 3 is mapped to Logical Port 1</td></tr>
<tr><td></td><td>‘0010’</td><td>Physical Port 3 is mapped to Logical Port 2</td></tr>
<tr><td></td><td>‘0011’</td><td>Physical Port 3 is mapped to Logical Port 3</td></tr>
<tr><td></td><td>‘0100’</td><td>Physical Port 3 is mapped to Logical Port 4</td></tr>
<tr><td></td><td>‘0101’</td><td>Physical Port 3 is mapped to Logical Port 5</td></tr>
<tr><td></td><td>‘0110’</td><td>Physical Port 3 is mapped to Logical Port 6</td></tr>
<tr><td></td><td>‘0111’</td><td>Physical Port 3 is mapped to Logical Port 7</td></tr>
</table>
</td></tr>
</table>

7.2.1.32 Register FDh: Port Remap 56 (Reset = 0x00)

<table>
<tr><th>Bit Number</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>7:0</td><td>PRTR56</td><td>
Port remap register for ports 5 & 6.
When a hub is enumerated by a USB Host Controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The Host Controller will number the downstream ports of the hub starting with the number '1', up to the number of ports that the hub recognizes.
The host's port number is referred to as "Logical Port Number" and the physical port on the hub is the “Physical Port Number". When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).
Note: The OEM must ensure that Contiguous Logical Port Numbers are used, starting from #1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a Host will communicate with the ports.
TABLE 7-4: PORT REMAP REGISTER FOR PORTS 5 & 6
<table>
<tr><td rowspan="9">Bit [7:4]</td><td>‘0000’</td><td>Physical Port 6 is Disabled</td></tr>
<tr><td>‘0001’</td><td>Physical Port 6 is mapped to Logical Port 1</td></tr>
<tr><td>‘0010’</td><td>Physical Port 6 is mapped to Logical Port 2</td></tr>
<tr><td>‘0011’</td><td>Physical Port 6 is mapped to Logical Port 3</td></tr>
<tr><td>‘0100’</td><td>Physical Port 6 is mapped to Logical Port 4</td></tr>
<tr><td>‘0101’</td><td>Physical Port 6 is mapped to Logical Port 5</td></tr>
<tr><td>‘0110’</td><td>Physical Port 6 is mapped to Logical Port 6</td></tr>
<tr><td>‘0111’</td><td>Physical Port 6 is mapped to Logical Port 7</td></tr>
<tr><td>‘1000’ to ‘1111’</td><td>Reserved, will default to ‘0000’ value</td></tr>
<tr><td rowspan="9">Bit [3:0]</td><td>‘0000’</td><td>Physical Port 3 is Disabled</td></tr>
<tr><td>‘0001’</td><td>Physical Port 5 is mapped to Logical Port 1</td></tr>
<tr><td>‘0010’</td><td>Physical Port 5 is mapped to Logical Port 2</td></tr>
<tr><td>‘0011’</td><td>Physical Port 5 is mapped to Logical Port 3</td></tr>
<tr><td>‘0100’</td><td>Physical Port 5 is mapped to Logical Port 4</td></tr>
<tr><td>‘0101’</td><td>Physical Port 5 is mapped to Logical Port 5</td></tr>
<tr><td>‘0110’</td><td>Physical Port 5 is mapped to Logical Port 6</td></tr>
<tr><td>‘0111’</td><td>Physical Port 5 is mapped to Logical Port 7</td></tr>
<tr><td>‘1000’ to ‘1111’</td><td>Reserved, will default to ‘0000’ value</td></tr>
</table>
</td></tr>
</table>

7.2.1.33 Register FEh: Port Remap 7 (Reset = 0x00)

<table>
<tr><th>Bit Number</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>7:0</td><td>PRTR7</td><td>Port remap register for ports 7.

When a hub is enumerated by a USB Host Controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The Host Controller will number the downstream ports of the hub starting with the number '1', up to the number of ports that the hub recognizes.

The host's port number is referred to as "Logical Port Number" and the physical port on the hub is the “Physical Port Number". When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).
Note: The OEM must ensure that Contiguous Logical Port Numbers are used, starting from #1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a Host will communicate with the ports.

TABLE 7-5: PORT REMAP REGISTER FOR PORT 7
<table>
<tr><td>Bit [7:4]</td><td>‘0000’ to ‘1111’</td><td>Reserved</td></tr>
<tr><td rowspan="9">Bit [3:0]</td><td>‘0000’</td><td>Physical Port 7 is Disabled</td></tr>
<tr><td>‘0001’</td><td>Physical Port 7 is mapped to Logical Port 1</td></tr>
<tr><td>‘0010’</td><td>Physical Port 7 is mapped to Logical Port 2</td></tr>
<tr><td>‘0011’</td><td>Physical Port 7 is mapped to Logical Port 3</td></tr>
<tr><td>‘0100’</td><td>Physical Port 7 is mapped to Logical Port 4</td></tr>
<tr><td>‘0101’</td><td>Physical Port 7 is mapped to Logical Port 5</td></tr>
<tr><td>‘0110’</td><td>Physical Port 7 is mapped to Logical Port 6</td></tr>
<tr><td>‘0111’</td><td>Physical Port 7 is mapped to Logical Port 7</td></tr>
<tr><td>‘1000’ to ‘1111’</td><td>Reserved, will default to ‘0000’ value</td></tr>
</table>
</td></tr>
</table>

7.2.1.34 Register FFh: Status/Command

Bit Number	Bit Name	Description
7:3	Reserved	Reserved
2	INTF_PW_DN	SMBus Interface Power Down '0' = Interface is active '1' = Interface power down after ACK has completed
1	RESET	Reset the SMBus Interface and internal memory back to RESET_N assertion default settings. '0' = Normal Run/Idle State '1' = Force a reset of registers to their default state
0	USB_ATTACH	USB Attach (and write protect) '0' = SMBus slave interface is active '1' = Hub will signal a USB attach event to an upstream device. The internal memory (address range 00h-FEh) is "write-protected" to prevent unintentional data corruption.

7.2.2 I^2C EEPROM

The I^2C EEPROM interface implements a subset of the I^2C Master Specification (Please refer to the Philips Semiconductor Standard I^2C-Bus Specification for details on I^2C bus protocols). The Hub's I^2C EEPROM interface is designed to attach to a single "dedicated" I^2C EEPROM, and conforms to the Standard-mode I^2C Specification (100kbit/s transfer rate and 7-bit addressing) for protocol and electrical compatibility.

Note: Extensions to the I^2C Specification are not supported.

The Hub acts as the master and generates the serial clock SCL, controls the bus access (determines which device acts as the transmitter and which device acts as the receiver), and generates the START and STOP conditions.

7.2.2.1 Implementation Characteristics

The Hub will only access an EEPROM using the Sequential Read Protocol.

7.2.2.2 Pull-Up Resistor

The Circuit board designer is required to place external pull-up resistors (10KΩ recommended) on the SDA/SMBDATA & SCL/SMBCLK/CFG_SELO lines (per SMBus 1.0 Specification, and EEPROM manufacturer guidelines) to Vcc in order to assure proper operation.

7.2.2.3 I^2C EEPROM Slave Address

Slave address is 1010000.

Note: 10-bit addressing is NOT supported.

7.2.3 IN-CIRCUIT EEPROM PROGRAMMING

The EEPROM can be programmed via ATE by pulling RESET_N low (which tri-states the Hub's EEPROM interface and allows an external source to program the EEPROM).

7.3 SMBus Slave Interface

Instead of loading User-Defined Descriptor data from an external EEPROM, the MCHP Hub can be configured to receive a code load from an external processor via an SMBus interface. The SMBus interface shares the same pins as the EEPROM interface; if CFG_SEL1 & CFG_SEL0 activates the SMBus interface, external EEPROM support is no longer available (and the user-defined descriptor data must be downloaded via the SMBus). Due to system issues, the MCHP Hub waits indefinitely for the SMBus code load to complete and only “appears” as a newly connected device on USB after the code load is complete.

The Hub’s SMBus implementation is a subset of the SMBus interface to the host. The device is a *slave-only* SMBus device. The implementation in the device is a subset of SMBus since it only supports two protocols.

The Write Block and Read Block protocols are the only valid SMBus protocols for the Hub. The Hub responds to other protocols as described in Section 7.3.2, "Invalid Protocol Response Behavior," on page 40. Reference the System Management Bus Specification, Rev 1.0.

The SMBus interface is used to read and write the registers in the device. The register set is shown in Section 7.2.1, "Internal Register Set (Common to EEPROM and SMBus)," on page 19.

7.3.1 BUS PROTOCOLS

Typical Write Block and Read Block protocols are shown below. Register accesses are performed using 7-bit slave addressing, an 8-bit register address field, and an 8-bit data field. The shading indicates the Hub driving data on the SMBDATA line; otherwise, host data is on the SDA/SMBDATA line.

The slave address is the unique SMBus Interface Address for the Hub that identifies it on SMBus. The register address field is the internal address of the register to be accessed. The register data field is the data that the host is attempting to write to the register or the contents of the register that the host is attempting to read.

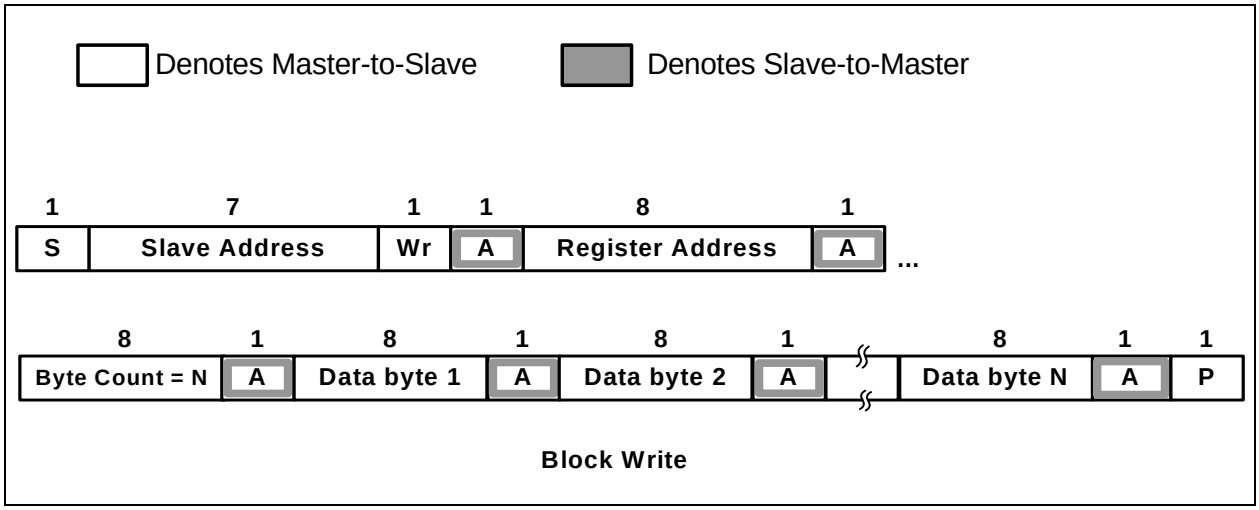
Note:	Data bytes are transferred MSB first (msb first).

7.3.1.1 Block Read/Write

The Block Write begins with a slave address and a write condition. After the command code, the host issues a byte count which describes how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A Block Read or Write is allowed to transfer a maximum of 32 data bytes.

Note: For the following SMBus tables:

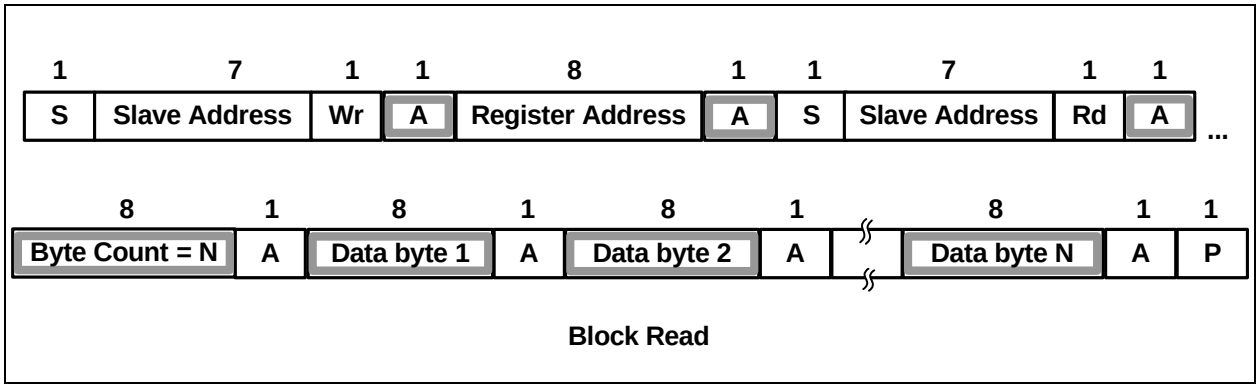
FIGURE 7-1: BLOCK WRITE



Block Read

A Block Read differs from a block write in that the repeated start condition exists to satisfy the I^2C specification's requirement for a change in the transfer direction.

FIGURE 7-2: BLOCK READ



7.3.2 INVALID PROTOCOL RESPONSE BEHAVIOR

Registers accessed with an invalid protocol are not updated. A register is only updated following a valid protocol. The only valid protocols are Write Block and Read Block, which are described above.

The Hub only responds to the hardware selected Slave Address.

Attempting to communicate with the Hub over SMBus with an invalid slave address or invalid protocol results in no response, and the SMBus Slave Interface returns to the idle state.

The only valid registers that are accessible by the SMBus slave address are the registers defined in the Registers Section. See Section 7.3.3 for the response to undefined registers.

7.3.3 GENERAL CALL ADDRESS RESPONSE

The Hub does not respond to a general call address of 0000_000b.

7.3.4 SLAVE DEVICE TIME-OUT

According to the SMBus Specification, V1.0 devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25ms ($T_{TIMEOUT, MIN}$). Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than 35ms ($T_{TIMEOUT, MAX}$).

Note:	Some simple devices do not contain a clock low drive circuit; this simple kind of device typically resets its communications port after a start or stop condition. The Slave Device Time-Out must be implemented.

7.3.5 STRETCHING THE SCLK SIGNAL

The Hub supports stretching of the SCLK by other devices on the SMBus. The Hub does not stretch the SCLK.

7.3.6 SMBUS TIMING

The SMBus Slave Interface complies with the SMBus AC Timing Specification. See the SMBus timing in the “Timing Diagram” section.

7.3.7 BUS RESET SEQUENCE

The SMBus Slave Interface resets and returns to the idle state upon a START field followed immediately by a STOP field.

7.3.8 SMBUS ALERT RESPONSE ADDRESS

The SMBALERT# signal is not supported by the Hub.

7.3.8.1 Undefined Registers

The registers shown in Table 7-1 are the defined registers in the Hub. Reads to undefined registers return to 00h. Writes to undefined registers have no effect and do not return an error.

7.3.8.2 Reserved Registers

Unless otherwise instructed, only a ‘0’ may be written to all reserved registers or bits.

7.4 Default Configuration Option

The MCHP Hub can be configured via its internal default configuration. (Please see Section 7.2.1, "Internal Register Set (Common to EEPROM and SMBus)" for specific details on how to enable default configuration.)

Please refer to Table 7-1 for the internal default values that are loaded when this option is selected.

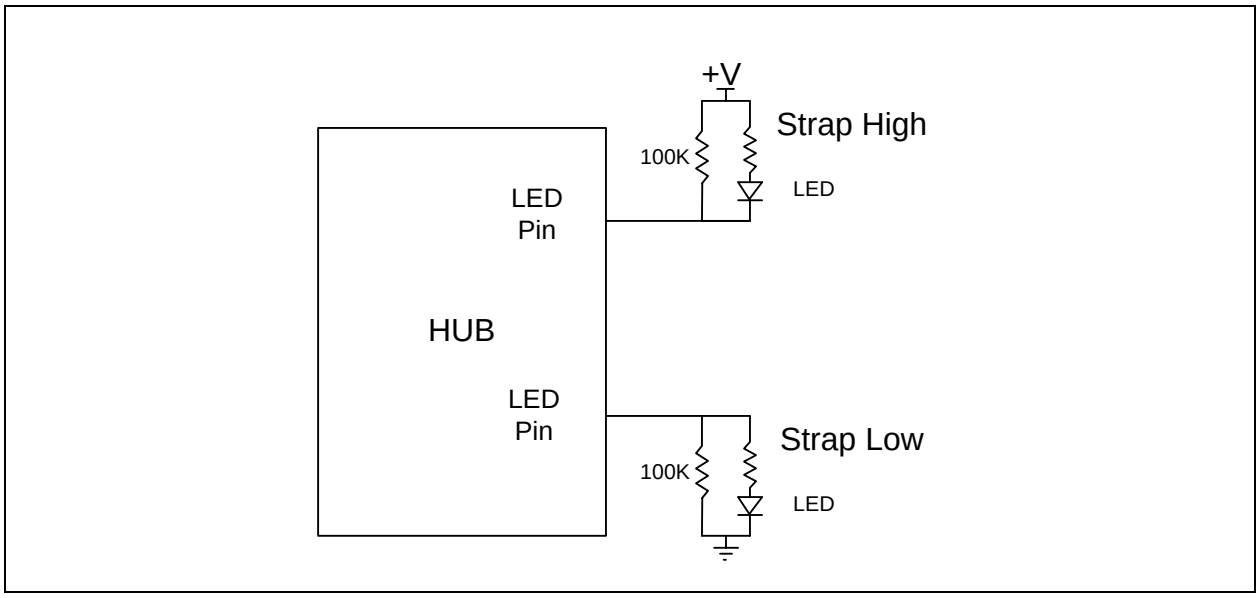
7.5 Default Strapping Options:

The USB2517/USB2517I can be configured via a combination of internal default values and pin strap options. Please see Table 5-1, "USB2517/USB2517I Pin Descriptions" and Table 5-2, "USB2517I SMBUS or EEPROM Interface Behavior" for specific details on how to enable the default/pin-strap configuration option.

The strapping option pins only cover a limited sub-set of the configuration options. The internal default values will be used for the bits & registers that are not controlled by a strapping option pin. Please refer to Table 7-1 for the internal default values that are loaded when this option is selected.

The Amber and Green LED pins are sampled after RESET_N negation, and the logic values are used to configure the hub if the internal default configuration mode is selected. The implementation shown below (see Section 7.6, "Reset") shows a recommended passive scheme. When a pin is configured with a “Strap High” configuration, the LED functions with active low signalling, and the PAD will “sink” the current from the external supply. When a pin is configured with a “Strap Low” configuration, the LED functions with active high signalling, and the PAD will “source” the current to the external LED.

FIGURE 7-3: LED STRAPPING OPTION



7.6 Reset

There are two different resets that the Hub experiences. One is a hardware reset (either from the internal POR reset circuit or via the RESET_N pin) and the second is a USB Bus Reset.

7.6.1 INTERNAL POR HARDWARE RESET

All reset timing parameters are ensured by design.

7.6.2 EXTERNAL HARDWARE RESET_N

A valid hardware reset is defined as assertion of RESET_N for a minimum of 1us after all power supplies are within operating range. While reset is asserted, the Hub (and its associated external circuitry) consumes less than 500μA of current from the upstream USB power source.

Assertion of RESET_N (external pin) causes the following:

1. All downstream ports are disabled, and PRTPWR power to downstream devices is removed.
2. The PHYs are disabled, and the differential pairs will be in a high-impedance state.
3. All transactions immediately terminate; no states are saved.
4. All internal registers return to the default state (in most cases, 00(h)).
5. The external crystal oscillator is halted.
6. The PLL is halted.
7. LED indicators are disabled.

The Hub is “operational” 500μs after RESET_N is negated.

Once operational, the Hub immediately reads OEM-specific data from the external EEPROM (if the SMBus option is not disabled).

7.6.2.1 RESET_N for Strapping Option Configuration

FIGURE 7-4: RESET_N TIMING FOR DEFAULT/STRAP OPTION MODE

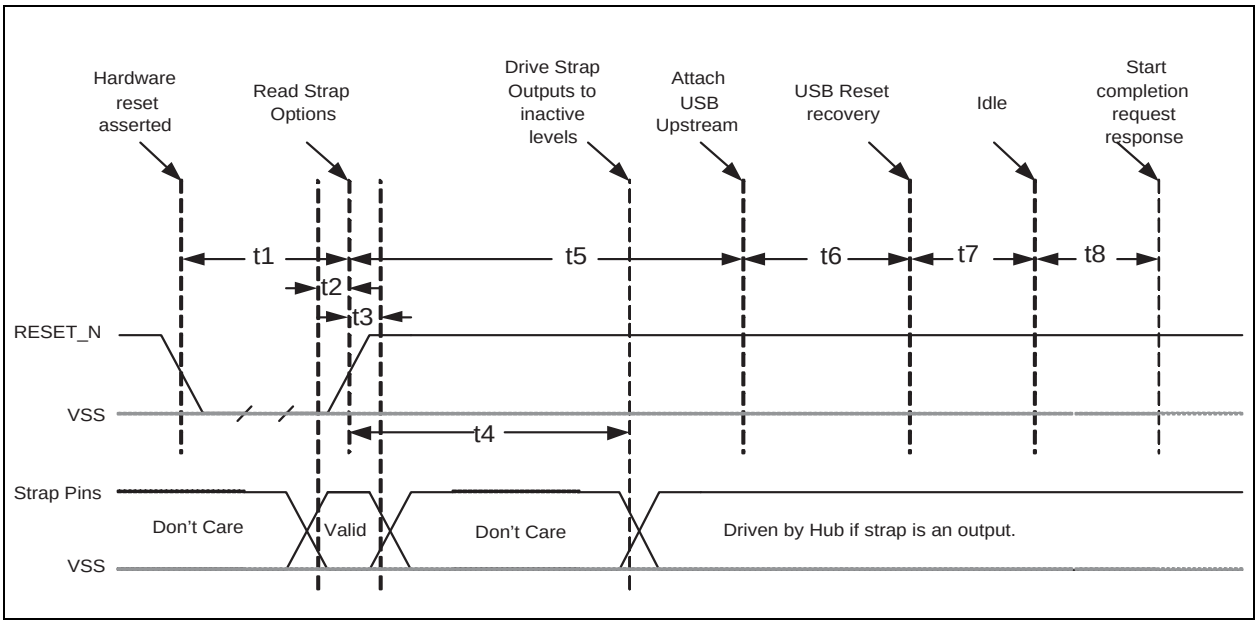


TABLE 7-6: RESET_N TIMING FOR DEFAULT/STRAP OPTION MODE

Name	Description	Min	Typ	Max	Units
t1	RESET_N Asserted.	1			µsec
t2	Strap Setup Time	16.7			nsec
t3	Strap Hold Time.	16.7		1400	nsec
t4	hub outputs driven to inactive logic states		1.5	2	µsec
t5	USB Attach (See Note).			100	msec
t6	Host acknowledges attach and signals USB Reset.	100			msec
t7	USB Idle.		undefined		msec
t8	Completion time for requests (with or without data stage).			5	msec

Note:

- When in Bus-Powered mode, the Hub and its associated circuitry must not consume more than 100mA from the upstream USB power source during t1+t5.
- All Power Supplies must have reached the operating levels mandated in Section 8.0, "DC Parameters", prior to (or coincident with) the assertion of RESET_N.

7.6.2.2 RESET_N for EEPROM Configuration

FIGURE 7-5: RESET_N TIMING FOR EEPROM MODE

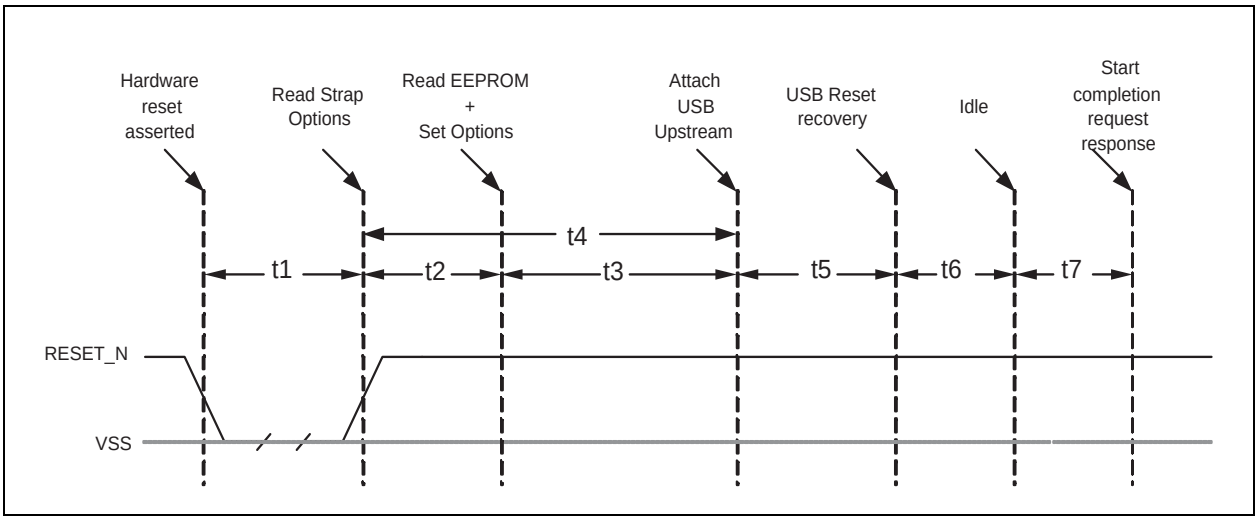


TABLE 7-7: RESET_N TIMING FOR EEPROM MODE

Name	Description	Min	Typ	Max	Units
t1	RESET_N Asserted.	1			µsec
t2	Hub Recovery/Stabilization.			500	µsec
t3	EEPROM Read / Hub Config.		2.0	99.5	msec
t4	USB Attach (See Note).			100	msec
t5	Host acknowledges attach and signals USB Reset.	100			msec
t6	USB Idle.		undefined		msec
t7	Completion time for requests (with or without data stage).			5	msec

Note:

- When in Bus-Powered mode, the Hub and its associated circuitry must not consume more than 100mA from the upstream USB power source during t4+t5+t6+t7.
- All Power Supplies must have reached the operating levels mandated in Section 8.0, "DC Parameters", prior to (or coincident with) the assertion of RESET_N.

7.6.2.3 RESET_N for SMBus Slave Configuration

FIGURE 7-6: RESET_N TIMING FOR SMBUS MODE

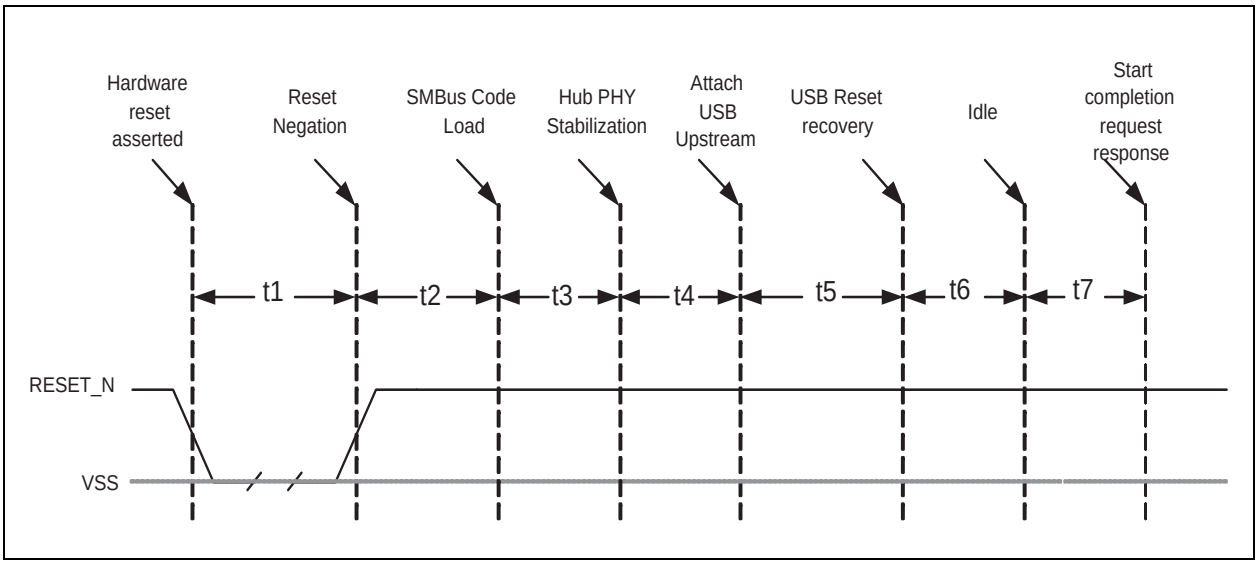


TABLE 7-8: RESET_N TIMING FOR SMBUS MODE

Name	Description	Min	Typ	Max	Units
t1	RESET_N Asserted.	1			µsec
t2	Hub Recovery/Stabilization.			500	µsec
t3	SMBus Code Load (See Note).		250	300	msec
t4	Hub Configuration and USB Attach.			100	msec
t5	Host acknowledges attach and signals USB Reset.	100			msec
t6	USB Idle.		Undefined		msec
t7	Completion time for requests (with or without data stage).			5	msec

Note:

- For Bus-Powered configurations, the 99.5ms (MAX) is required, and the Hub and its associated circuitry must not consume more than 100mA from the upstream USB power source during t2+t3+t4+t5+t6+t7. For Self-Powered configurations, t3 MAX is not applicable and the time to load the configuration is determined by the external SMBus host.
- All Power Supplies must have reached the operating levels mandated in Section 8.0, "DC Parameters", prior to (or coincident with) the assertion of RESET_N.

7.6.3 USB BUS RESET

In response to the upstream port signaling a reset to the Hub, the Hub does the following:

Note:	The Hub does not propagate the upstream USB reset to downstream devices.

1. Sets default address to 0.
2. Sets configuration to: Unconfigured.
    1. Negates PRTPWR[7:1] to all downstream ports.
    2. Clears all TT buffers.
    3. Moves device from suspended to active (if suspended).
    4. Complies with Section 11.10 of the USB 2.0 Specification for behavior after completion of the reset sequence.

The Host then configures the Hub and the Hub's downstream port devices in accordance with the USB Specification.

8.0 DC PARAMETERS

8.1 Maximum Ratings

Parameter	Symbol	Min	Max	Units	Comments
Storage Temperature	T_{STOR}	-55	150	°C	
Lead Temperature			325	°C	Soldering < 10 seconds
1.8V supply voltage	$V_{DDA18PLL}$, V_{DD18}		2.5	V	
3.3V supply voltage	V_{DDA33}, $V_{DD33PLL}$, V_{DD33}, V_{DD33CR}		4.6	V	
Voltage on any I/O pin		-0.5	5.5	V	
Voltage on XTAL1		-0.5	4.0	V	
Voltage on XTAL2		-0.5	3.6	V	
HBM ESD Performance			4	kV	

Note: Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied.

When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

8.2 Operating Conditions

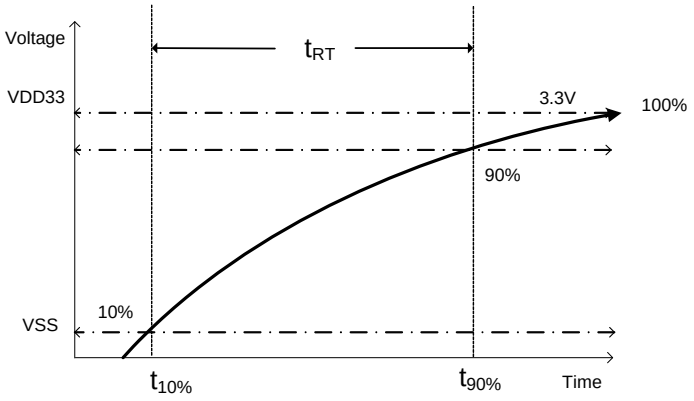
Parameter	Symbol	Min	Max	Units	Comments
Operating Temperature	T_A	Note 8-2	Note 8-3	°C	Ambient temperature in still air.
1.8V supply voltage	$V_{DDA18PLL}$ V_{DD18}	1.62	1.98	V	
3.3V supply voltage	V_{DDA33} $V_{DDA33PLL}$ V_{DD33} V_{DD33CR}	3.0	3.6	V	
3.3V supply rise time	t_{RT}		400	µs	(See Note 8-1and Figure 8-1, "SUPPLY RISE TIME MODEL")
Voltage on any I/O pin		-0.3	5.5	V	If any 3.3V supply voltage drops below 3.0V, then the MAX becomes: (3.3V supply voltage) + 0.5
Voltage on XTAL1		-0.3	V_{DD33}	V	
Voltage on XTAL2		-0.3	V_{DD18}	V	

Note 8-1 If RESET_N is controlled low during the 3.3V rise time and driven high after VDD33 is stable, the rise time can be extended to 100 ms.

Note 8-2 0°C for commercial temperature version, -40°C for industrial temperature version

Note 8-3 70°C for commercial temperature version, +85°C for industrial temperature version

FIGURE 8-1: SUPPLY RISE TIME MODEL



8.3 Package Thermal Specifications

TABLE 8-1: PACKAGE THERMAL PARAMETERS

Symbol	°C/W	Velocity (Meters/s)
Θ_{JA}	27	0
	24	1
Θ_{JB}	15	0
Ψ_{JT}	0.2	0
Θ_{JC}	2.3	0

Note: Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESDN51.

TABLE 8-2: DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Comments
I, IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Input Leakage	I_{IL}	-10		+10	uA	V_{IN} = 0 to V_{DD33}
Hysteresis (‘IS’ Only)	V_{HYSI}	250		350	mV	
Input Buffer with Pull-Up (IPU)						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Low Input Leakage	I_{ILL}	+35		+90	uA	V_{IN} = 0
High Input Leakage	I_{IHL}	-10		+10	uA	V_{IN} = V_{DD33}
Input Buffer with Pull-Down (IPD)						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Low Input Leakage	I_{ILL}	+10		-10	uA	V_{IN} = 0
High Input Leakage	I_{IHL}	-35		-90	uA	V_{IN} = V_{DD33}

TABLE 8-2: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Min	Typ	Max	Units	Comments
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.5	V	
High Input Level	V_{IHCK}	1.4			V	
Input Leakage	I_{IL}	-10		+10	uA	V_{IN} = 0 to V_{DD33}
O12, I/O12 & I/OSD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA @ V_{DD33} = 3.3V
High Output Level	V_{OH}	2.4			V	I_{OH} = -12mA @ V_{DD33} = 3.3V
Output Leakage	I_{OL}	-10		+10	uA	V_{IN} = 0 to V_{DD33} (Note 8-4)
Hysteresis ('I/OSD12' pad only)	V_{HYSC}	250		350	mV	
IO-U (Note 8-5)						
Supply Current Unconfig-ured						
Hi-Speed Host	$I_{CCINTHS}$		95		mA	
Full-Speed Host	$I_{CCINITFS}$		95		mA	
Supply Current Configured (Hi-Speed Host) (Note 8-6)						All supplies combined
1 Port HS, 1 Port LS/FS	I_{HCH1C1}		230		mA	
2 Ports @ LS/FS	I_{HCC2}		230		mA	
2 Ports @ HS	I_{HCH2}		270		mA	
4 Ports @ HS	I_{HCH4}		330		mA	
7 Ports @ HS	I_{HCH7}		420	460	mA	
Supply Current Configured (Full-Speed Host)						All supplies combined
1 Port	I_{FCC1}		205		mA	
2 Ports	I_{FCC2}		210		mA	
3 Ports	I_{FCC3}		215		mA	
4 Ports	I_{FCC4}		220		mA	
7 Ports	I_{FCC7}		235	270	mA	
Supply Current Suspend	I_{CSBY}		360	610	µA	All supplies combined
Supply Current Reset	I_{CRST}		110	400	µA	All supplies combined

Note 8-4 Output leakage is measured with the current pins in high impedance.

Note 8-5 See USB 2.0 Specification for USB DC electrical characteristics.

Note 8-6 Max supply current was measured under ICH10 EHCI controller while transferring files in Windows7 using fastest available HDs, at VDD=3.3V+20% and T (case) temperature -55C.

8.4 CAPACITANCE T_A = 25°C; fc = 1MHz; V_{DD18}, V_{DDPLL} = 1.8*V*

TABLE 8-3: PIN CAPACITANCE

Parameter	Symbol	Limits			Unit	Test Condition
		Min	Typ	Max		
Clock Input Capacitance	C_{XTAL}			2	pF	All pins except USB pins (and pins under test tied to AC ground)
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

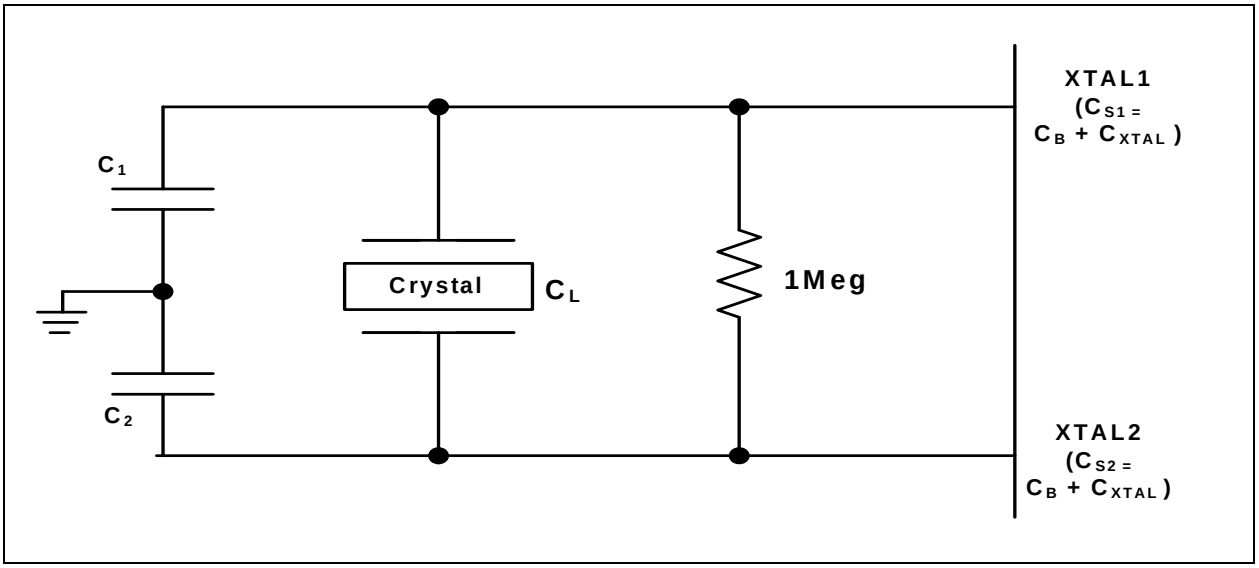
9.0 AC SPECIFICATIONS

9.1 Oscillator/Clock

Crystal: Parallel Resonant, Fundamental Mode, 24 MHz ±350ppm.

External Clock: 50% Duty cycle ± 10%, 24 MHz ± 350ppm

FIGURE 9-1: TYPICAL CRYSTAL CIRCUIT



Note: C_B equals total board/trace capacitance.

FIGURE 9-2: FORMULA TO FIND VALUE OF C_1 AND C_2

$$\frac{(C_1 + C_{S1}) \times (C_2 + C_{S2})}{(C_1 + C_{S1} + C_2 + C_{S2})} = C_L$$

9.1.1 SMBUS INTERFACE

The MCHP Hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the SMBus 1.0 Specification for Slave-Only devices (except as noted in Section 7.3, "SMBus Slave Interface").

9.1.2 I^2C EEPROM

Frequency is fixed at 58.6KHz ± 20%.

9.1.3 USB 2.0

The MCHP Hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the USB 2.0 Specification. Please refer to the USB 2.0 Specification for more information.

10.0 PACKAGE OUTLINE

FIGURE 10-1: 64-PIN QFN, 9X9MM BODY, 0.5MM PITCH

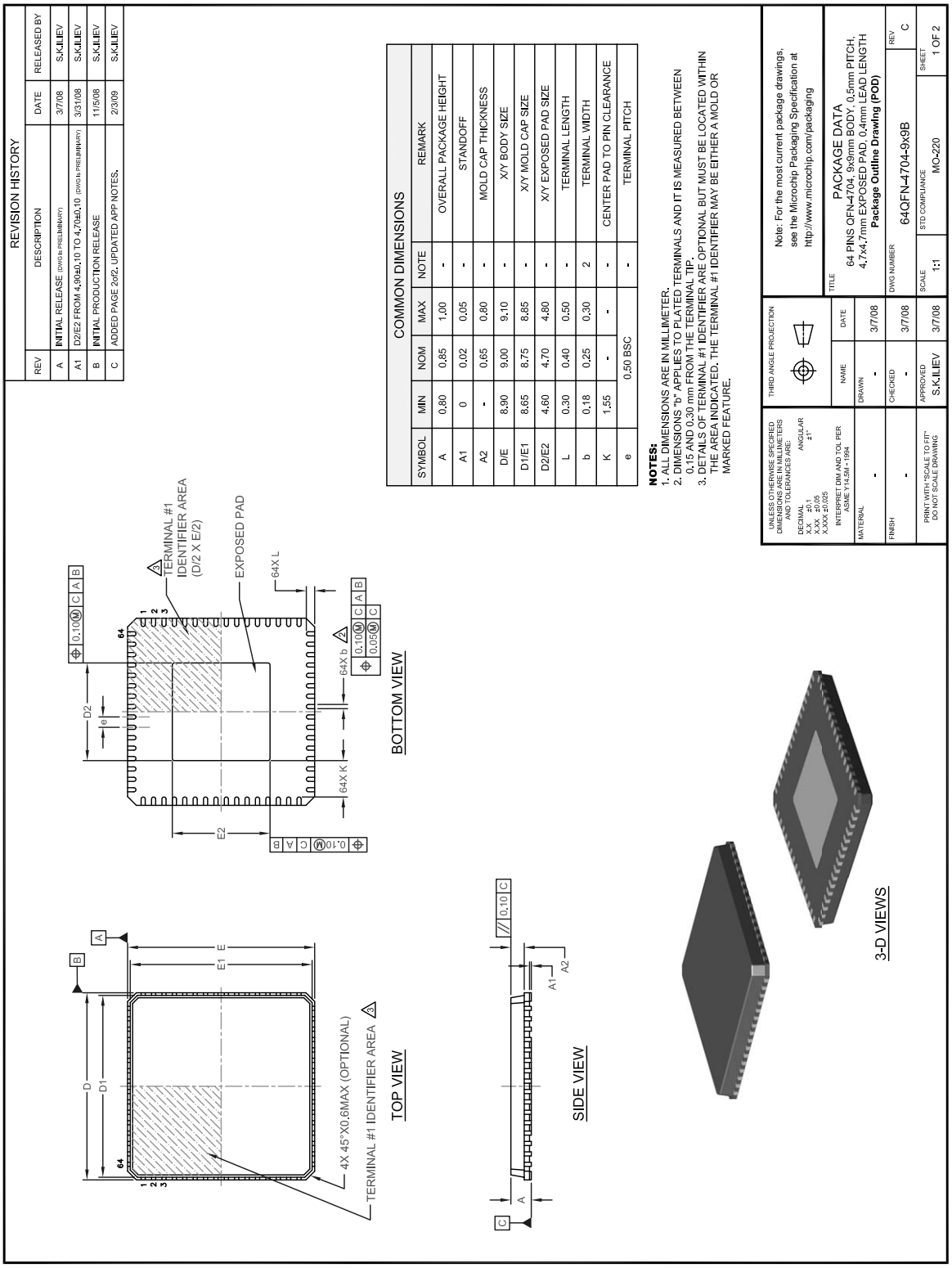
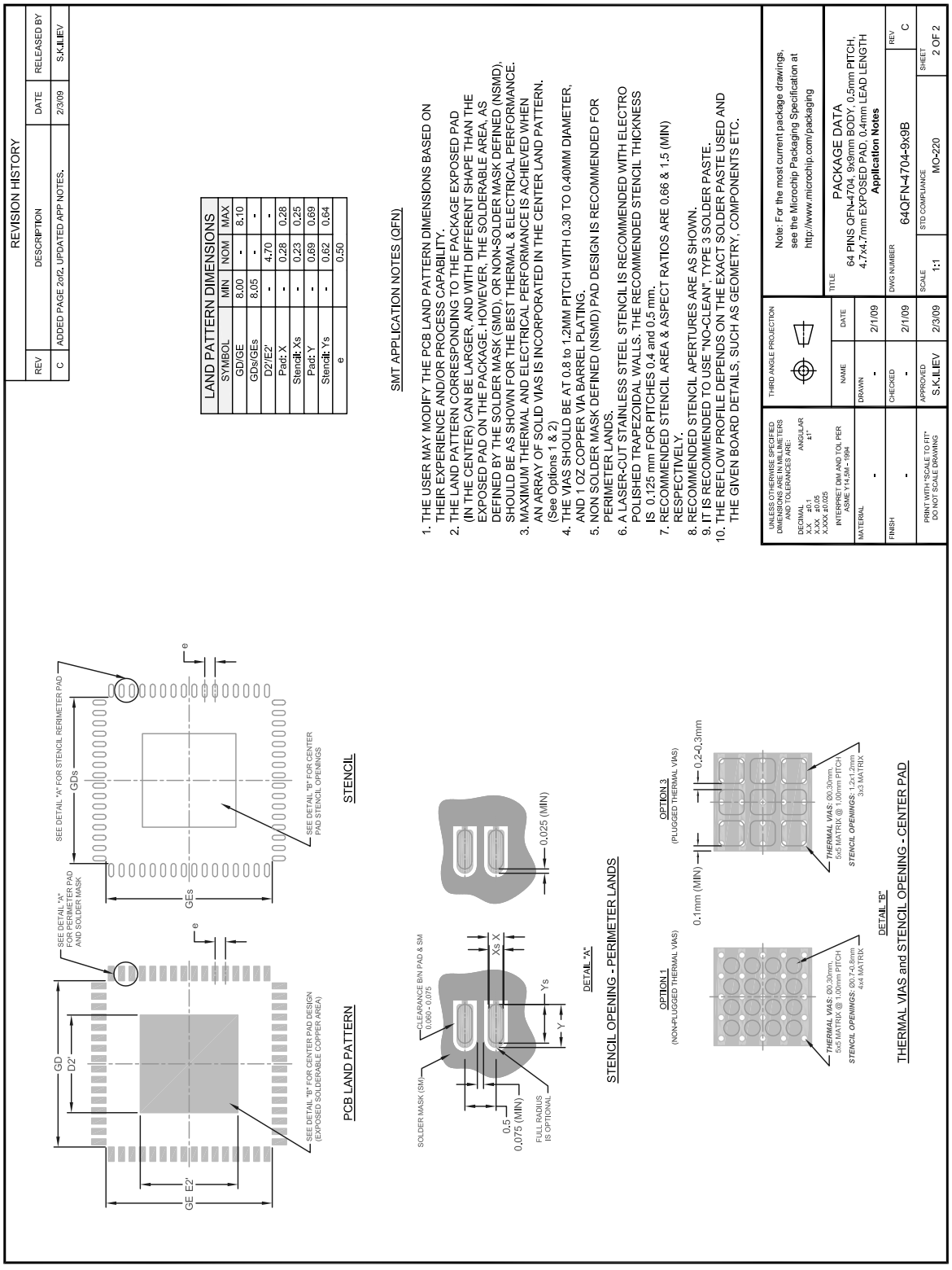


FIGURE 10-1: 64-PIN QFN, 9X9MM BODY, 0.5MM PITCH (CONTINUED)



APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
DS00001598C (04-13-18)	Section 8.1, "Maximum Ratings"	Added row: “HBM ESD Performance.
	Section 8.3, "Package Thermal Specifications"	Added section.
DS00001598B (05-23-16)	Table 5-1, "USB2517/USB2517I Pin Descriptions"	Corrected the USBDN[7:1]_DP/PRT_DIS_P[7:1] & USBDN[7:1]_DM/PRT_DIS_M[7:1] pin number assignments to correctly reflect the 7:1 ordering and clarified the description.
USB2517/USB2517I Rev A, replaces the previous SMSC version, Rev 2.9		

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PART NO.	[X]	-	XXX	-	[X](1)
Device	Temperature Range		Package		Tape and Reel Option

Device:	USB2517	
Temperature Range:	Blank = 0°C to +70°C I = -40°C to +85°C	(Commercial) (Industrial)
Package:	JZX = 64-pin QFN	
Tape and Reel Option:	Blank = Standard packaging (tray) TR = Tape and Reel(1)	

Examples:

a) USB2517I - JZX-TR
Industrial temperature,
64-pin QFN
Tape & Reel

b) USB2517-JXZX
Commercial temperature,
64-pin QFN
Tray

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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