

## 1. General description

AC Thyristor power switch in a SOT54 plastic package with self-protective capabilities against low and high energy transients

## 2. Features and benefits

- Exclusive negative gate triggering
- Full cycle AC conduction
- High noise immunity
- Remote gate separates the gate driver from the effects of the load current
- Very sensitive gate for lowest gate trigger current
- Safe clamping of low energy over-voltage transients
- Self-protective turn-on during high energy voltage transients

## 3. Applications

- Fan motor circuits
- Pump motor circuits
- Lower-power highly inductive, resistive and safety loads

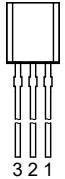
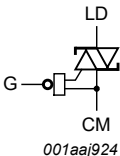
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 71\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	0.8	A
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 100\text{ mA}$ ; LD+ G-; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 6</a>	0.5	-	5	mA
		$V_D = 12\text{ V}$ ; $I_T = 100\text{ mA}$ ; LD- G-; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 6</a>	0.5	-	5	mA

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	 <p>TO-92 (SOT54)</p>	 <p>001aa924</p>
2	G	gate		
3	LD	load		

## 6. Ordering information

Table 3. Ordering information

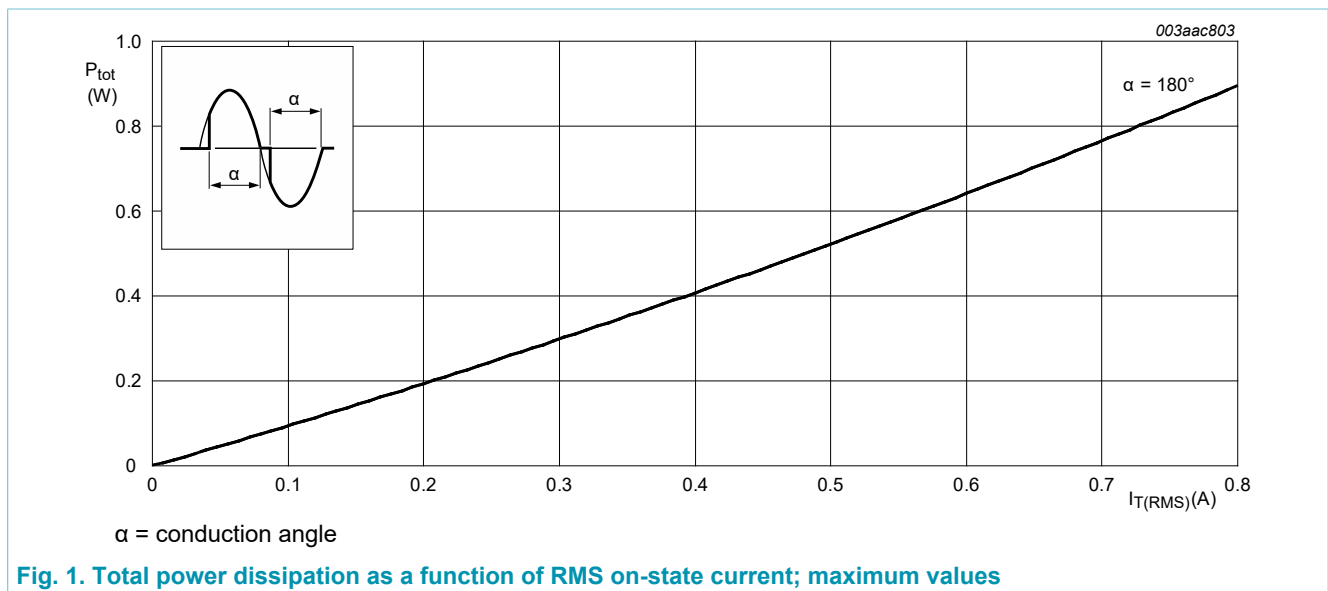
Type number	Package		
	Name	Description	Version
ACT108-600D	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54
ACT108-600D/DG	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 71\text{ °C}$ ; <a href="#">Fig. 1</a>	-	0.8	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 16.7\text{ ms}$	-	8.8	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	8	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; SIN	-	0.32	A <sup>2</sup> s
$di_T/dt$	rate of rise of on-state current	$I_G = 10\text{ mA}$	-	50	A/ $\mu$ s
$I_{GM}$	peak gate current	$t = 20\text{ }\mu$ s	-	1	A
$V_{GM}$	peak gate voltage		-	15	V
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
$T_{stg}$	storage temperature		-40	150	°C
$T_j$	junction temperature		-	125	°C
$V_{PP}$	peak pulse voltage	$T_j = 25\text{ °C}$ ; non-repetitive, off-state; <a href="#">Fig. 4</a>	-	2	kV



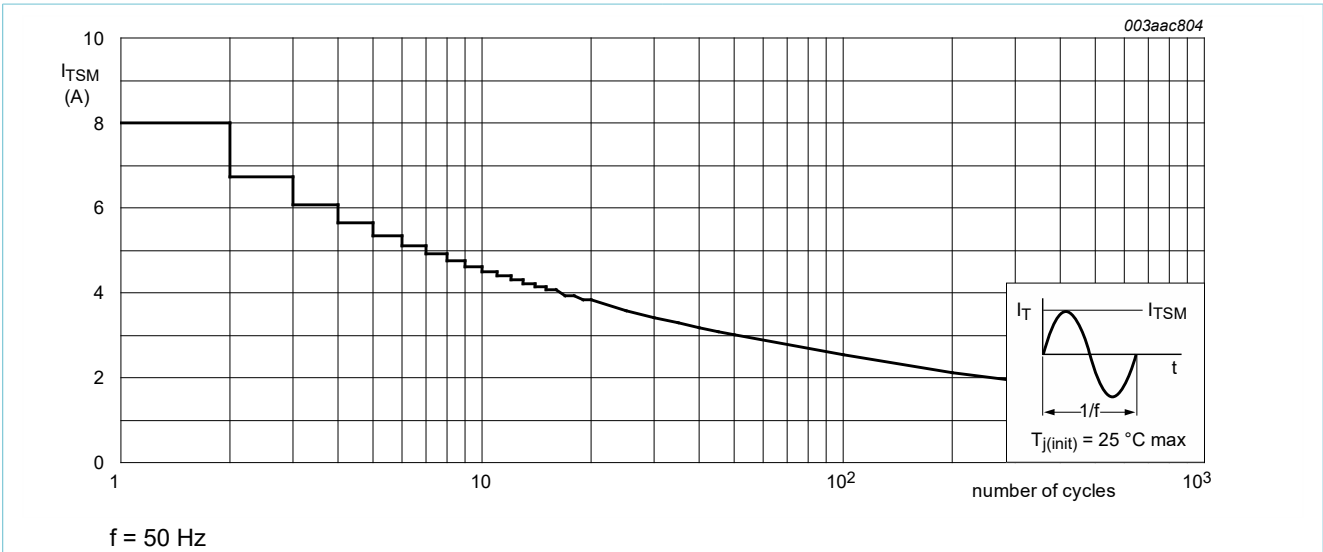


Fig. 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

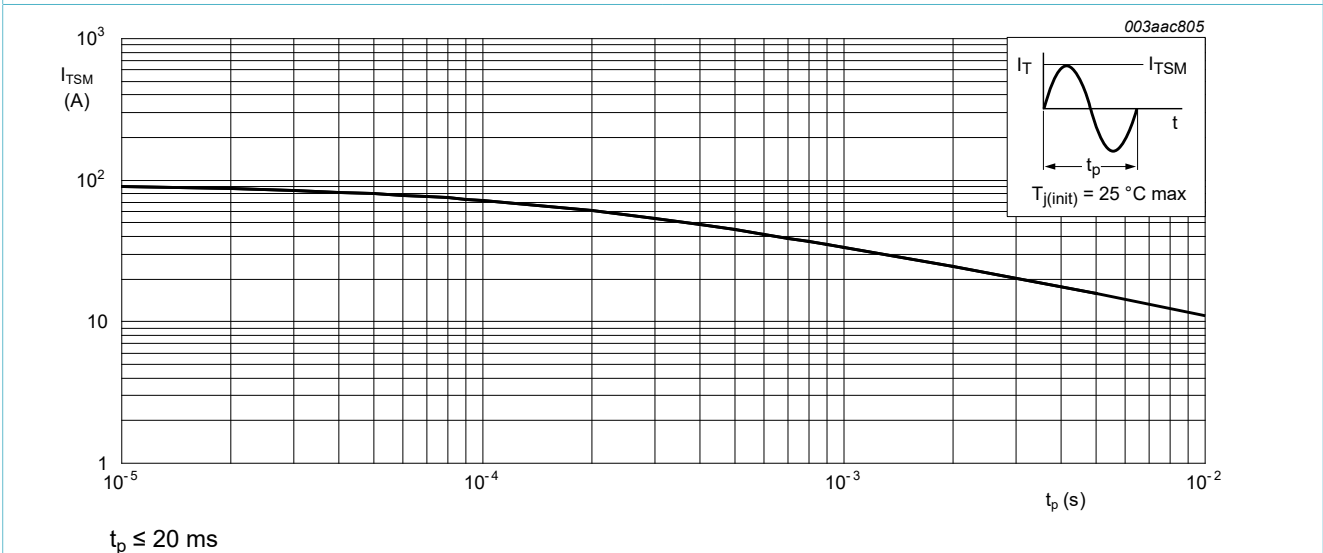


Fig. 3. Non-repetitive peak on-state current as a function of pulse width; maximum values

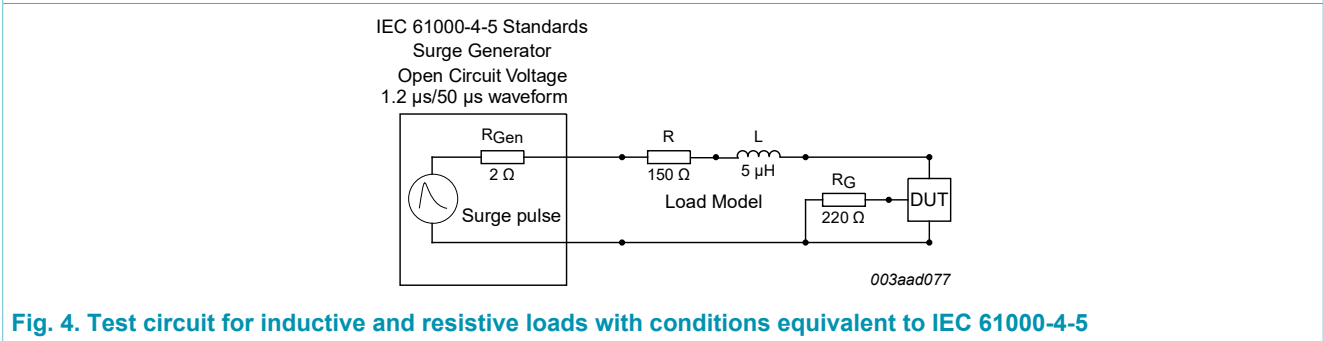


Fig. 4. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

### 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle with heatsink compound; <a href="#">Fig. 5</a>	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	full cycle; printed-circuit board mounted; lead length 4 mm	-	150	-	K/W

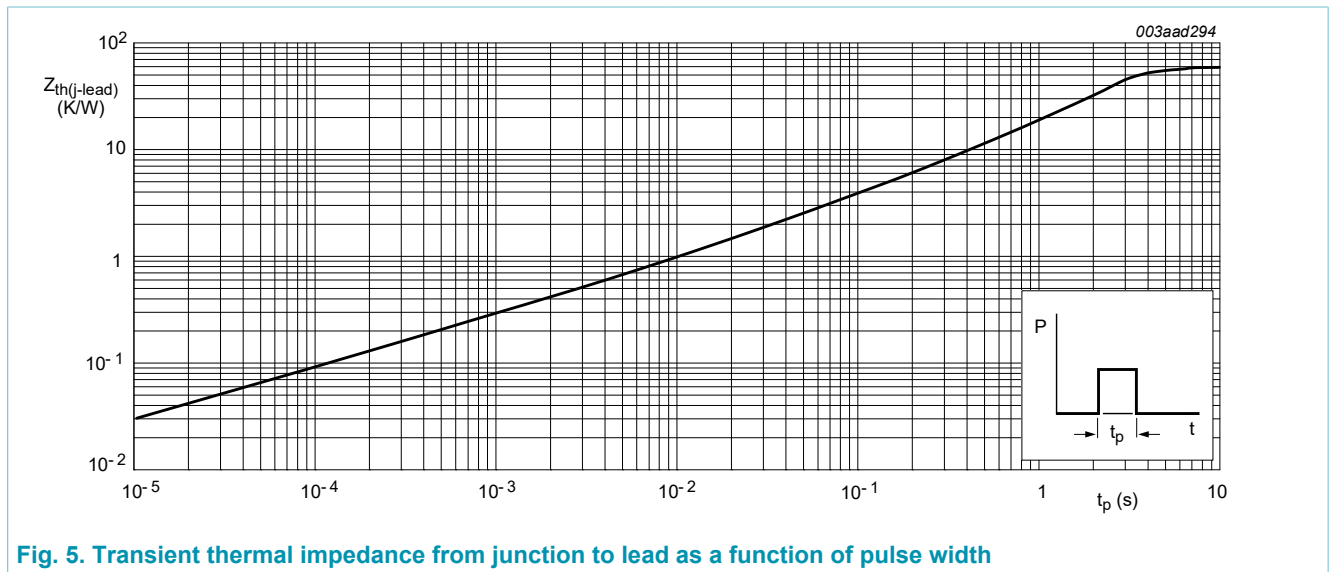


Fig. 5. Transient thermal impedance from junction to lead as a function of pulse width

### 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
I <sub>GT</sub>	gate trigger current	V <sub>D</sub> = 12 V; I <sub>T</sub> = 100 mA; LD+ G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 6</a>	0.5	-	5	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 100 mA; LD- G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 6</a>	0.5	-	5	mA
I <sub>L</sub>	latching current	V <sub>D</sub> = 12 V; I <sub>G</sub> = 100 mA; LD+ G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 7</a>	-	-	25	mA
		V <sub>D</sub> = 12 V; I <sub>G</sub> = 100 mA; LD- G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 7</a>	-	-	25	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>	-	-	20	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 1.1 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 9</a>	-	-	1.3	V
V <sub>GT</sub>	gate trigger voltage	V <sub>D</sub> = 400 V; I <sub>T</sub> = 100 mA; T <sub>j</sub> = 125 °C	0.15	-	-	V
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 100 mA; T <sub>j</sub> = 25 °C	-	-	0.9	V
I <sub>D</sub>	off-state current	V <sub>D</sub> = 600 V; T <sub>j</sub> = 25 °C	-	-	2	μA
		V <sub>D</sub> = 600 V; T <sub>j</sub> = 125 °C	-	-	0.2	mA
V <sub>CL</sub>	clamping voltage	I <sub>CL</sub> = 0.1 mA; t <sub>p</sub> = 1 ms; T <sub>j</sub> ≤ 125 °C	650	-	-	V
<b>Dynamic characteristics</b>						
dV <sub>D</sub> /dt	rate of rise of off-state voltage	V <sub>DM</sub> = 402 V; T <sub>j</sub> = 125 °C; (V <sub>DM</sub> = 67% of V <sub>DRM</sub> ); exponential waveform; gate open circuit; <a href="#">Fig. 10</a>	300	-	-	V/μs
di <sub>com</sub> /dt	rate of change of commutating current	V <sub>D</sub> = 400 V; T <sub>j</sub> = 125 °C; I <sub>T(RMS)</sub> = 1 A; dV <sub>com</sub> /dt = 15 V/μs; gate open circuit; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>	0.15	-	-	A/ms

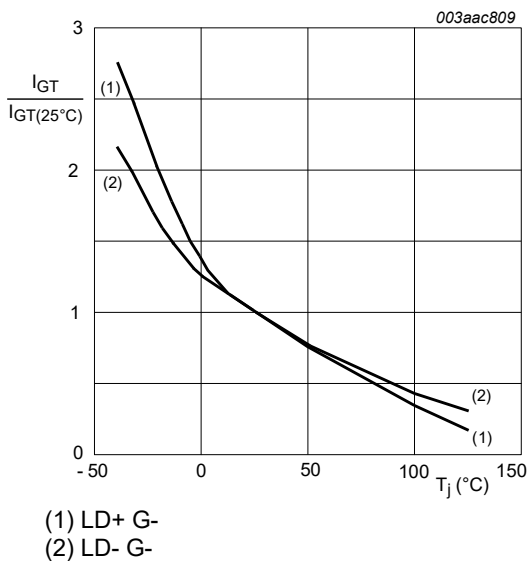


Fig. 6. Normalized gate trigger current as a function of junction temperature

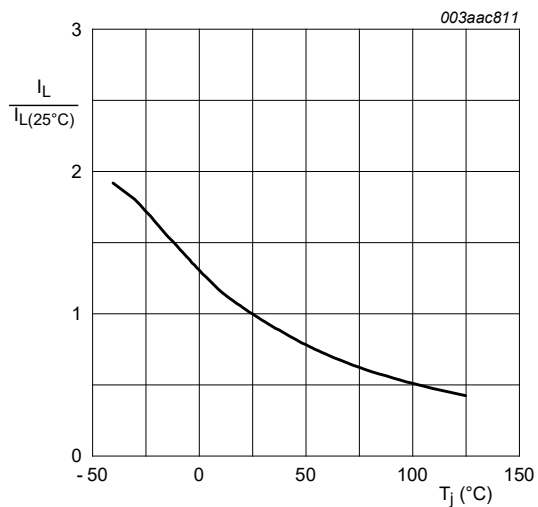


Fig. 7. Normalized latching current as a function of junction temperature

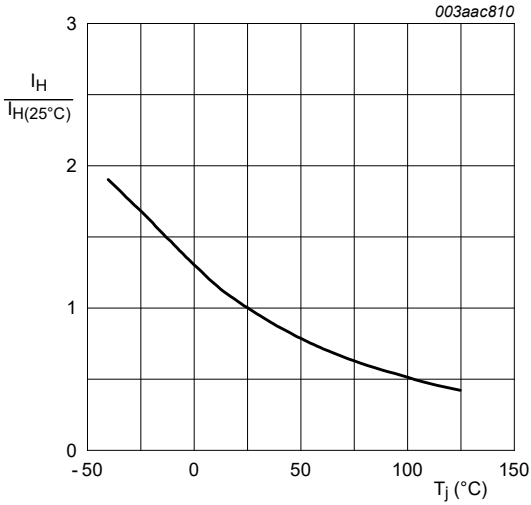
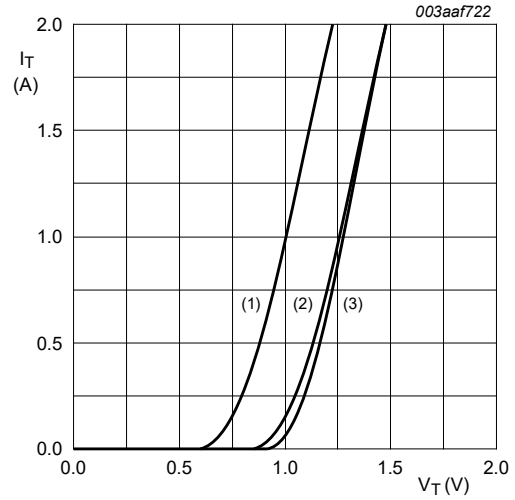


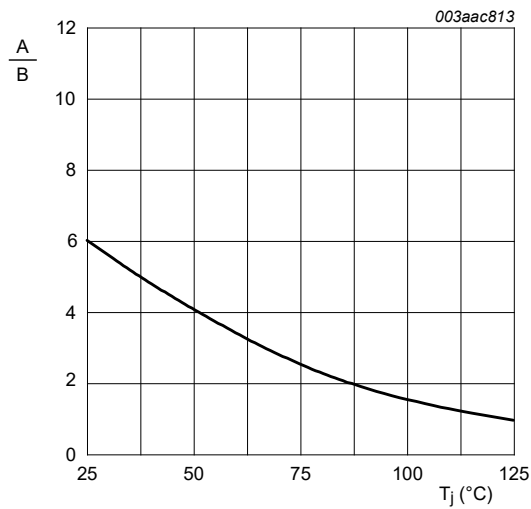
Fig. 8. Normalized holding current as a function of junction temperature



$V_o = 0.758 \text{ V}; R_s = 0.263 \Omega$

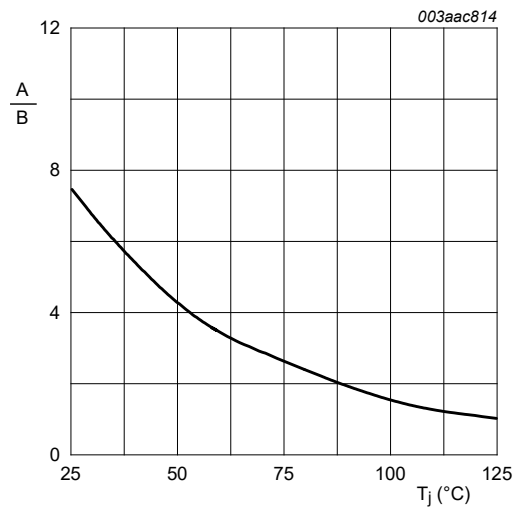
- (1)  $T_j = 125 \text{ }^\circ\text{C}$ ; typical values
- (2)  $T_j = 125 \text{ }^\circ\text{C}$ ; maximum values
- (3)  $T_j = 25 \text{ }^\circ\text{C}$ ; maximum values

Fig. 9. On-state current as a function of on-state voltage



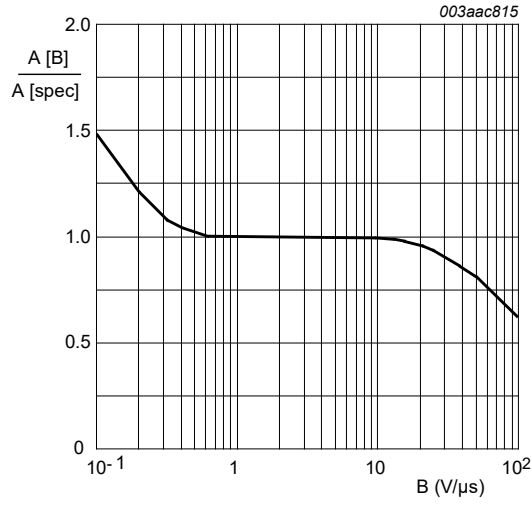
$A = dV_D/dt$  at condition  $T_j \text{ }^\circ\text{C}$   
 $B = dV_D/dt$  at condition  $T_j [125] \text{ }^\circ\text{C}$

Fig. 10. Normalized rate of rise of off-state voltage as a function of junction temperature



$A = di_{com}/dt$  at condition  $T_j \text{ }^\circ\text{C}$   
 $B = di_{com}/dt$  at condition  $T_j [125] \text{ }^\circ\text{C}$   
 $V_D = 400 \text{ V}$

Fig. 11. Normalized critical rate of rise of commutating current as a function of junction temperature



A [B] =  $dl_{com}/dt$  at condition B,  $dV_{com}/dt$   
 A [spec] is the data sheet value for  $dl_{com}/dt$   
 turn-off time is less than 20 ms

**Fig. 12. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values**



### 10. Package outline

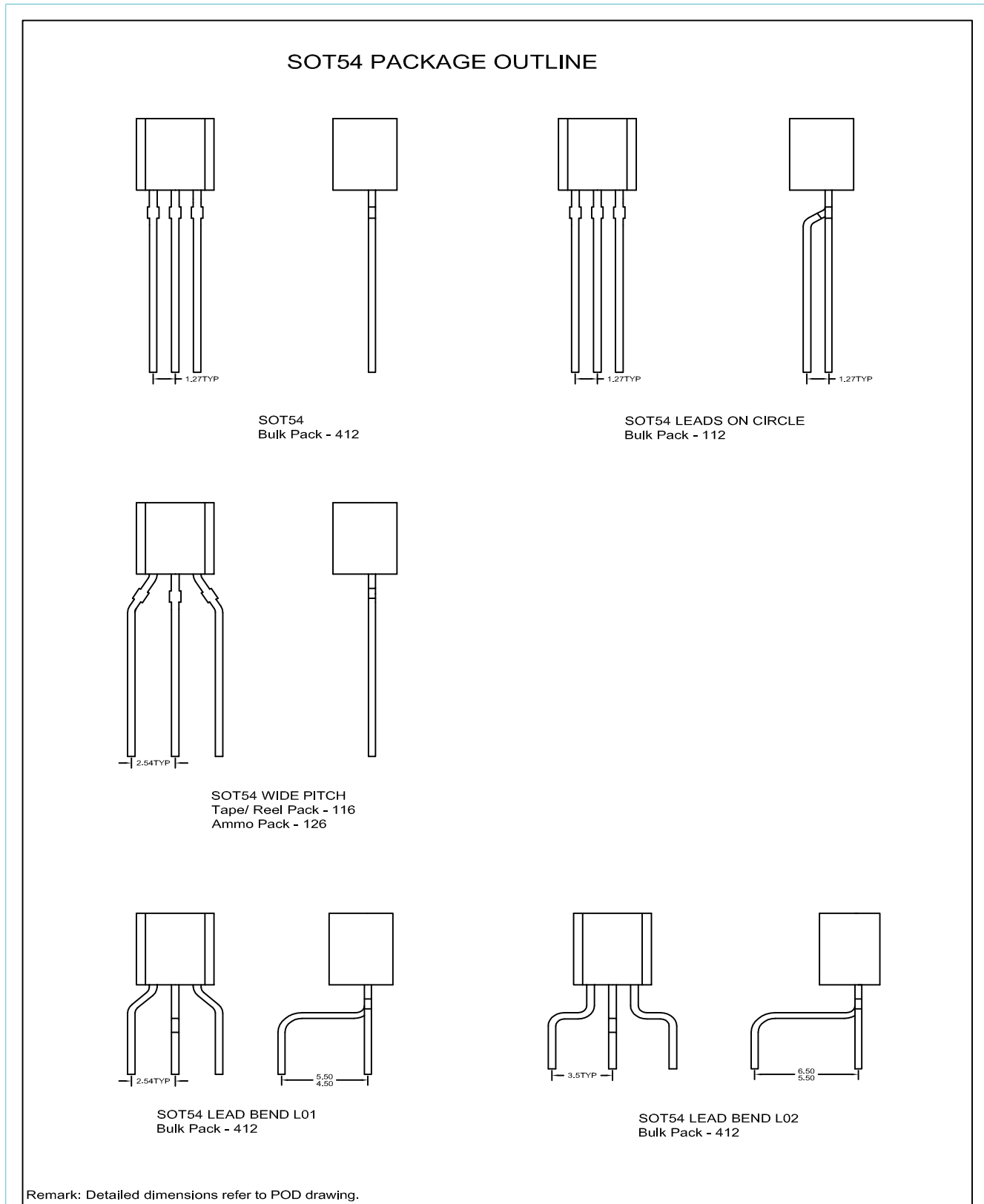


Fig. 13. Package outline TO-92 (SOT54)

## 11. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 22 September 2016