

# BT149 series

## Thyristors logic level

Rev. 5 — 1 November 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Passivated, sensitive gate thyristors in a SOT54 plastic package.

### 1.2 Features and benefits

- Designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

### 1.3 Applications

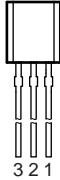

- General purpose switching and phase control.

### 1.4 Quick reference data

- $V_{\text{DRM}}, V_{\text{RRM}} \leq 200 \text{ V}$  (BT149B)
- $V_{\text{DRM}}, V_{\text{RRM}} \leq 400 \text{ V}$  (BT149D)
- $V_{\text{DRM}}, V_{\text{RRM}} \leq 600 \text{ V}$  (BT149G)
- $I_{\text{T(RMS)}} \leq 0.8 \text{ A}$
- $I_{\text{T(AV)}} \leq 0.5 \text{ A}$
- $I_{\text{TSM}} \leq 8 \text{ A}$ .

## 2. Pinning information

Table 1. Discrete pinning

Pin	Description	Simplified outline	Symbol
1	cathode (K)		
2	gate (G)		
3	anode (A)		

**SOT54 (TO-92)**

### 3. Ordering information

**Table 2. Ordering information**

Type number	Package		Version
	Name	Description	
BT149B	-	plastic single-ended leaded (through hole) package; 3 leads	SOT54
BT149D			
BT149G			

### 4. Limiting values

**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}, V_{RRM}$	repetitive peak off-state voltage				
	BT149B		[1] -	200	V
	BT149D		[1] -	400	V
	BT149G		[1] -	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83\text{ °C}$ ; see <a href="#">Figure 1</a>	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles; see <a href="#">Figure 4</a> and <a href="#">5</a>	-	0.8	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_j = 25\text{ °C}$ prior to surge; see <a href="#">Figure 2</a> and <a href="#">3</a>			
		$t = 10\text{ ms}$	-	8	A
		$t = 8.3\text{ ms}$	-	9	A
$I^2t$	$I^2t$ for fusing	$t = 10\text{ ms}$	-	0.32	$A^2s$
$di_T/dt$	repetitive rate of rise of on-state current after triggering	$I_{TM} = 2\text{ A}$ ; $I_G = 10\text{ mA}$ ; $di_G/dt = 100\text{ mA}/\mu s$	-	50	$A/\mu s$
$I_{GM}$	peak gate current		-	1	A
$V_{GM}$	peak gate voltage		-	5	V
$V_{RGM}$	peak reverse gate voltage		-	5	V
$P_{GM}$	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
$T_{stg}$	storage temperature		-40	+150	$^{\circ}C$
$T_j$	junction temperature		-	125	$^{\circ}C$

- [1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ $\mu s$ .

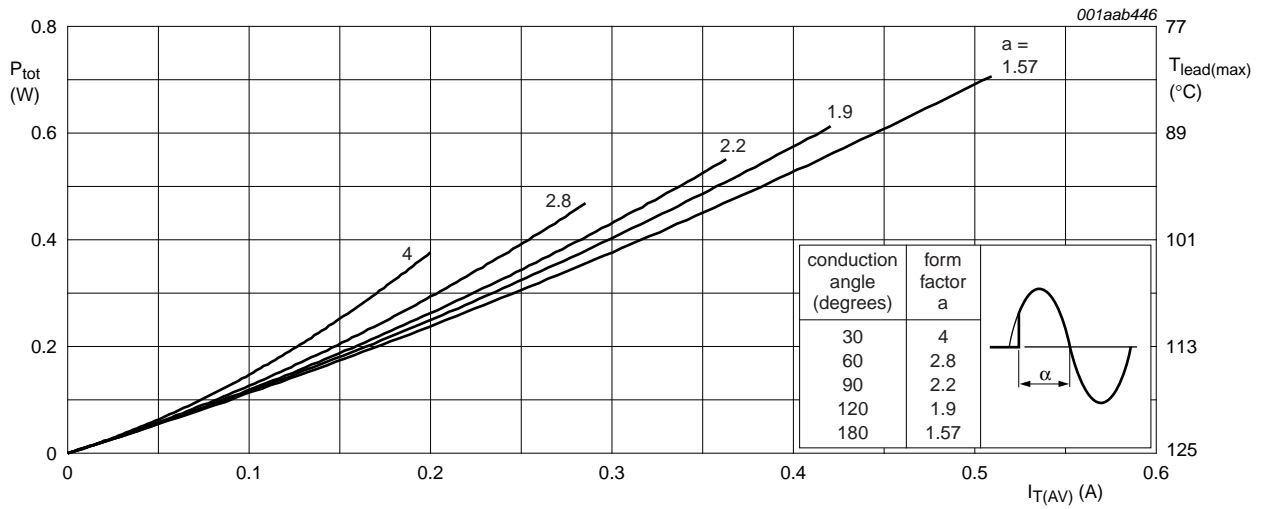


Fig 1. Total power dissipation as a function of average on-state current; maximum values

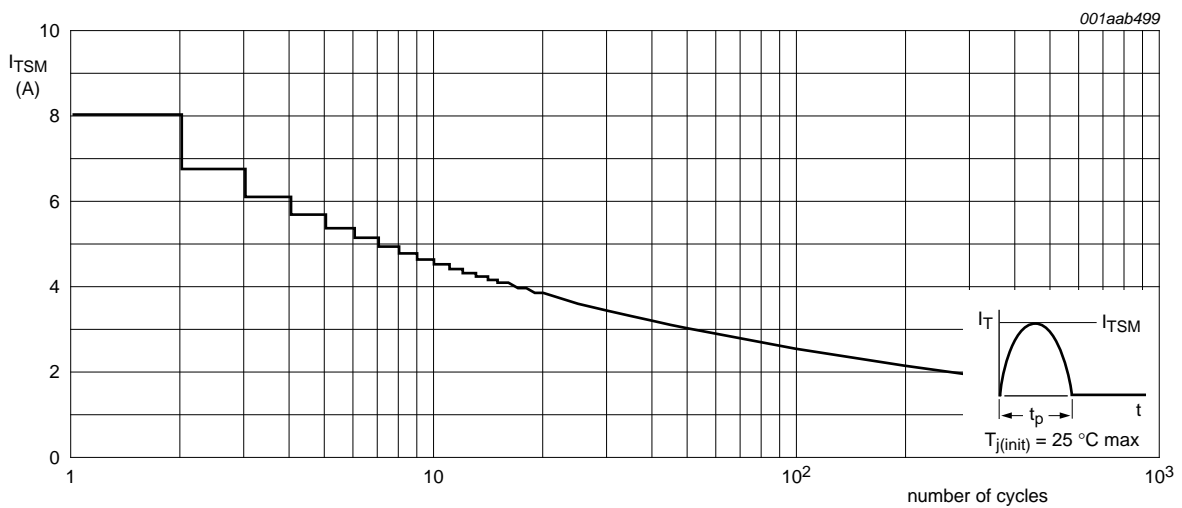
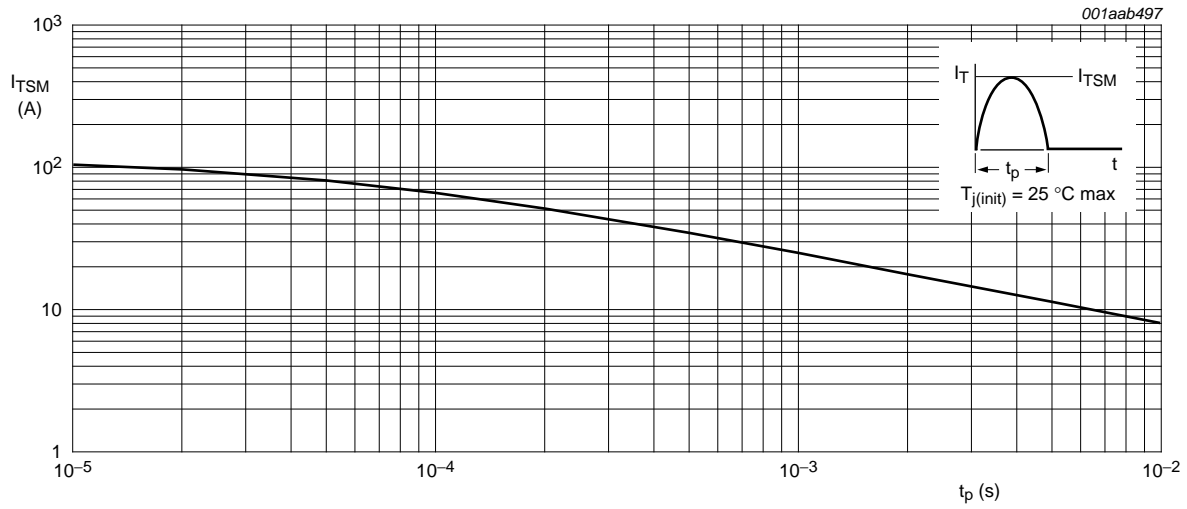
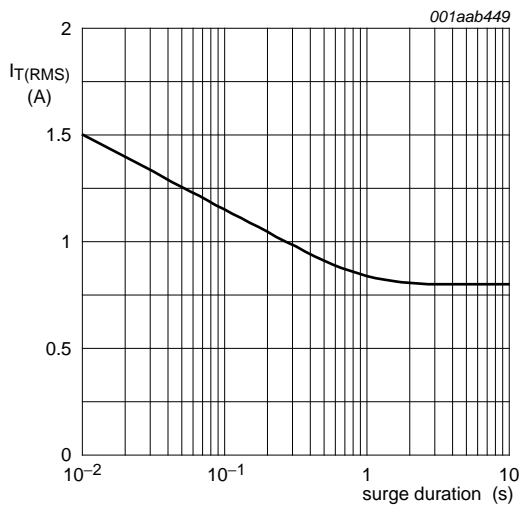


Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



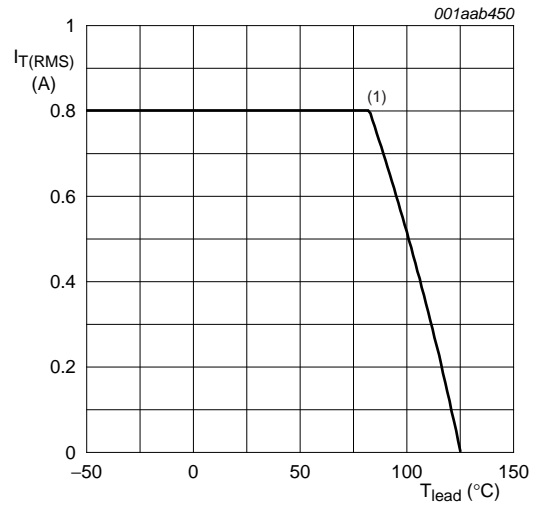
$t_p \leq 10\text{ ms.}$

**Fig 3. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values**



$f = 50\text{ Hz; } T_{lead} \leq 83\text{ °C.}$

**Fig 4. RMS on-state current as a function of surge duration, for sinusoidal currents; maximum values**



(1)  $T_{lead} = 83\text{ °C}$

**Fig 5. RMS on-state current as a function of lead temperature; maximum values**

### 5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead		-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed-circuit board mounted; lead length = 4 mm	-	150	-	K/W

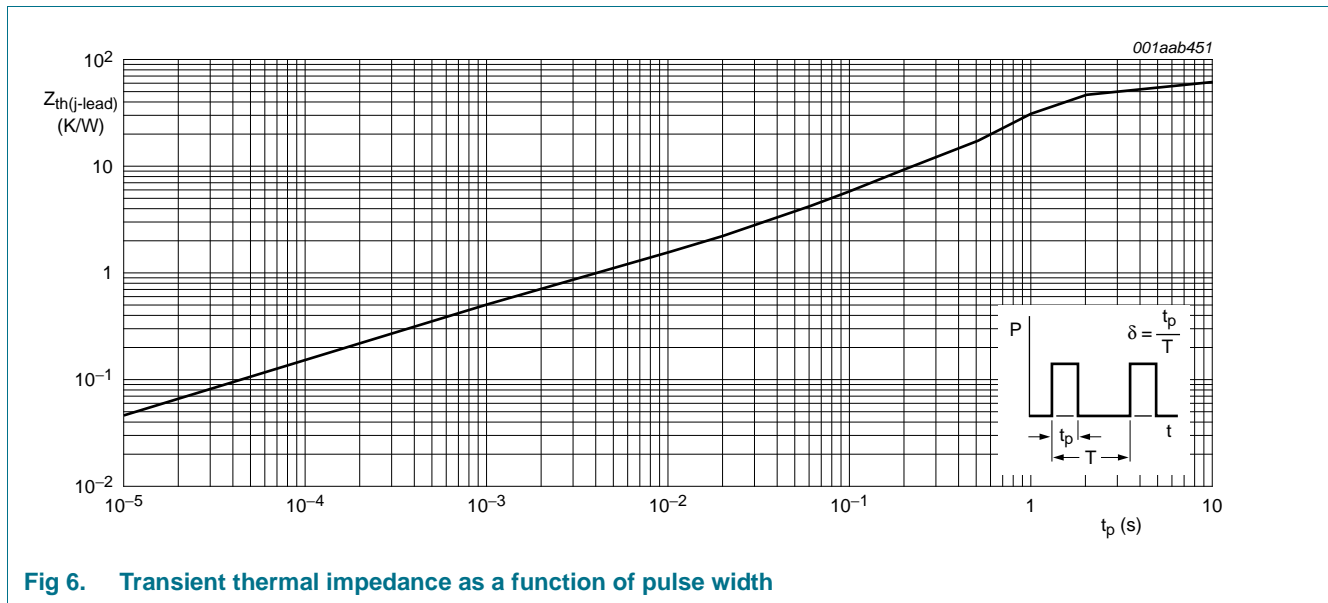


Fig 6. Transient thermal impedance as a function of pulse width

## 6. Characteristics

**Table 5. Characteristics**

$T_j = 25\text{ °C}$  unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 10\text{ mA}$ ; gate open circuit; see <a href="#">Figure 8</a>	-	50	200	$\mu\text{A}$
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_{GT} = 0.5\text{ mA}$ ; $R_{GK} = 1\text{ k}\Omega$ ; see <a href="#">Figure 10</a>	-	2	6	$\text{mA}$
$I_H$	holding current	$V_D = 12\text{ V}$ ; $I_{GT} = 0.5\text{ mA}$ ; $R_{GK} = 1\text{ k}\Omega$ ; see <a href="#">Figure 11</a>	-	2	5	$\text{mA}$
$V_T$	on-state voltage	$I_T = 1.2\text{ A}$	-	1.25	1.7	$\text{V}$
$V_{GT}$	gate trigger voltage	$I_T = 10\text{ mA}$ ; gate open circuit; see <a href="#">Figure 7</a>	-	-	-	-
		$V_D = 12\text{ V}$	-	0.5	0.8	$\text{V}$
		$V_D = V_{DRM(max)}$ ; $T_j = 125\text{ °C}$	0.2	0.3	-	$\text{V}$
$I_D, I_R$	off-state leakage current	$V_D = V_{DRM(max)}$ ; $V_R = V_{RRM(max)}$ ; $T_j = 125\text{ °C}$ ; $R_{GK} = 1\text{ k}\Omega$	-	0.05	0.1	$\text{mA}$
<b>Dynamic characteristics</b>						
$dV_D/dt$	critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}$ ; $T_j = 125\text{ °C}$ ; exponential waveform; see <a href="#">Figure 12</a>	-	-	-	-
		gate open circuit	-	25	-	$\text{V}/\mu\text{s}$
		$R_{GK} = 1\text{ k}\Omega$	500	800	-	$\text{V}/\mu\text{s}$
$t_{gt}$	gate controlled turn-on time	$I_{TM} = 2\text{ A}$ ; $V_D = V_{DRM(max)}$ ; $I_G = 10\text{ mA}$ ; $dI_G/dt = 0.1\text{ A}/\mu\text{s}$	-	2	-	$\mu\text{s}$
$t_q$	circuit commuted turn-off time	$V_D = 67\% V_{DRM(max)}$ ; $T_j = 125\text{ °C}$ ; $I_{TM} = 1.6\text{ A}$ ; $V_R = 35\text{ V}$ ; $dI_{TM}/dt = 30\text{ A}/\mu\text{s}$ ; $dV_D/dt = 2\text{ V}/\mu\text{s}$ ; $R_{GK} = 1\text{ k}\Omega$	-	100	-	$\mu\text{s}$

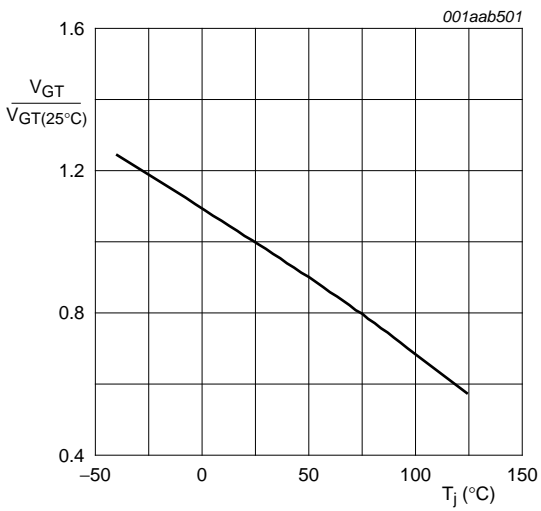


Fig 7. Normalized gate trigger voltage as a function of junction temperature

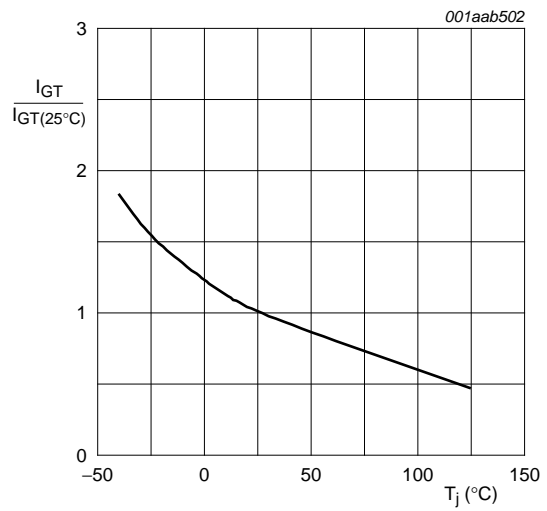
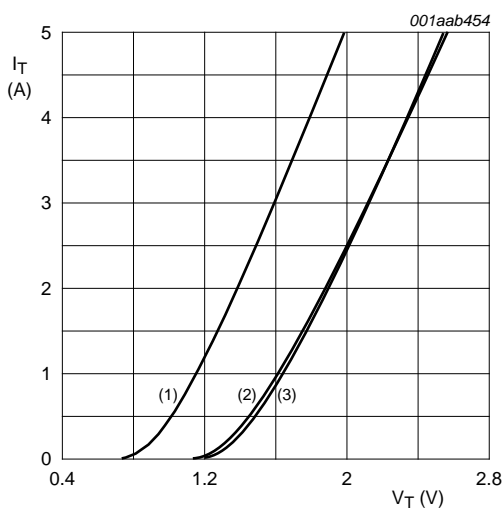
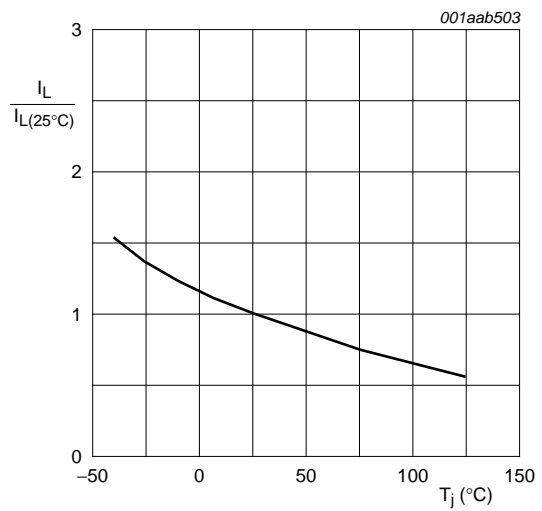


Fig 8. Normalized gate trigger current as a function of junction temperature



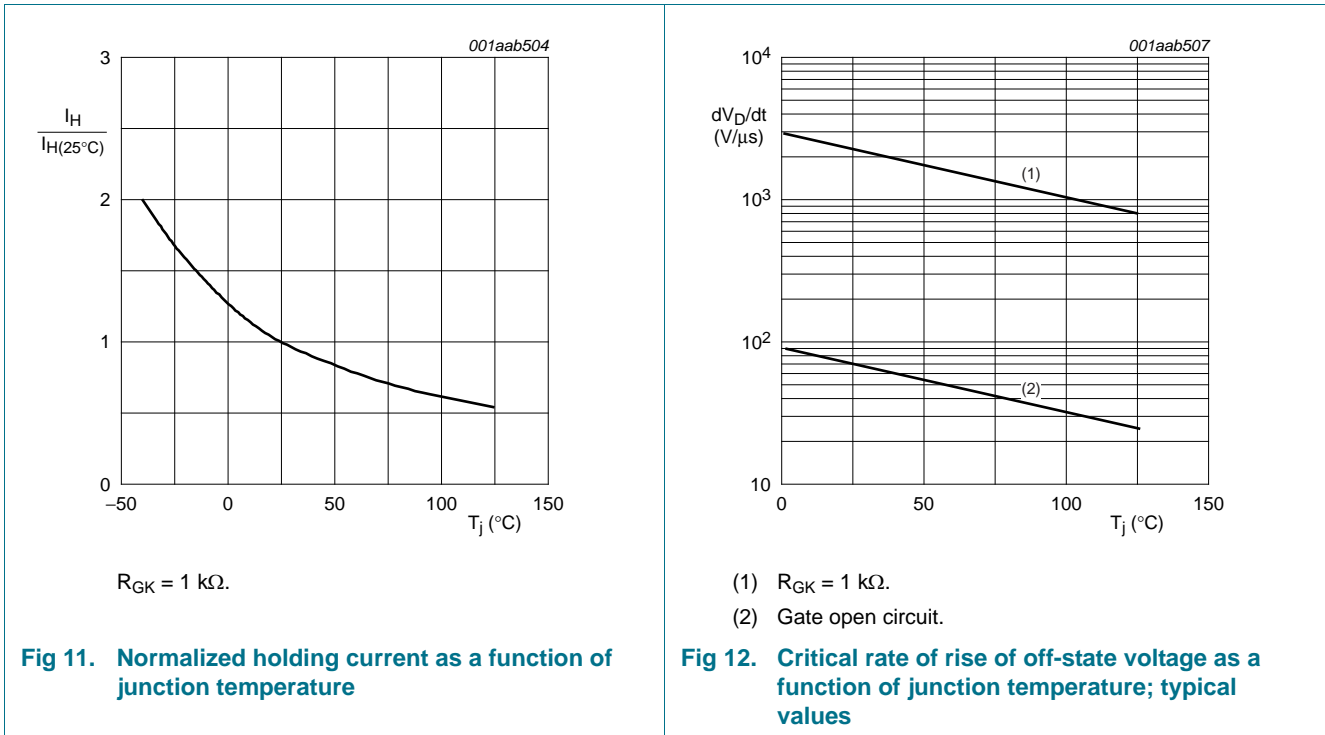
$V_O = 1.067 \text{ V.}$   
 $R_S = 0.187 \text{ }\Omega.$   
 (1)  $T_j = 125 \text{ }^\circ\text{C; typical values}$   
 (2)  $T_j = 125 \text{ }^\circ\text{C; maximum values}$   
 (3)  $T_j = 25 \text{ }^\circ\text{C; maximum values}$

Fig 9. On-state current characteristics



$R_{GK} = 1 \text{ k}\Omega.$

Fig 10. Normalized latching current as a function of junction temperature



## 7. Package information

Epoxy meets requirements of UL94 V-0 at 1/8 inch.



8. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

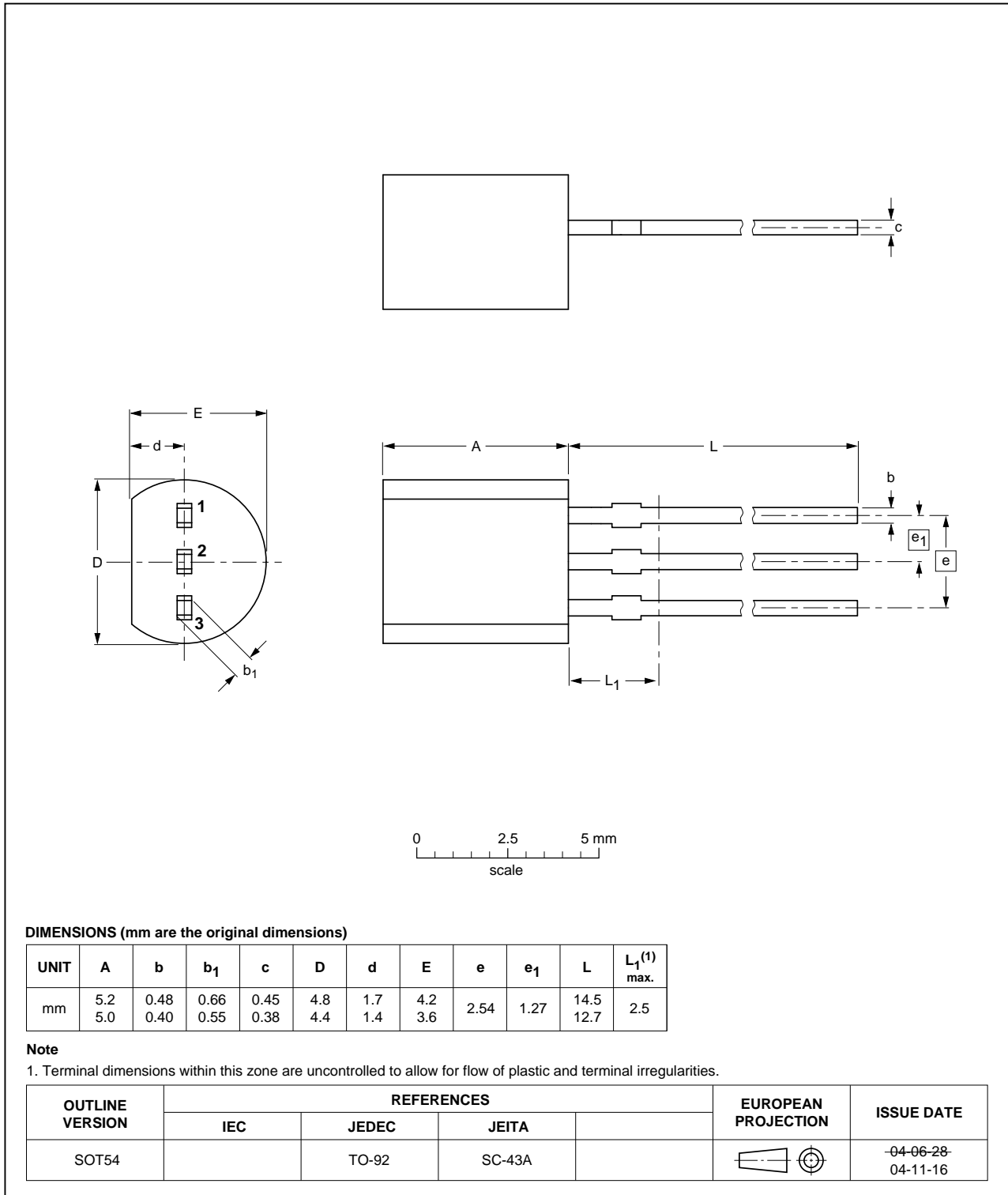


Fig 13. Package outline SOT54 (TO-92)

## 9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BT149_SER v.5	20111101	Product data sheet		BT149_SERIES v.4
Modifications:			<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>	
BT149_SERIES v.4	20040820	Product data sheet		BT149_SERIES v.3
BT149_SERIES v.3	20010902	Product specification		BT149_SERIES v.2
BT149_SERIES v.2	20010901	Product specification		BT149_SERIES v.1
BT149_SERIES v.1	19970901	Product specification		-

## 10. Legal information

### 10.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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