

# ESD7371, SZESD7371 Series

## ESD Protection Diode

### Ultra-Low Capacitance

The ESD7371 Series is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, high breakdown voltage, high linearity, low leakage, and fast response time make these parts ideal for ESD protection on designs where board space is at a premium. It has industry leading capacitance linearity over voltage making it ideal for RF applications. This capacitance linearity combined with the extremely small package and low insertion loss makes this part well suited for use in antenna line applications for wireless handsets and terminals.

#### Features

- Industry Leading Capacitance Linearity Over Voltage
- Low Capacitance (0.7 pF Max, I/O to GND)
- Stand-off Voltage: 5.3 V
- Low Leakage: < 1 nA
- Low Dynamic Resistance < 1  $\Omega$
- IEC61000-4-2 Level 4 ESD Protection
- 1000 ESD IEC61000-4-2 Strikes  $\pm 8$  kV Contact / Air Discharged
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Typical Applications

- RF Signal ESD Protection
- RF Switching, PA, and Antenna ESD Protection
- Near Field Communications
- USB 2.0, USB 3.0

#### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
IEC 61000-4-2 (ESD) (Note 1)		20	kV
IEC 61000-4-5 (ESD) (Note 2)		3.0	A
Total Power Dissipation (Note 3) @ $T_A = 25^\circ\text{C}$	$P_D$	300	mW
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	400	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature – Maximum (10 Second Duration)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

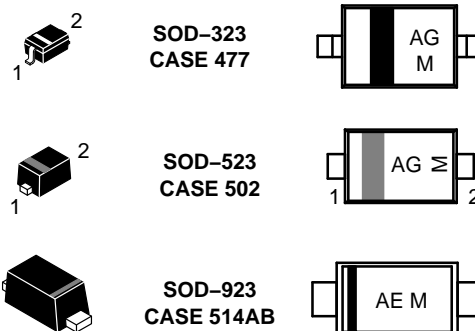
1. Non-repetitive current pulse at  $T_A = 25^\circ\text{C}$ , per IEC61000-4-2 waveform.
2. Non-repetitive current pulse at  $T_A = 25^\circ\text{C}$ , per IEC61000-4-5 waveform.
3. Mounted with recommended minimum pad size, DC board FR-4



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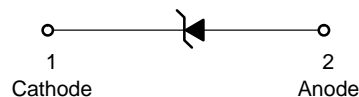
[www.onsemi.com](http://www.onsemi.com)

#### MARKING DIAGRAMS



X, XX = Specific Device Code  
M = Date Code

#### PIN CONFIGURATION AND SCHEMATIC



#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

## ESD7371, SZESD7371 Series

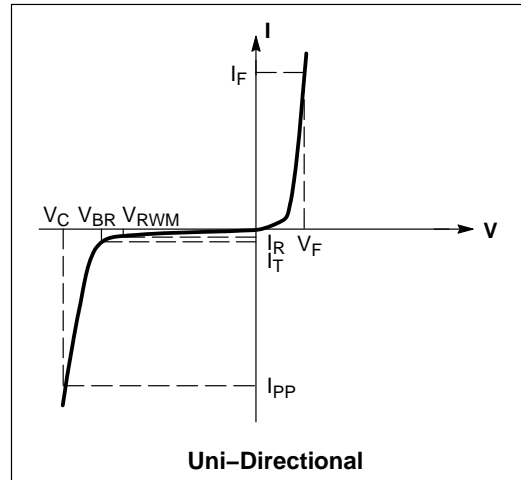
See Application Note AND8308/D for further description of survivability specs.

### ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current

\*See Application Note AND8308/D for detailed explanations of datasheet parameters.



### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$				5.3	V
Breakdown Voltage (Note 4)	$V_{BR}$	$I_T = 1\text{ mA}$	7.0			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 5.3\text{ V}$		< 1.0	50	nA
Clamping Voltage (Note 5)	$V_C$	$I_{PP} = 1\text{ A}$		11	15	V
Clamping Voltage (Note 5)	$V_C$	$I_{PP} = 3\text{ A}$		14	20	V
Junction Capacitance	$C_J$	$V_R = 0\text{ V}, f = 1\text{ MHz}$ $V_R = 0\text{ V}, f < 1\text{ GHz}$		0.43 0.39	0.7 0.7	pF
Dynamic Resistance	$R_{DYN}$	TLP Pulse		0.45		$\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Breakdown voltage is tested from pin 1 to 2 and pin 2 to 1.
5. Non-repetitive current pulse at  $T_A = 25^\circ\text{C}$ , per IEC61000-4-5 waveform.

# ESD7371, SZESD7371 Series

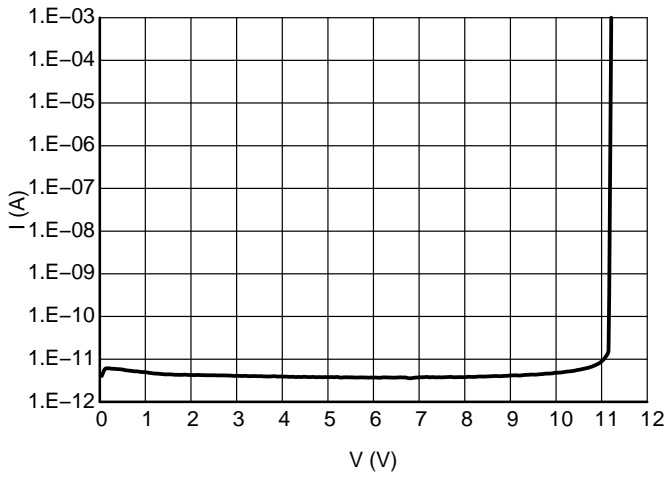


Figure 1. IV Characteristics

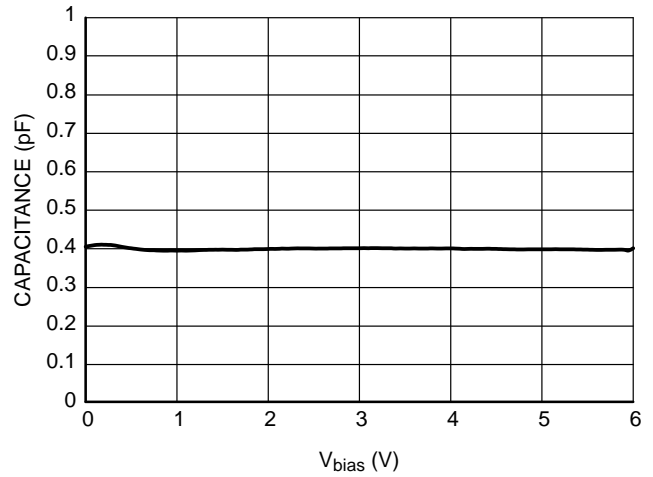


Figure 2. CV Characteristics

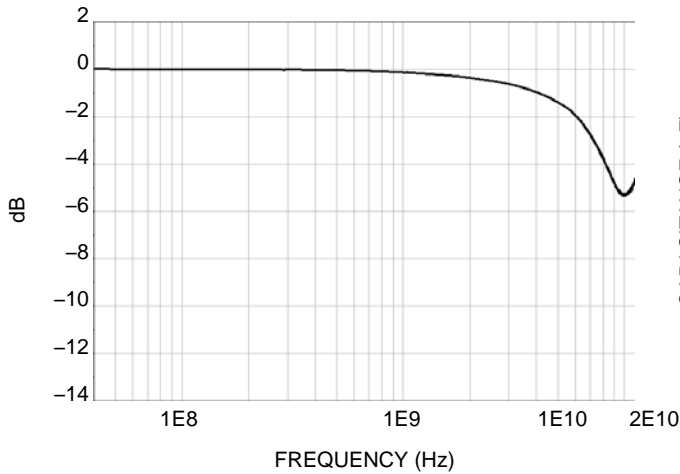


Figure 3. RF Insertion Loss

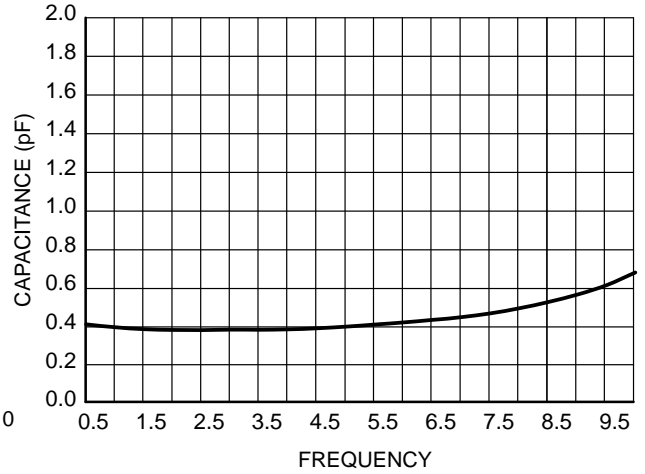


Figure 4. Capacitance over Frequency

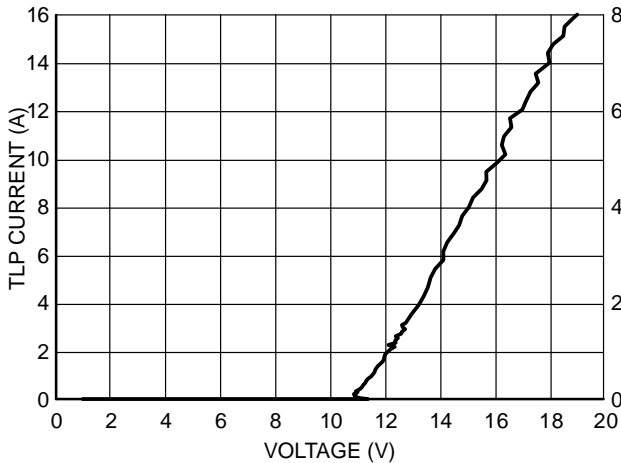


Figure 5. Positive TLP I-V Curve

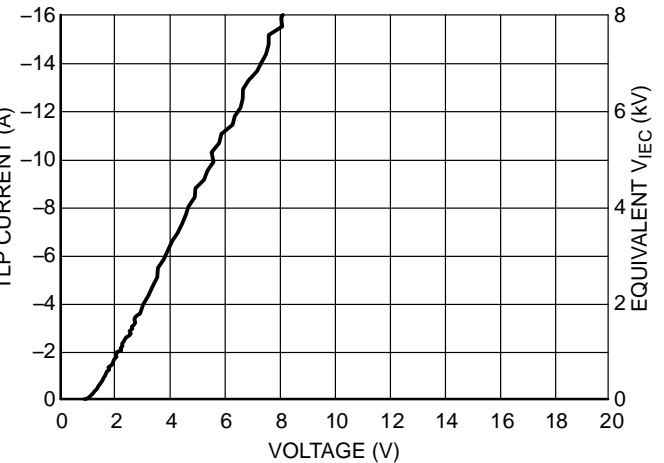


Figure 6. Negative TLP I-V Curve

# ESD7371, SZESD7371 Series

## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Figure 7. IEC61000-4-2 Spec

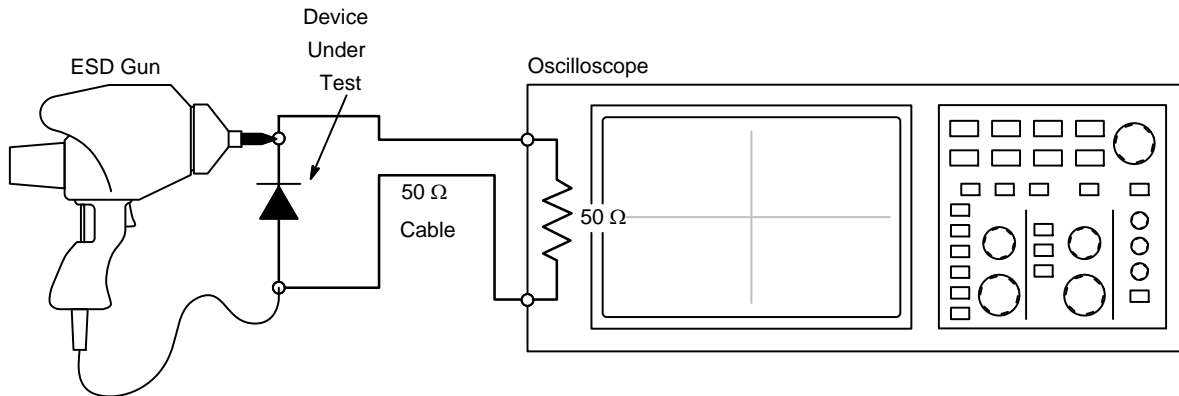


Figure 8. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

### Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained

from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 9. TLP I-V curves of ESD protection devices accurately demonstrate the product’s ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 10 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

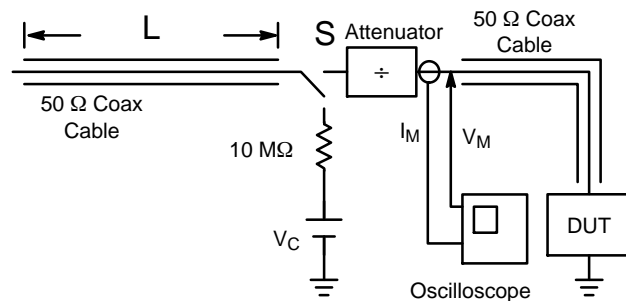
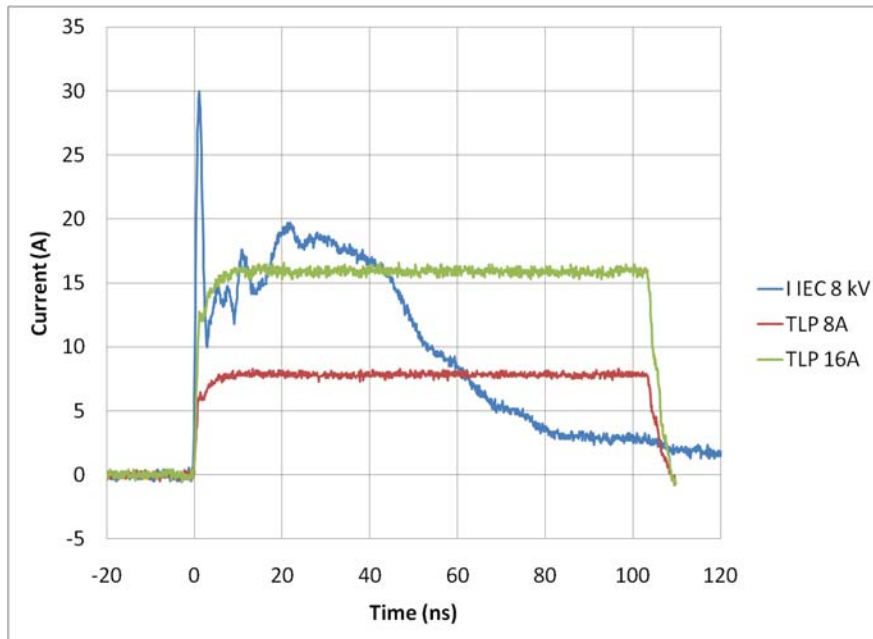


Figure 9. Simplified Schematic of a Typical TLP System

## ESD7371, SZESD7371 Series



**Figure 10. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms**

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
ESD7371HT1G, SZESD7371HT1G*	SOD-323 (Pb-Free)	3000 / Tape & Reel
ESD7371XV2T1G, SZESD7371XV2T1G*	SOD-523 (Pb-Free)	3000 / Tape & Reel
ESD7371XV2T5G, SZESD7371XV2T5G*	SOD-523 (Pb-Free)	8000 / Tape & Reel
ESD7371P2T5G, SZESD7371P2T5G*	SOD-923 (Pb-Free)	8000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE

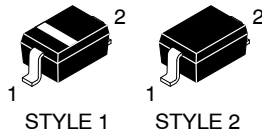
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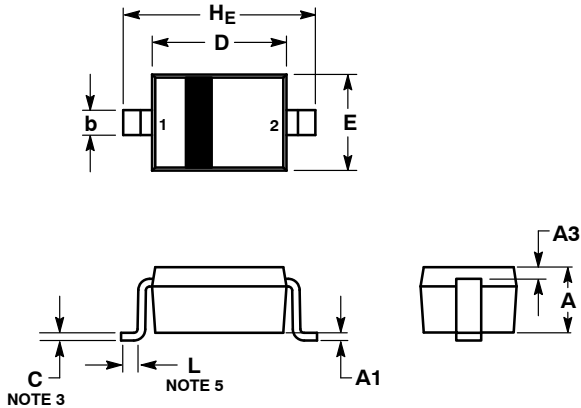


SOD-323  
CASE 477-02  
ISSUE H

DATE 13 MAR 2007



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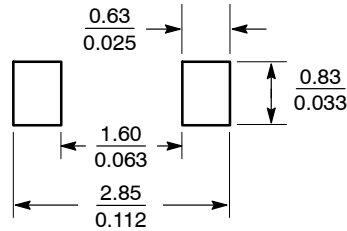


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS SPECIFIED PER L/F DRAWING WITH SOLDER PLATING.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DIMENSION L IS MEASURED FROM END OF RADIUS.

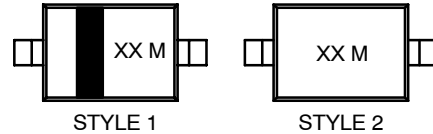
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3	0.15 REF			0.006 REF		
b	0.25	0.32	0.4	0.010	0.012	0.016
C	0.089	0.12	0.177	0.003	0.005	0.007
D	1.60	1.70	1.80	0.062	0.066	0.070
E	1.15	1.25	1.35	0.045	0.049	0.053
L	0.08			0.003		
HE	2.30	2.50	2.70	0.090	0.098	0.105

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XX = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLE 1: PIN 1. CATHODE (POLARITY BAND)  
2. ANODE

STYLE 2: NO POLARITY

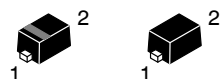
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DESCRIPTION:	SOD-323	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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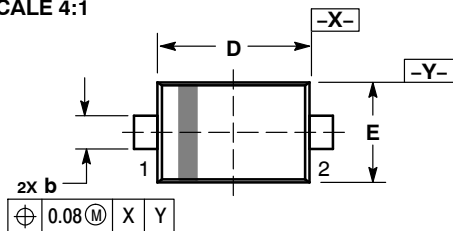


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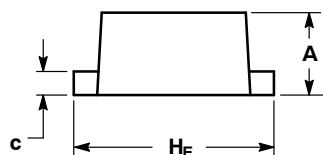
**SOD-523**  
CASE 502-01  
ISSUE E

DATE 28 SEP 2010

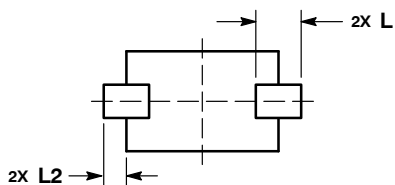
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TOP VIEW

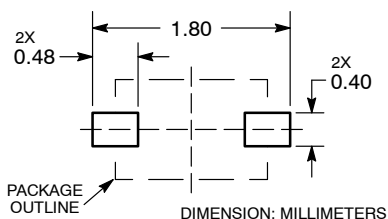


SIDE VIEW



BOTTOM VIEW

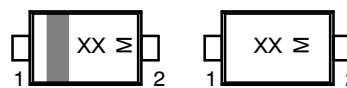
### RECOMMENDED SOLDERING FOOTPRINT\*



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.50	0.60	0.70
b	0.25	0.30	0.35
c	0.07	0.14	0.20
D	1.10	1.20	1.30
E	0.70	0.80	0.90
HE	1.50	1.60	1.70
L	0.30 REF		
L2	0.15	0.20	0.25

### GENERIC MARKING DIAGRAM\*



STYLE 1

STYLE 2

XX = Specific Device Code  
M    Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLE 1:  
PIN 1. CATHODE (POLARITY BAND)  
2. ANODE

STYLE 2:  
NO POLARITY

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

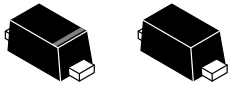
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# MECHANICAL CASE OUTLINE

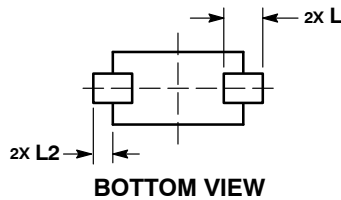
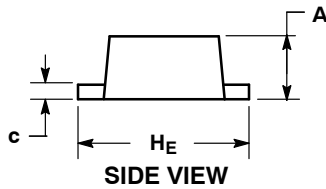
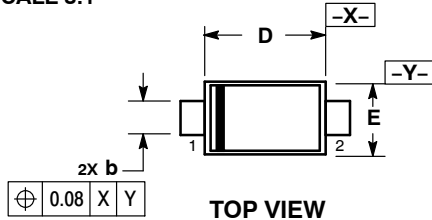
## PACKAGE DIMENSIONS

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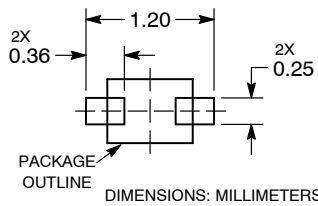


STYLE 1      STYLE 2

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### SOLDERING FOOTPRINT\*



SOD-923  
CASE 514AB  
ISSUE D

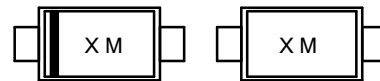
DATE 03 SEP 2020

#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. DIMENSION L WILL NOT EXCEED 0.30mm.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.37	0.40	0.013	0.015	0.016
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.07	0.12	0.17	0.003	0.005	0.007
D	0.75	0.80	0.85	0.030	0.031	0.033
E	0.55	0.60	0.65	0.022	0.024	0.026
HE	0.95	1.00	1.05	0.037	0.039	0.041
L	0.19 REF			0.007 REF		
L2	0.05	0.10	0.15	0.002	0.004	0.006

### GENERIC MARKING DIAGRAM\*



STYLE 1

STYLE 2

X = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLE 1:      STYLE 2:  
PIN 1. CATHODE (POLARITY BAND)      NO POLARITY  
2. ANODE

See Application Note AND8455/D for more mounting details

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Phone: 011 421 33 790 2910

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Phone: 00421 33 790 2910

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