MOSFET - Power, Single

N-Channel

100 V, 3.6 mΩ, 131 A

NTMFS3D6N10MCL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	100	V
Gate-to-Source Voltage	Э		V _{GS}	±20	V
Continuous Drain		T _C = 25°C	I _D	131	Α
Current R _{θJC} (Notes 1, 3)	Steady	T _C = 100°C		93	
Power Dissipation $R_{\theta JC}$ (Note 1)	State	T _C = 25°C	P _D	136	W
Continuous Drain Current R _{0JA} (Notes 1, 2, 3)	Steady State	T _A = 25°C	I _D	19.5	Α
Power Dissipation R _{θJA} (Notes 1, 2)	State	T _A = 25°C	P _D	3.0	W
Pulsed Drain Current	$T_A = 25^{\circ}C$, $t_p = 10 \mu s$		I _{DM}	1674	Α
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +175	°C
Single Pulse Drain-to-Source Avalanche Energy (L = 3 mH, I _{AS} = 14 A)			E _{AS}	294	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	1.1	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	50	

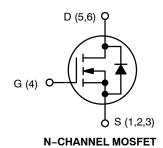
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- 3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



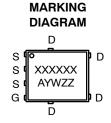
ON Semiconductor®

www.onsemi.com

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX	
100 V	3.6 m Ω @ 10 V	131 A	
100 V	5.8 mΩ @ 4.5 V	1017	







XXXXXX = Specific Device Code

A = Assembly Location

Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 3 of this data sheet.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•					1	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /				60		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 100 V	T _J = 25 °C			1.0	μΑ
			T _J = 125°C			250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D =$	= 270 μA	1	1.5	3	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-5.0		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 48 A		3.0	3.6	
		V _{GS} = 4.5 V	I _D = 39 A		4.4	5.8	mΩ
Forward Transconductance	9 _{FS}	V _{DS} =5 V, I _D	= 48 A		163		S
CHARGES, CAPACITANCES & GATE RE	SISTANCE						
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 50 V			4411		
Output Capacitance	C _{OSS}				1808		pF
Reverse Transfer Capacitance	C _{RSS}				29		
Gate Resistance	R_{G}			0.1	0.7	3	Ω
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 50 V; I _D = 48 A			29		nC
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 50 V; I _D = 48 A			60		nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 10 V, V _{DS} = 50 V; I _D = 48 A			6		
Gate-to-Source Charge	Q _{GS}				10		nC
Gate-to-Drain Charge	Q_{GD}				7		
Plateau Voltage	V_{GP}				3		V
Output Charge	Q _{OSS}	V _{GS} = 0 V, V _{DS} = 50 V			119		nC
Total Gate Charge Sync	Q _{SYNC}	V _{GS} = 0 to 10 V, V _{DS} = 0 V			51		nC
SWITCHING CHARACTERISTICS (Note 5)						
Turn-On Delay Time	t _{d(ON)}				14		
Rise Time	t _r	V_{GS} = 10 V, V_{DS} = 50 V, I_{D} = 48 A, R_{G} = 6.0 Ω			11]
Turn-Off Delay Time	t _{d(OFF)}				42		ns
Fall Time	t _f				8		1
DRAIN-SOURCE DIODE CHARACTERIS	TICS						
Source to Drain Diode Forward Voltage	V_{SD}	V _{GS} = 0 V, I _S = 2 A	(Note 7)		0.65	1.2	V
		V _{GS} = 0 V, I _S = 48 A	(Note 7)		0.83	1.3	1
Reverse Recovery Time	t _{rr}		000 4/		34		ns
Reverse Recovery Charge	Q _{rr}	I _F = 24 A, di/dt = 300 A/μs			73		nC
Reverse Recovery Time	t _{rr}	I _F = 24 A, di/dt = 1000 A/μs			28		ns
Reverse Recovery Charge	Q _{rr}				183		nC

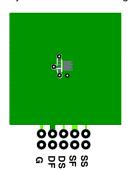
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

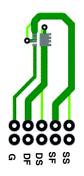
5. Switching characteristics are independent of operating junction temperatures.

NOTES:

6. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 \times 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

- 7. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.
- 8. E_{AS} of 294 mJ is based on starting T_J = 25°C; L = 3 mH, I_{AS} = 14 A, V_{DD} = 100 V, V_{GS} = 10 V.
 9. Pulsed I_D please refer to Figure 11 SOA graph for more details.
- 10. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTMFS3D6N10MCLT1G	3D6L10	DFN5 (Pb-Free)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

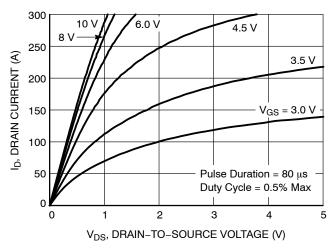


Figure 1. On-Region Characteristics

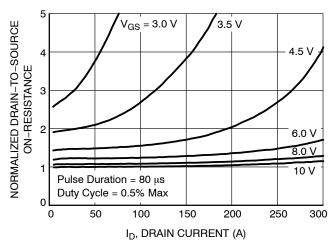


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

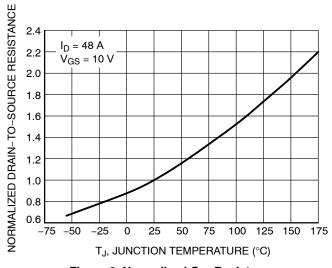


Figure 3. Normalized On-Resistance vs. Junction Temperature

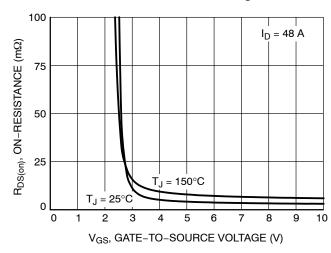


Figure 4. On-Resistance vs. Gate-to-Source Voltage

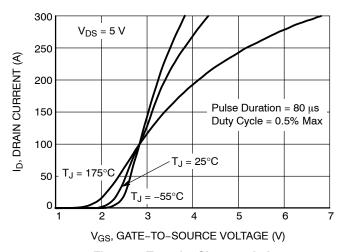


Figure 5. Transfer Characteristics

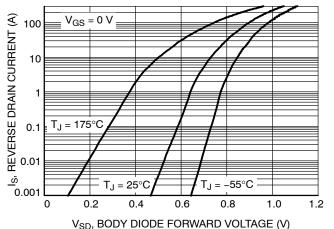


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS

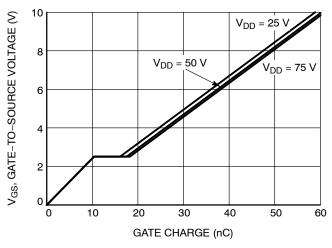


Figure 7. Gate Charge Characteristics

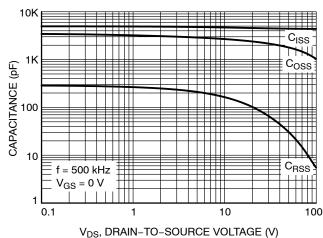


Figure 8. Capacitance vs. Drain-to-Source Voltage

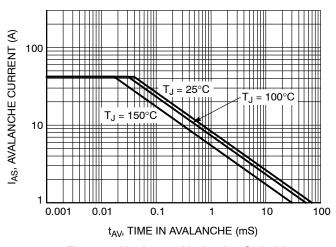


Figure 9. Unclamped Inductive Switching Capability

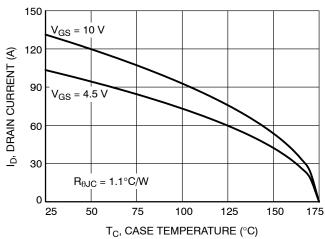


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

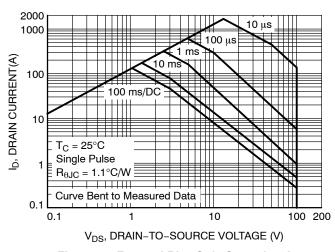


Figure 11. Forward Bias Safe Operating Area

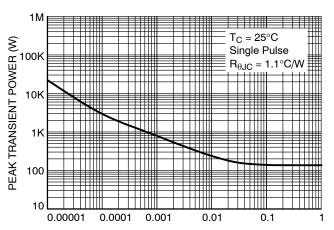


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

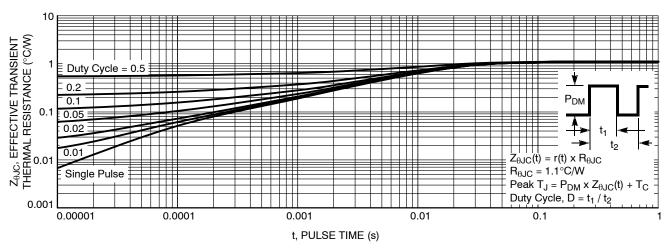


Figure 13. Junction-to-Case Transient Thermal Response Curve



0.10

0.10

SIDE VIEW

DFN5 5x6, 1.27P (SO-8FL) CASE 488AA ISSUE N

DATE 25 JUN 2018

NOTES:

BURRS

- DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE

	MILLIMETERS			
DIM	MIN	NOM	MAX	
Α	0.90	1.00	1.10	
A1	0.00		0.05	
b	0.33	0.41	0.51	
С	0.23	0.28	0.33	
D	5.00	5.15	5.30	
D1	4.70	4.90	5.10	
D2	3.80	4.00	4.20	
E	6.00	6.15	6.30	
E1	5.70	5.90	6.10	
E2	3.45	3.65	3.85	
е	1.27 BSC			
G	0.51	0.575	0.71	
K	1.20	1.35	1.50	
L	0.51	0.575	0.71	
L1	0.125 REF			
M	3.00	3.40	3.80	
A	0 0		12 °	

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code

= Assembly Location Α

Υ = Year W = Work Week ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.





DETAIL A

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)		PAGE 1 OF 1	

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