NTTFS1D2N02P1E

MOSFET – Power, Single N-Channel, Power33
25 V, 1.0 mΩ, 180 A

Features
- Small Footprint for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications
- DC–DC Converters
- Power Load Switch
- Notebook Battery Management

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain–to–Source Voltage			V_{DSS}	25	V
Gate–to–Source Voltage			V_{GS}	+16/–12	V
Continuous Drain Current $R_{\theta JC}$ (Note 3)	Steady State	T_C = 25°C	I_D	180	A
		T_C = 85°C		130	
Power Dissipation $R_{\theta JC}$ (Note 3)		T_C = 25°C	P_D	52	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	T_A = 25°C	I_D	41	A
		T_A = 85°C		29	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		T_A = 25°C	P_D	2.7	W
Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)	Steady State	T_A = 25°C	I_D	23	A
		T_A = 85°C		16	
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)		T_A = 25°C	P_D	0.82	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	195	A
Single Pulse Drain–to–Source Avalanche Energy ($I_{L(pk)}$ = 63.7 A) (Note 4)			E_{AS}	202	mJ
Operating Junction and Storage Temperature Range			T_J, T_{stg}	–55 to +150	°C
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface–mounted on FR4 board using a 1 in^2 pad size, 2 oz Cu pad.
2. Surface–mounted on FR4 board using minimum pad size, 2 oz Cu pad.
3. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro–mechanical application board design. $R_{\theta CA}$ is determined by the user's board design.
4. 100% UIS tested at L = 0.1 mH, I_{AV} = 40 A.

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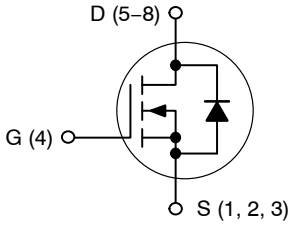
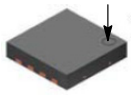
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
25 V	1.0 mΩ @ 10 V	180 A
	1.2 mΩ @ 4.5 V	

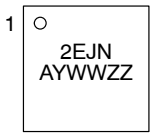
NMOS





PQFN8 (Power33) CASE 483AW

MARKING DIAGRAM



2EJN	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
ZZ	= Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Case − Steady State (Note 1)	$R_{\theta JC}$	2.4	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	47	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	152	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA		25			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 1 mA, ref to 25°C			16		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 20 V	T_J = 25°C			10	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = +16/−12 V				±100	±nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 934 μA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 934 μA, ref to 25°C			−4.4		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 38 A		0.86	1.0	mΩ
		V_{GS} = 4.5 V	I_D = 35 A		1.05	1.2	
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 38 A			224		S
Gate Resistance	R_G	T_A = 25°C			0.5		Ω
CHARGES & CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 13 V			4040		pF
Output Capacitance	C_{OSS}				1100		
Reverse Capacitance	C_{RSS}				68		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 13 V; I_D = 38 A			24		nC
Threshold Gate Charge	$Q_{G(TH)}$				5.2		
Gate−to−Drain Charge	Q_{GD}				3.9		
Gate−to−Source Charge	Q_{GS}				9.8		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 13 V; I_D = 38 A			54		
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DD} = 13 V, I_D = 38 A, R_G = 6 Ω			24.6		ns
Rise Time	t_r				13		
Turn−Off Delay Time	$t_{d(OFF)}$				38.5		
Fall Time	t_f				9.8		
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DD} = 13 V, I_D = 38 A, R_G = 6 Ω			14.8		ns
Rise Time	t_r				4.2		
Turn−Off Delay Time	$t_{d(OFF)}$				59		
Fall Time	t_f				7.9		
SOURCE−TO−DRAIN DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 38 A	T_J = 25°C		0.78	1.2	V
			T_J = 125°C		0.65		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI/dt = 100 A/μs, I_S = 38 A			38		ns
Reverse Recovery Charge	Q_{RR}				25		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

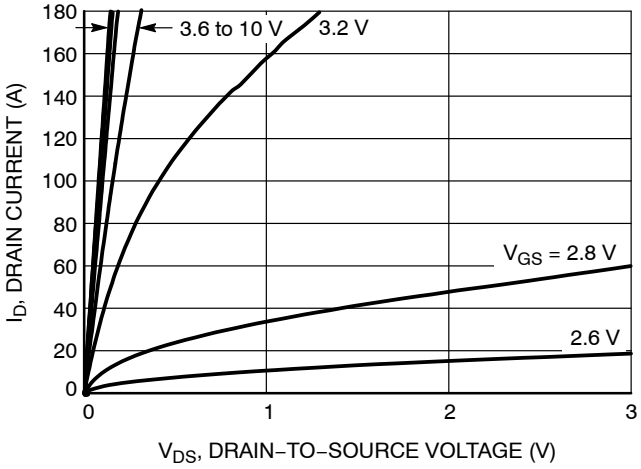


Figure 1. On−Region Characteristics

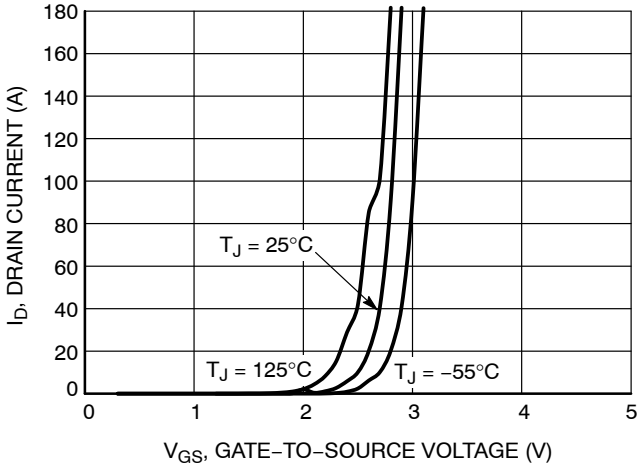


Figure 2. Transfer Characteristics

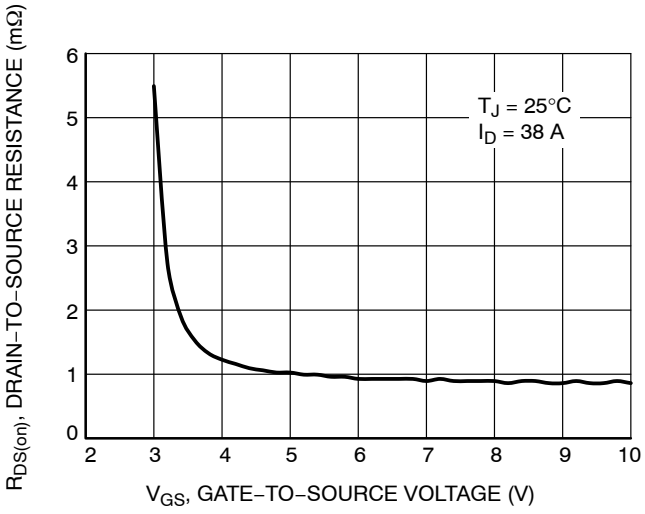


Figure 3. On−Resistance vs. Gate−to−Source Voltage

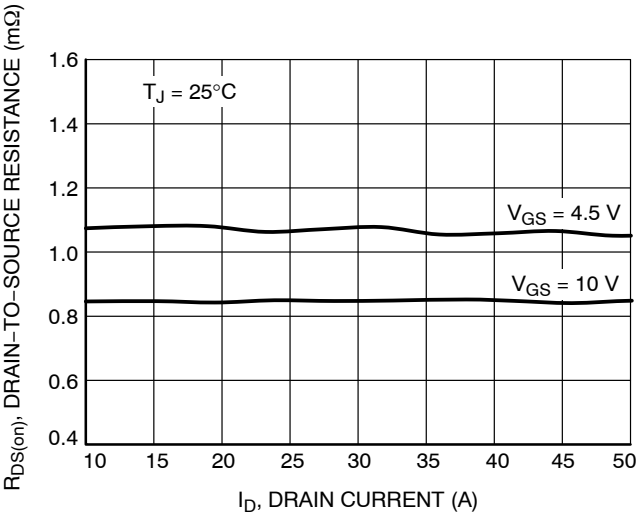


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

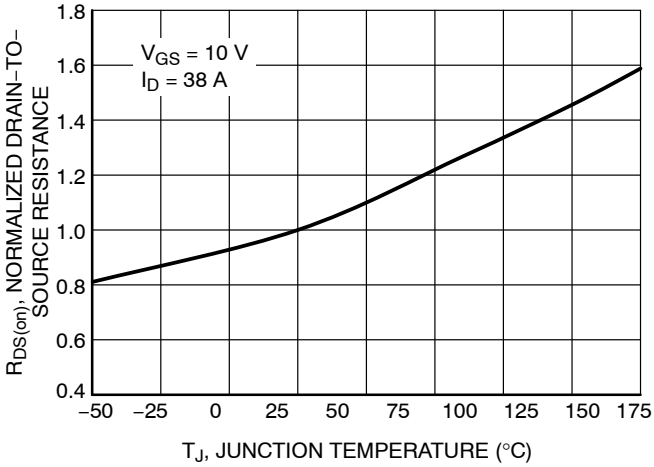


Figure 5. On−Resistance Variation with Temperature

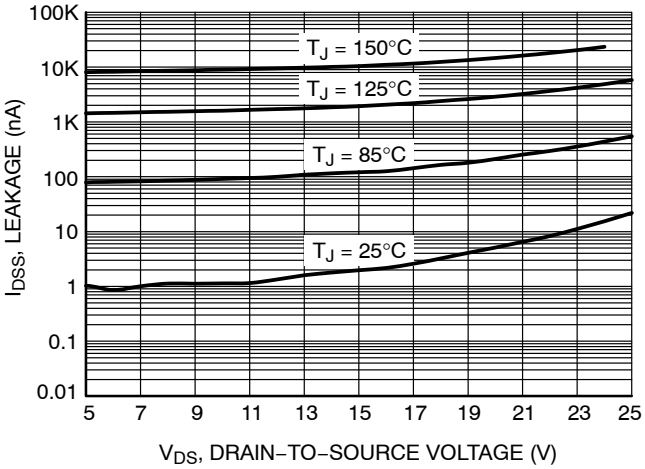


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

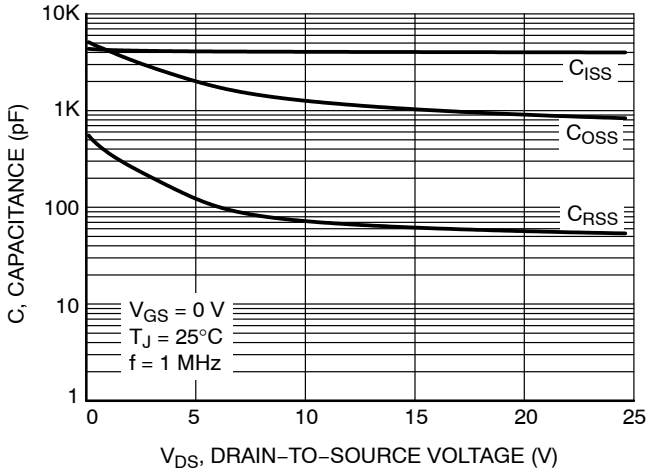


Figure 7. Capacitance Variation

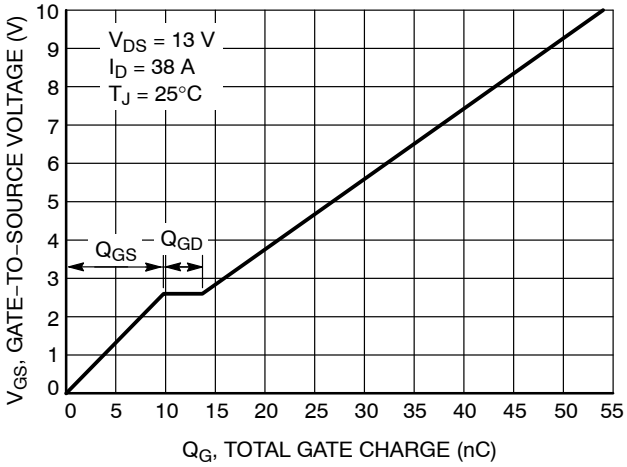


Figure 8. Gate−to−Source vs. Total Charge

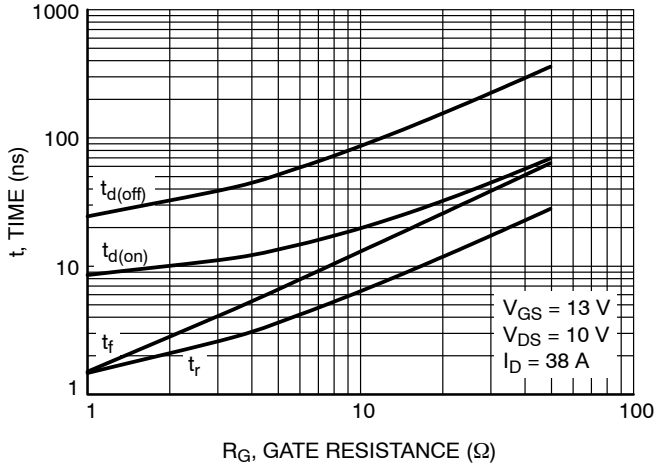


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

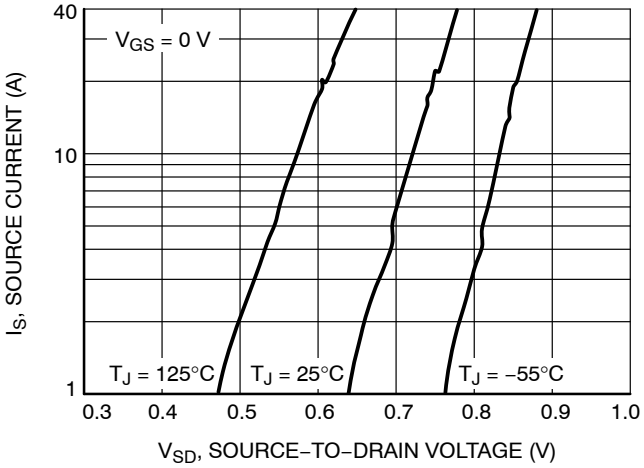


Figure 10. Diode Forward Voltage vs. Current

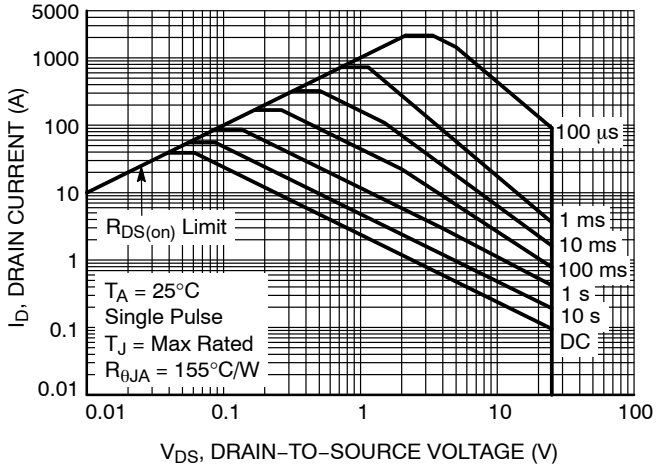


Figure 11. Maximum Rated Forward Biased Safe Operating Area

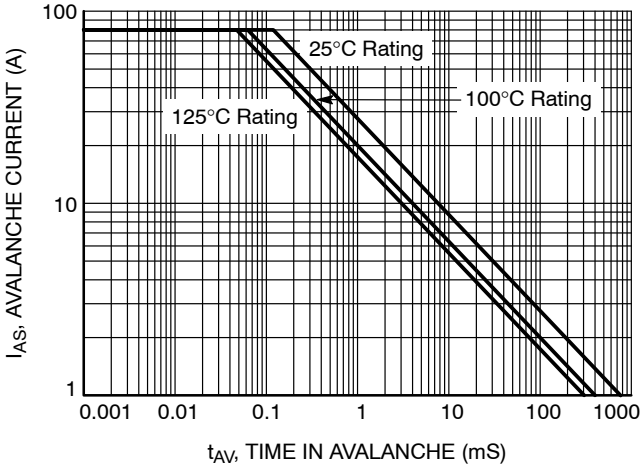


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

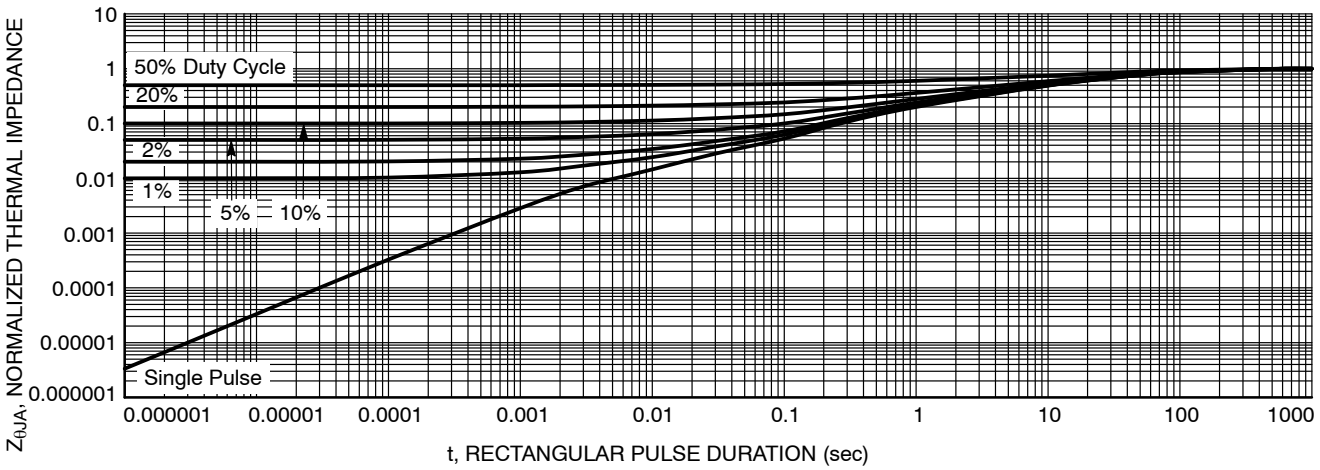


Figure 13. transient Thermal impedance

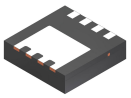
ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTTFS1D2N02P1E	2EJN	Power33 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



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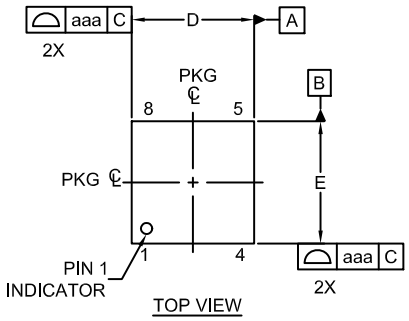
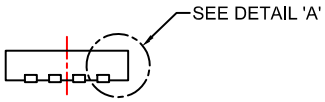
CASE 483AW
ISSUE A

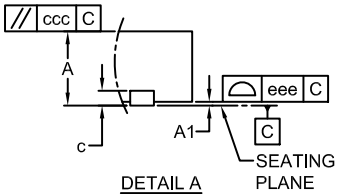
DATE 10 SEP 2019



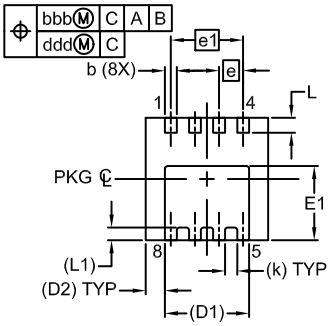
TOP VIEW



FRONT VIEW

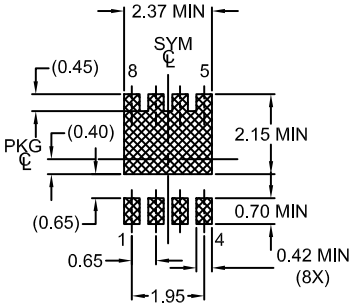


DETAIL A
SCALE: 2x



BOTTOM VIEW

LAND PATTERN RECOMMENDATION*



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	-	0.05
b	0.27	0.32	0.37
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.27 REF		
D2	0.52 REF		
E	3.20	3.30	3.40
E1	1.85	1.95	2.05
e	0.65 BSC		
e1	1.95 BSC		
k	0.33 REF		
L	0.30	0.40	0.50
L1	0.34 REF		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFN8 3.3X3.3, 0.65P**	**PAGE 1 OF 1**

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