

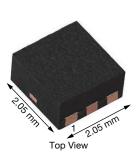
www.vishay.com

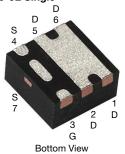
Vishay Siliconix

# P-Channel 150 V (D-S) MOSFET

PRODUCT SUMMARY									
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) MAX.	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)						
-150	2.6 at V <sub>GS</sub> = -10 V	-1.6 <sup>a</sup>	4.2 nC						
	2.7 at V <sub>GS</sub> = -6 V	-1.6 <sup>a</sup>	4.2110						

### PowerPAK® SC-70-6L Single





Marking Code: B4 **Ordering Information:** 

SiA485DJ-T1-GE3 (Lead (Pb)-free and halogen-free)

#### **FEATURES**

- TrenchFET® power MOSFET
- Thermally enhanced PowerPAK® SC-70 package
  - Small footprint area
  - Low on-resistance
- 100 % R<sub>a</sub> and UIS tested

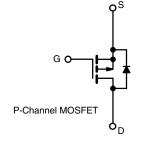


### **APPLICATIONS**

- Active clamp switch
- · Load switch



RoHS



ABSOLUTE MAXIMUM RATINGS (	$T_A = 25  ^{\circ}C$ , unless	otherwise noted	(k	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V <sub>DS</sub>	-150	V
Gate-Source Voltage		V <sub>GS</sub>	± 20	v
	T <sub>C</sub> = 25 °C		-1.6	
Continuous Drain Current /T 150 °C\	T <sub>C</sub> = 70 °C	,	-1.3	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	-0.7 b, c	
	T <sub>A</sub> = 70 °C		-0.57 <sup>b, c</sup>	
Pulsed Drain Current (t = 100 μs)	<u>.</u>	I <sub>DM</sub>	-2	A
Continuous Courses Drain Diada Current	T <sub>C</sub> = 25 °C		-1.6	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	-1.6 <sup>b, c</sup>	
Avalanche Current	l 0.1 mll	I <sub>AS</sub>	-1.5	
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	0.1	mJ
	T <sub>C</sub> = 25 °C		15.6	
Maximum Dawar Dissination	T <sub>C</sub> = 70 °C		10	W
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.9 b, c	VV
	T <sub>A</sub> = 70 °C		1.8 b, c	
Operating Junction and Storage Temperature R	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering Recommendations (Peak Temperatur	e) <sup>d, e</sup>		260	

THERMAL RESISTANCE RATINGS									
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT				
Maximum Junction-to-Ambient b, f	t ≤ 5 s	R <sub>thJA</sub>	32	43	°C/W				
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	6	8	C/VV				

- a.  $T_C = 25$  °C.
- b. Surface mounted on 1" x 1" FR4 board.
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 80 °C/W.



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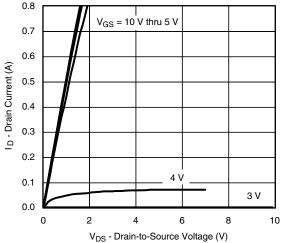
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ , $I_D = -250 \mu A$	-150		-	v
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-2.5	-	-4.5	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
Zoro Coto Voltago Prain Current	ı	V <sub>DS</sub> = -150 V, V <sub>GS</sub> = 0 V	-	-	-1	μΑ
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -150 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	-10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \le -5 \text{ V}, V_{GS} = -10 \text{ V}$	-0.8	-	-	Α
Dunin Course On Chata Desintance 3		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -0.5 A	-	2.1	2.6	Ω
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -6 V, I <sub>D</sub> = -0.5 A	-	2.2	2.7	
Forward Transconductance a	9 <sub>fs</sub>	$V_{DS} = -10 \text{ V}, I_D = -0.5 \text{ A}$	-	1.5	-	S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>		-	155	-	pF
Output Capacitance	C <sub>oss</sub>	$V_{DS} = -75 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	8	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	5.5	-	
Total Gate Charge	Qg		-	4.2	6.3	nC
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = -75 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -0.5 \text{ A}$	-	0.9	-	
Gate-Drain Charge	$Q_{gd}$		-	1.3	-	
Gate Resistance	Rg	f = 1 MHz	2	10	20	Ω
Turn-On Delay Time	t <sub>d(on)</sub>		-	5	10	- ns
Rise Time	t <sub>r</sub>	$V_{DD} = -75 \text{ V}, R_{L} = 75 \Omega$	-	20	40	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong -1 \stackrel{-}{A}, V_{GEN} = -10 \stackrel{-}{0} V, R_g = 1 \Omega$	-	10	20	
Fall Time	t <sub>f</sub>		-	20	40	
Drain-Source Body Diode Characteristi	cs					
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-		-1.6	_
Pulse Diode Forward Current	I <sub>SM</sub>		-		-2	A
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = -0.5 A, V <sub>GS</sub> = 0 V	-	-0.8	-1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>		-	40	80	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	-	65	130	nC
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = -1 \text{ A, dI/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 ^{\circ}\text{C}$	-	28	-	ns
Reverse Recovery Rise Time	t <sub>b</sub>		-	12	-	

#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

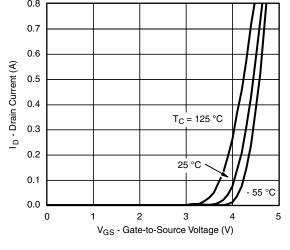
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



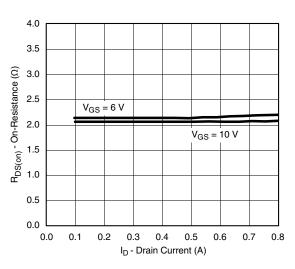


**Output Characteristics** 

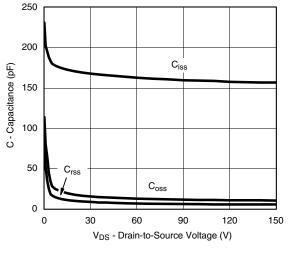




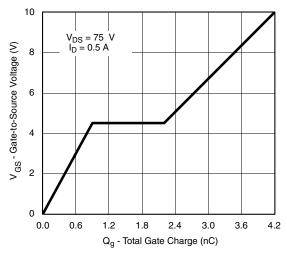
#### **Transfer Characteristics**



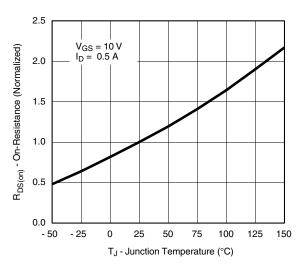
On-Resistance vs. Drain Current and Gate Voltage



#### Capacitance

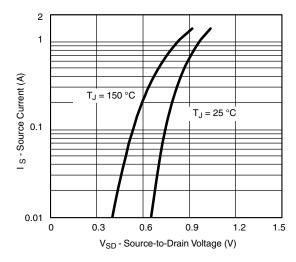




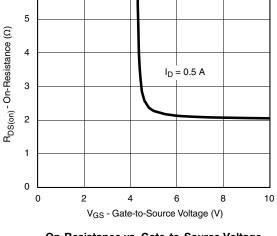


On-Resistance vs. Junction Temperature



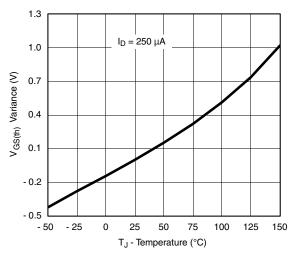


#### Source-Drain Diode Forward Voltage

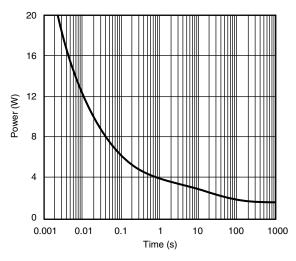


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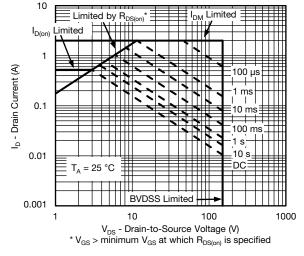
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 

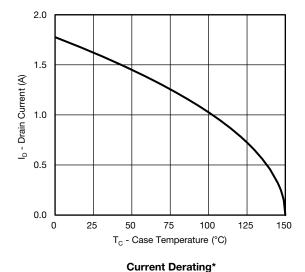


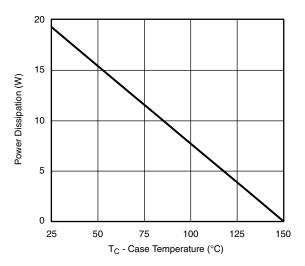
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient



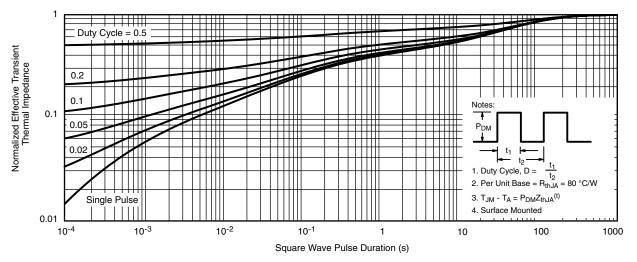




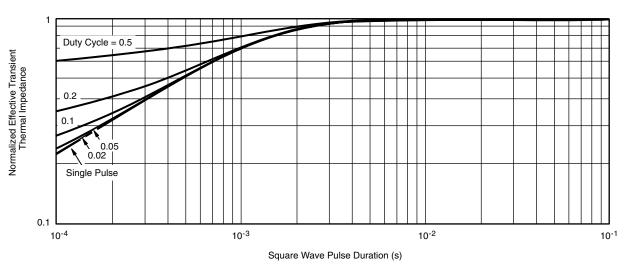
**Power Derating** 

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J (max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





#### Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

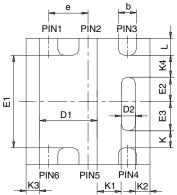
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg262988">www.vishay.com/ppg262988</a>.





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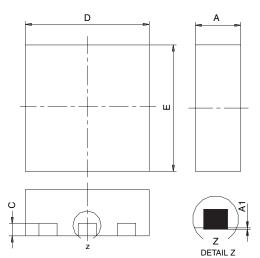
# PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
  Package outline exclusive of mold flash and metal burr
  Package outline inclusive of plating

		SINGLE PAD						DUAL PAD					
DIM	MILLIMETERS			INCHES			MILLIMETERS			INCHES			
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032	
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002	
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015	
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010	
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028	
D2	0.135	0.235	0.335	0.005	0.009	0.013							
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041	
E2	0.345	0.395	0.445	0.014	0.016	0.018							
E3	0.425	0.475	0.525	0.017	0.019	0.021							
е		0.65 BSC			0.026 BSC	;	0.65 BSC			0.026 BSC			
K		0.275 TYP 0.011 TYP		0.275 TYP			0.011 TYP						
K1		0.400 TYP 0.016 TYP		0.320 TYP			0.013 TYP						
K2		0.240 TYP 0.009 TYP		0.252 TYP			0.010 TYP						
К3		0.225 TYP 0.009 TYP				•		•	•				
K4		0.355 TYP		0.014 TYP									
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015	
T							0.05	0.10	0.15	0.002	0.004	0.006	

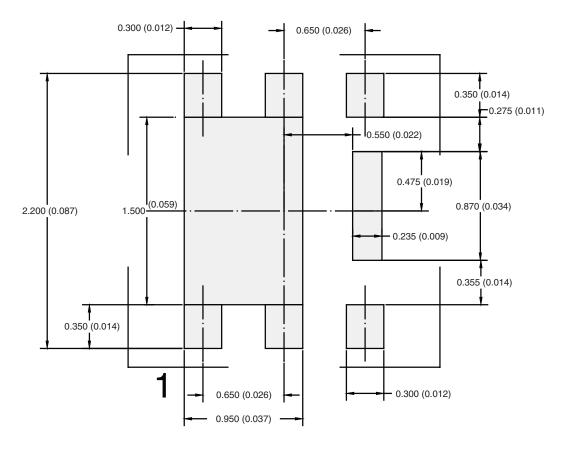
ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5934

06-Aug-07



# RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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Vishay

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