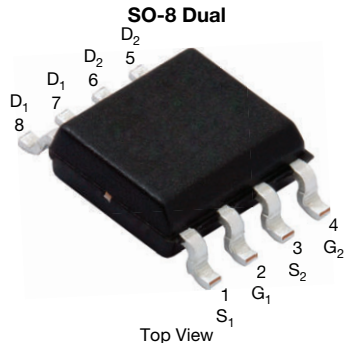


Complementary (N- and P-Channel) MOSFET



FEATURES

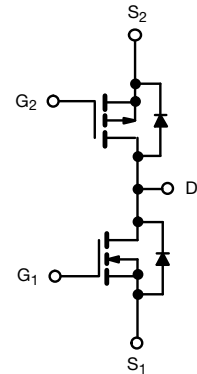
- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Level shift
- Load switch



PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
V _{DS} (V)	30	-8
R _{DS(on)} (Ω) at V _{GS} = ± 10 V	0.017	0.027
R _{DS(on)} (Ω) at V _{GS} = ± 4.5 V	0.020	0.037
Q _g typ. (nC)	7.9	16.5
I _D (A) ^a	12	-8
Configuration	N- and p-pair	

ORDERING INFORMATION

Package	SO-8
Lead (Pb)-free and halogen-free	Si4501BDY-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT	
Drain-source voltage	V _{DS}	30	-8	V	
Gate-source voltage	V _{GS}	± 20	± 8		
Continuous drain current (T _J = 150 °C)	I _D	T _C = 25 °C	12	-8	A
		T _C = 70 °C	9.5	-6.4	
		T _A = 25 °C	9 ^{b, c}	-6.4 ^{b, c}	
		T _A = 70 °C	7.2 ^{b, c}	-5.1 ^{b, c}	
Pulsed drain current (10 μs pulse width)	I _{DM}	40	-40	A	
Source-drain current diode current	I _S	T _C = 25 °C	4		-2.8
		T _A = 25 °C	2.2 ^{b, c}	-1.8 ^{b, c}	
Pulsed source-drain current	I _{SM}	40	-40	A	
Single pulse avalanche current	I _{AS}	5	-5		
Single pulse avalanche energy	E _{AS}	1.25	1.25	mJ	
Maximum power dissipation	P _D	T _C = 25 °C	4.5	3.1	W
		T _C = 70 °C	2.8	2	
		T _A = 25 °C	2.5 ^{b, c}	2 ^{b, c}	
		T _A = 70 °C	1.6 ^{b, c}	1.28 ^{b, c}	
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150		°C	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	N-CHANNEL		P-CHANNEL		UNIT
		TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient ^{b, d}	R _{thJA}	40	50	52	62.5	°C/W
Maximum junction-to-foot (Drain)	R _{thJF}	22	28	32	40	

Notes

- Based on T_C = 25 °C
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- Maximum under steady state conditions is 95 °C/W (N-Channel) and 110 °C/W (P-Channel)



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP. ^a	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	30	-	-	V
		V _{GS} = 0 V, I _D = -250 μA	P-Ch	-8	-	-	
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch	-	34	-	mV/°C
		I _D = -250 μA	P-Ch	-	-3	-	
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch	-	-4.5	-	mV/°C
		I _D = -250 μA	P-Ch	-	2.6	-	
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.8	-	2	V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-0.45	-	-0.9	
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	N-Ch	-	-	± 100	nA
		V _{DS} = 0 V, V _{GS} = ± 8 V	P-Ch	-	-	± 100	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	N-Ch	-	-	1	μA
		V _{DS} = -8 V, V _{GS} = 0 V	P-Ch	-	-	-1	
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch	-	-	5	
		V _{DS} = -8 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch	-	-	-5	
On-state drain current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N-Ch	20	-	-	A
		V _{DS} = -5 V, V _{GS} = -4.5 V	P-Ch	-20	-	-	
Drain-source on-state resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A	N-Ch	-	0.0135	0.0170	Ω
		V _{GS} = -4.5 V, I _D = -6 A	P-Ch	-	0.0210	0.0270	
		V _{GS} = 4.5 V, I _D = 7 A	N-Ch	-	0.0160	0.0200	
		V _{GS} = -2.5 V, I _D = -5 A	P-Ch	-	0.0290	0.0370	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 10 A	N-Ch	-	29	-	S
		V _{DS} = -15 V, I _D = -6 A	P-Ch	-	24	-	
Dynamic ^a							
Input capacitance	C _{iss}	N-Channel V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz P-Channel V _{DS} = -4 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	-	805	-	pF
Output capacitance	C _{oss}		N-Ch	-	170	-	
			P-Ch	-	660	-	
Reverse transfer capacitance	C _{rss}		N-Ch	-	80	-	
		P-Ch	-	630	-		
Total gate charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A	N-Ch	-	16.5	25	nC
		V _{DS} = -4 V, V _{GS} = -8 V, I _D = -6 A	P-Ch	-	27.5	42	
Gate-source charge	Q _{gs}	N-Channel V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 10 A P-Channel V _{DS} = -4 V, V _{GS} = -4.5 V, I _D = -6 A	N-Ch	-	7.9	12	
			P-Ch	-	16.5	25	
Gate-drain charge	Q _{gd}	N-Ch	-	2.2	-	nC	
		P-Ch	-	2.2	-		
Gate resistance	R _g	f = 1 MHz	N-Ch	0.3	1.1	2.2	Ω
			P-Ch	0.9	4.2	8.4	



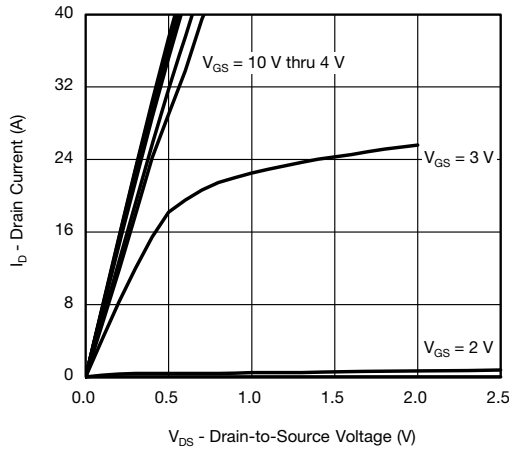
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP. ^a	MAX.	UNIT	
Dynamic ^a							
Turn-on delay time	t _{d(on)}	N-Channel V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch	-	7	14	ns
			P-Ch	-	6	12	
Rise time	t _r		N-Ch	-	11	22	
			P-Ch	-	12	24	
Turn-off delay time	t _{d(off)}	P-Channel V _{DD} = -4 V, R _L = 0.8 Ω I _D ≅ -5 A, V _{GEN} = -10 V, R _g = 1 Ω	N-Ch	-	15	30	
			P-Ch	-	35	65	
Fall time	t _f		N-Ch	-	8	16	
			P-Ch	-	9	18	
Turn-on delay time	t _{d(on)}	N-Channel V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	N-Ch	-	16	30	
			P-Ch	-	22	40	
Rise time	t _r		N-Ch	-	55	100	
			P-Ch	-	18	35	
Turn-off delay time	t _{d(off)}	P-Channel V _{DD} = -4 V, R _L = 0.8 Ω I _D ≅ -5 A, V _{GEN} = -4.5 V, R _g = 1 Ω	N-Ch	-	22	40	
			P-Ch	-	34	65	
Fall time	t _f		N-Ch	-	10	20	
			P-Ch	-	14	28	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	T _C = 25 °C	N-Ch	-	-	4	A
			P-Ch	-	-	-2.8	
Pulse diode forward current ^a	I _{SM}		N-Ch	-	-	40	A
			P-Ch	-	-	-40	
Body diode voltage	V _{SD}	I _S = 2 A	N-Ch	-	0.72	1.1	V
		I _S = -2 A	P-Ch	-	-0.71	-1.1	
Body diode reverse recovery time	t _{rr}	N-Channel I _F = 1.8 A, di/dt = 100 A/μs, T _J = 25 °C	N-Ch	-	14	28	ns
			P-Ch	-	49	98	
Body diode reverse recovery charge	Q _{rr}	P-Channel I _F = -1.8 A, di/dt = -100 A/μs, T _J = 25 °C	N-Ch	-	5.5	11	nC
			P-Ch	-	47	94	
Reverse recovery fall time	t _a		N-Ch	-	7.5	-	ns
			P-Ch	-	26	-	
Reverse recovery rise time	t _b		N-Ch	-	6.5	-	
			P-Ch	-	23	-	

Notes

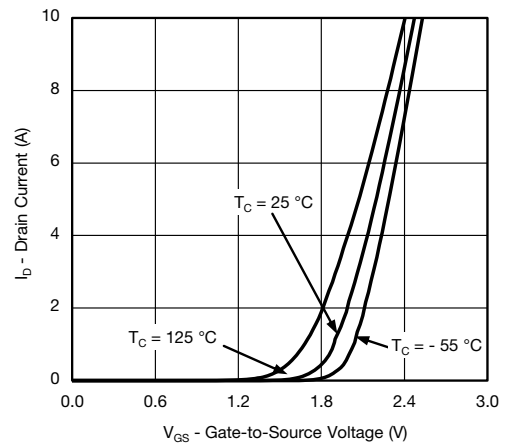
- a. Guaranteed by design, not subject to production testing
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

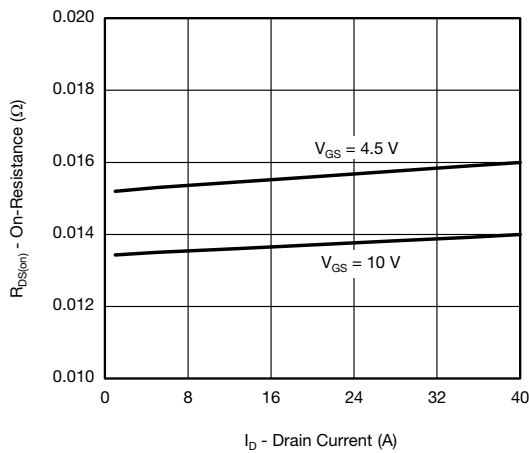
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



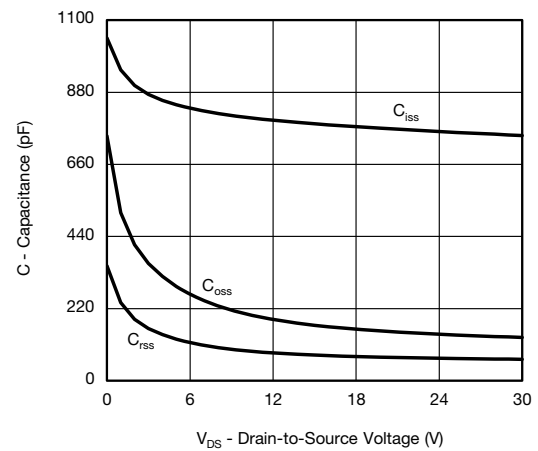
Output Characteristics



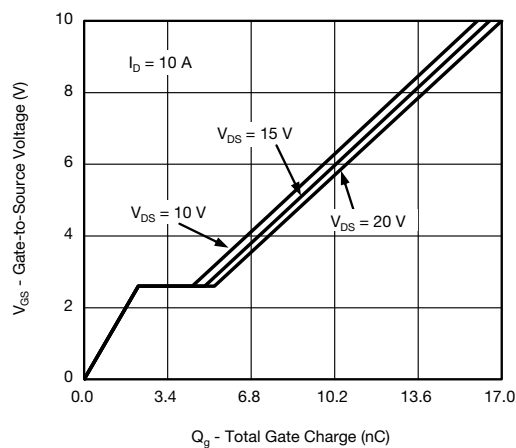
Transfer Characteristics



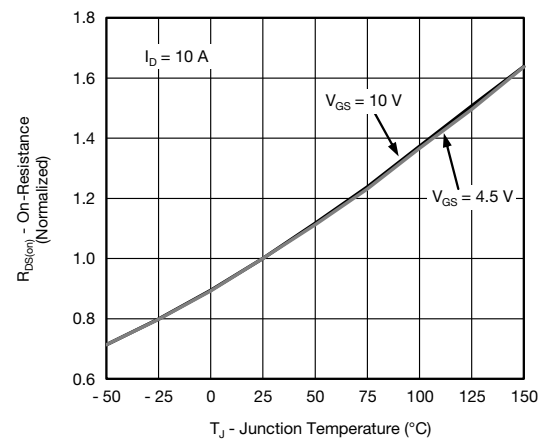
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



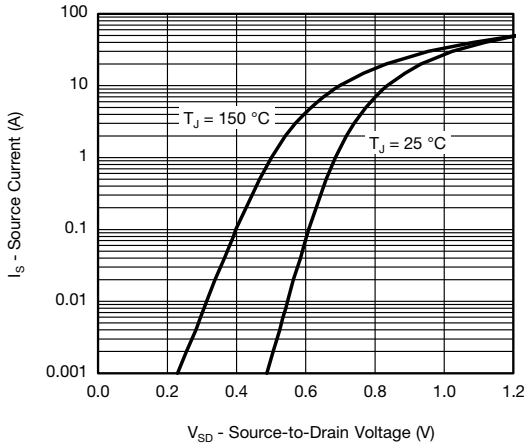
Gate Charge



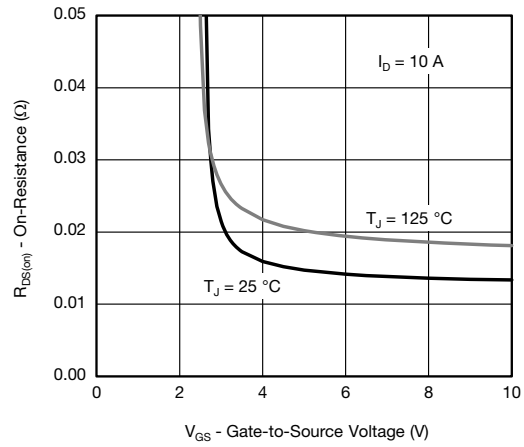
On-Resistance vs. Junction Temperature



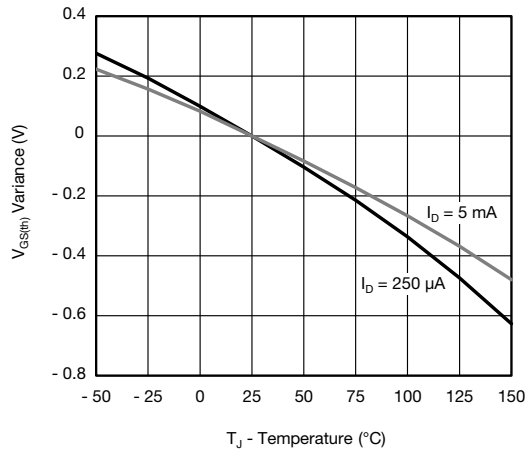
N-CHANNEL TYPICAL CHARACTERISTICS(25 °C, unless otherwise noted)



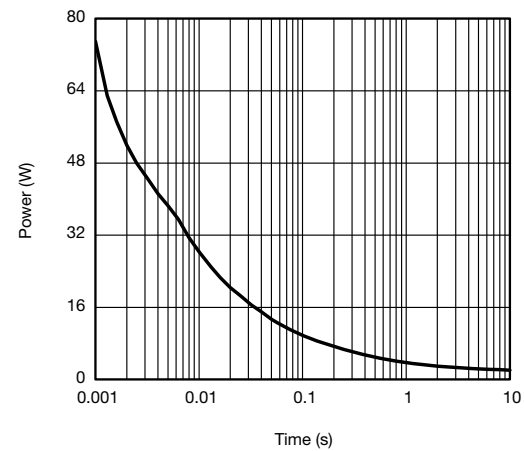
Source-Drain Diode Forward Voltage



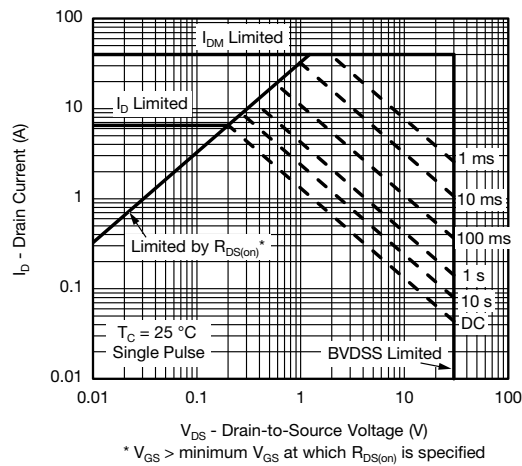
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



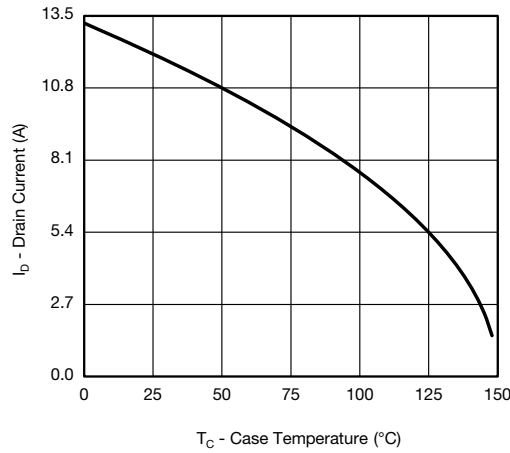
Single Pulse Power, Junction-to-Ambient



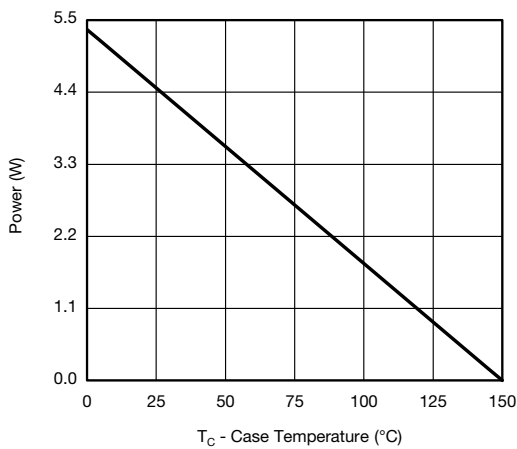
Safe Operating Area, Junction-to-Ambient



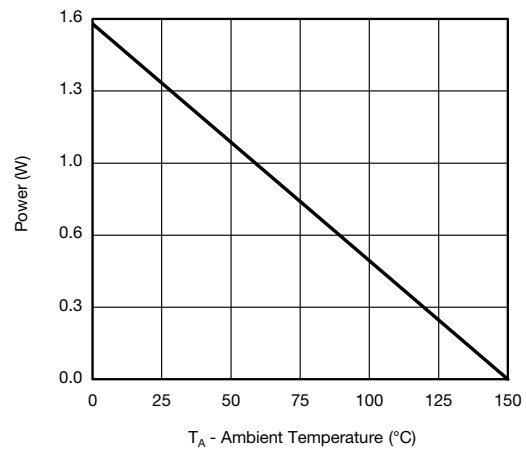
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power Derating, Junction-to-Foot



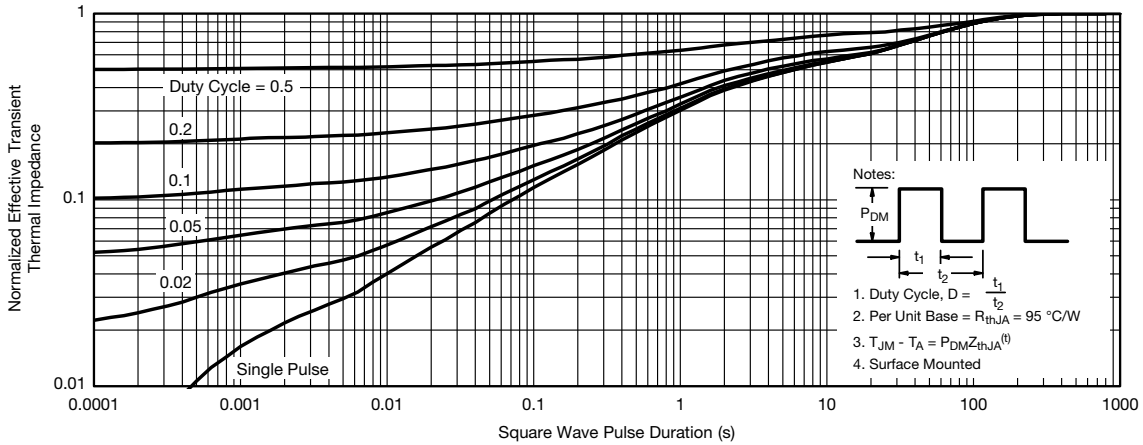
Power Derating, Junction-to-Ambient

Note

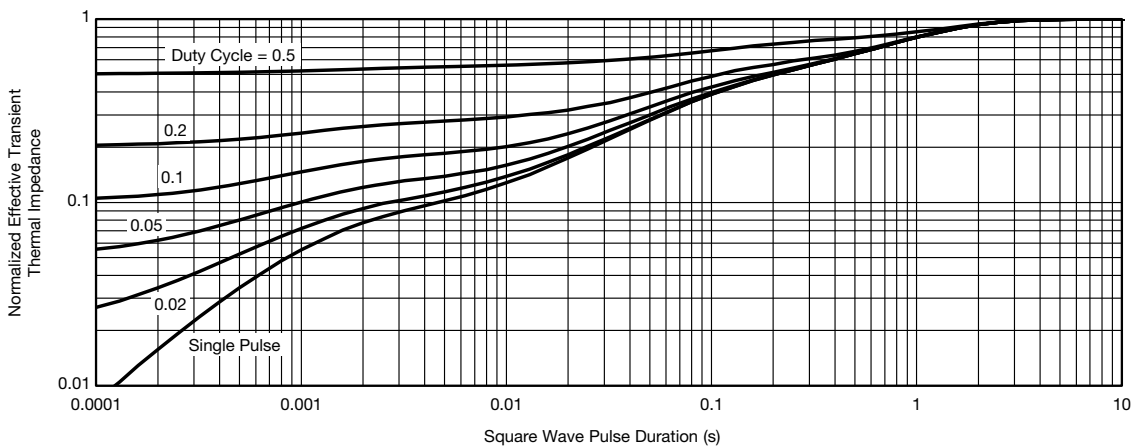
- a. The power dissipation P_D is based on T_J max = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



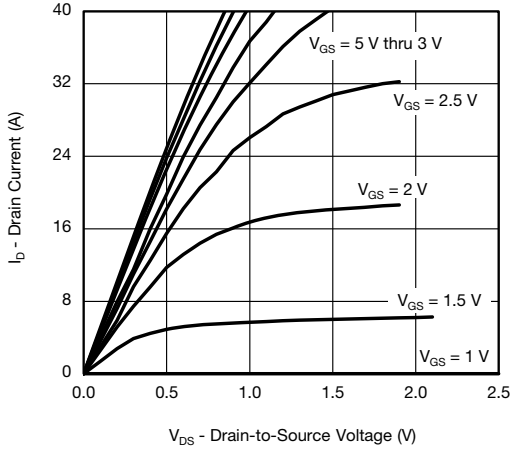
Normalized Thermal Transient Impedance, Junction-to-Ambient



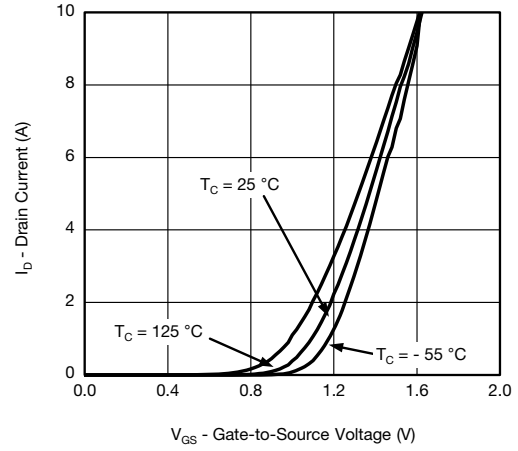
Normalized Thermal Transient Impedance, Junction-to-Foot



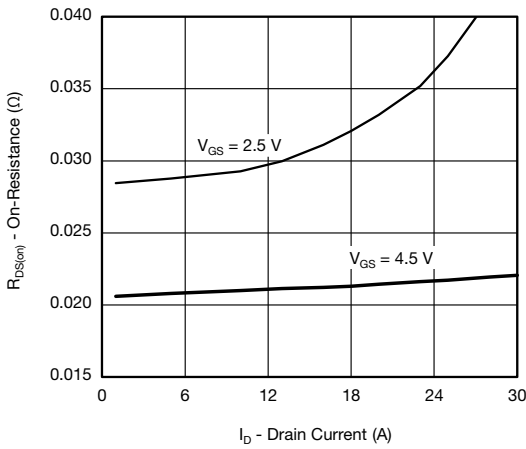
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



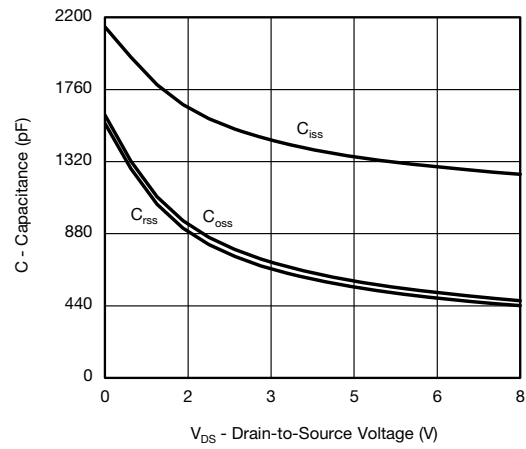
Output Characteristics



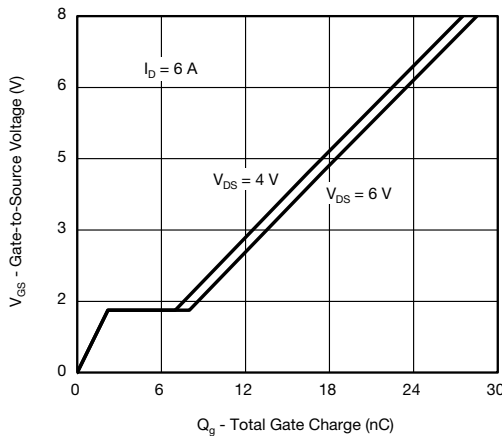
Transfer Characteristics



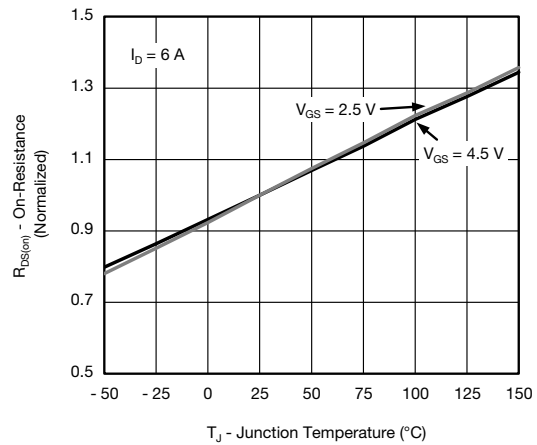
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



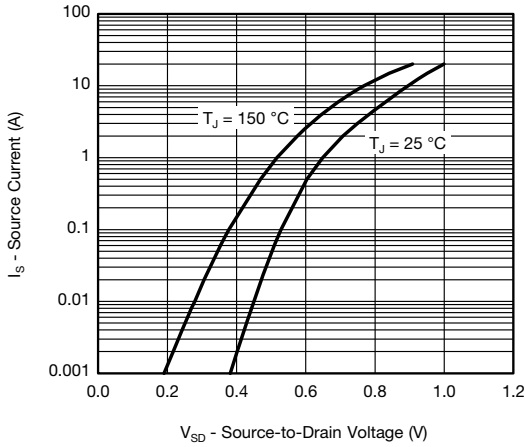
Gate Charge



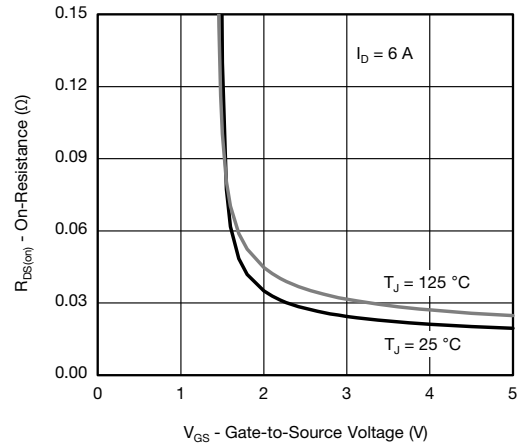
On-Resistance vs. Junction Temperature



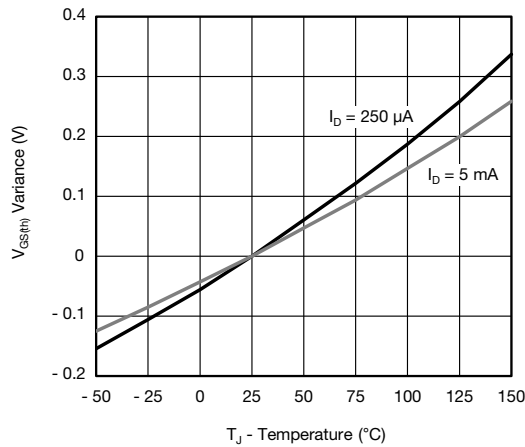
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



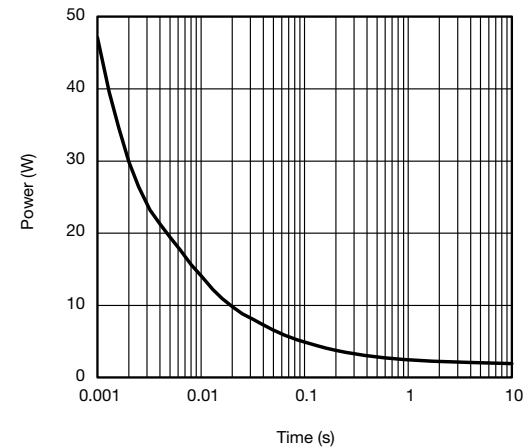
Source-Drain Diode Forward Voltage



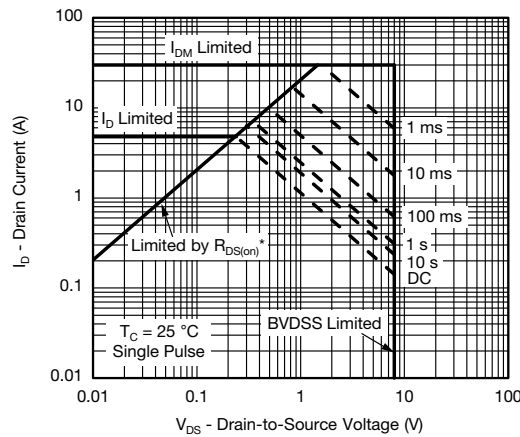
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

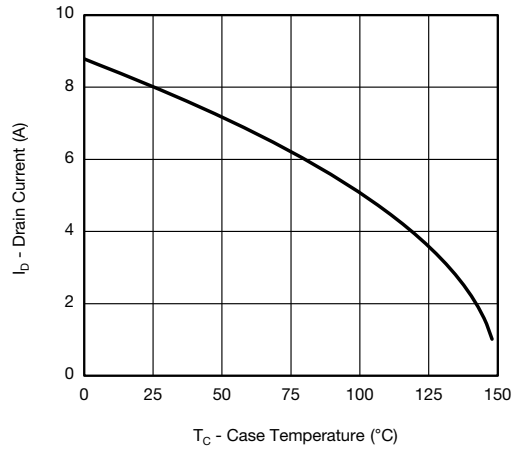


Single Pulse Power, Junction-to-Ambient

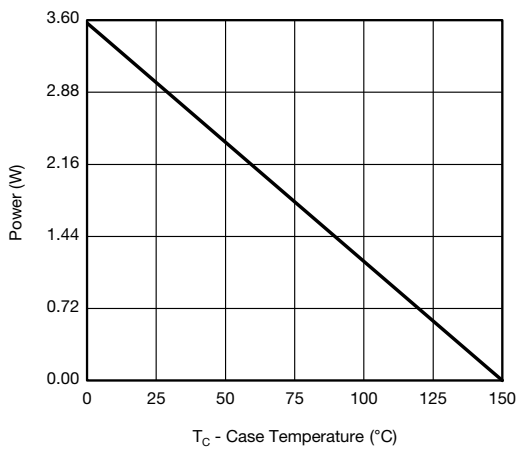


Safe Operating Area, Junction-to-Ambient
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

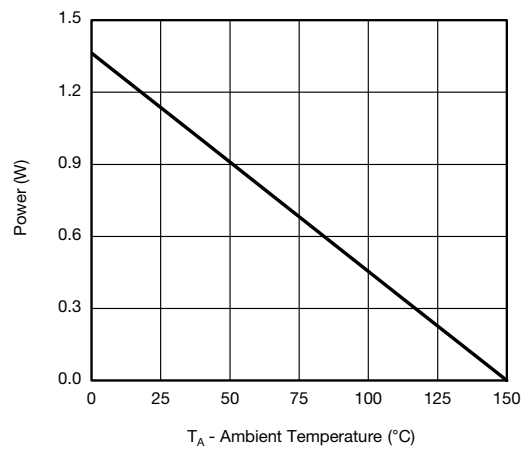
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power Derating, Junction-to-Foot



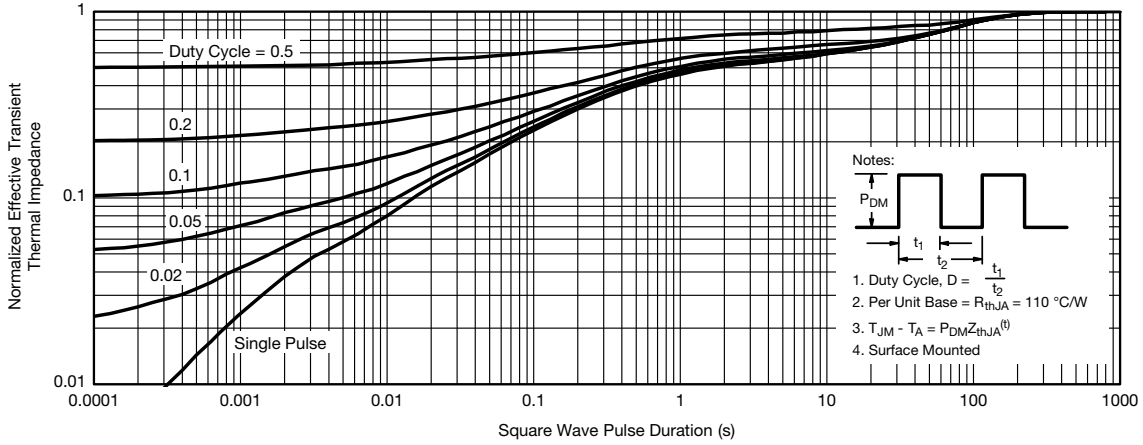
Power Derating, Junction-to-Ambient

Note

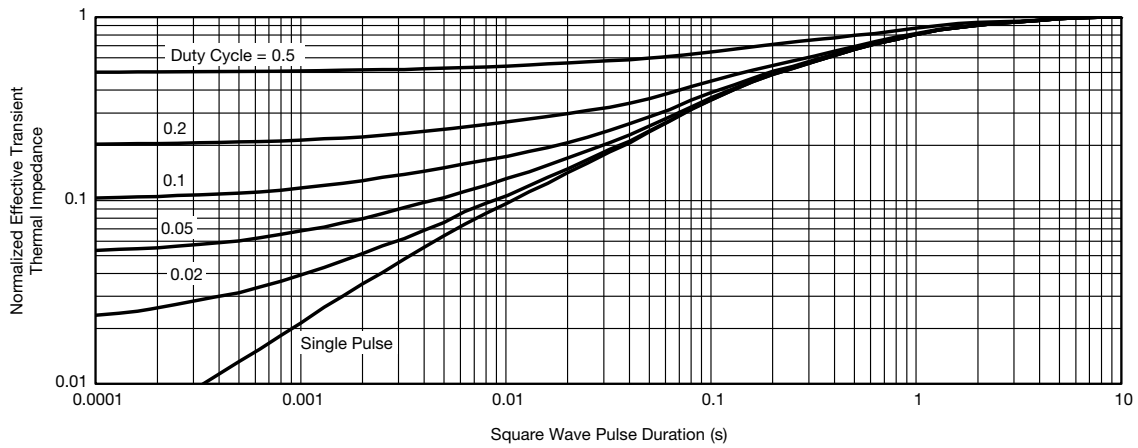
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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