SC8837C
1A Low-Voltage H-Bridge Driver

1 Features

- H-Bridge Motor Driver
  - Drives a DC Motors or Other Loads
  - Low-MOSFET ON-Resistance: HS + LS 0.85Ω
- 1-A Maximum Drive Current
- Separate Motor and Logic-Supply Pins:
  - 0-V to 10-V Motor-Operating Supply-Voltage
  - 1.6-V to 7-V Logic Supply-Voltage
- Separate Logic and Motor Power Supply Pins
- Standard PWM Interface (IN1/IN2)
- Low-Power Sleep Mode With 120-nA Maximum Supply Current
  - nSLEEP pin
- Small Package and Footprint
  - 8 DFN(With Thermal Pad)
  - 2.00mm x 2.00mm
- Protection Features
  - VCC Undervoltage Lockout(UVLO)
  - Overcurrent Protection(OCP)
  - Thermal Shutdown(TSD)

2 Applications

- Battery-Powered:
- Cameras
- DSLR Lenses
- Consumer Products
- Toys
- Robotics
- Medical Devices

3 Description

The SC8837C provides an integrated motor driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device has a H-bridge driver, and drives one DC motors, as well as other devices like solenoids. The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the motor winding. An internal charge pump generates gate drive voltages.

The SC8837C supplies up to 1.0-A of output current. The operates on a motor power supply voltage from 0 V to 10 V, and control logic can operate on 1.6-V to 7-V rails.

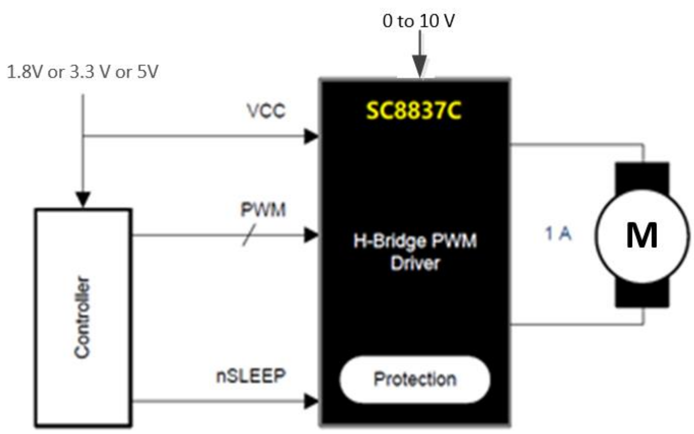
The SC8837C device has a PWM(IN/IN) input interface. Internal shutdown functions are provided for overcurrent protection, short circuit protection, undervoltage lockout, and overtemperature.

The SC8837C is packaged in a 8-pin DFN package.

Device Information

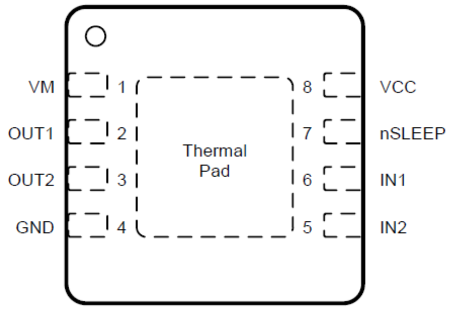
PART NUMBER	PACKAGE	BODY SIZE (NOM)
SC8837C	DFN (8)	2.00 mm × 2.00 mm

Simplified Schematic



4 Pin Configuration and Functions

DFN Package
8-Pin DFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
GND, Thermal pad	4	PWR	Device ground	This pin must be connected to the PCB ground
VM	1	PWR	Motor supply	Bypass to GND with a 0.1uF(minimum) ceramic capacitor
VCC	8	PWR	Device supply	Bypass to GND with a 0.1uF(minimum) ceramic capacitor
CONTROL				
IN1	6	I	Bridge input 1	Logic high sets OUT1 high Internal pulldown resistor
IN2	5	I	Bridge input 2	Logic high sets OUT2 high Internal pulldown resistor
nSLEEP	7	I	Sleep mode input	Logic low : the device enters low-power sleep mode Logic high: the device operates normal mode Internal pulldown resistor
OUTPUT				
OUT1	2	O	Bridge output 1	Connect to motor winding
OUT2	3	O	Bridge output 2	

5 Specifications

5.1 Absolute Maximum Ratings

See[1][2]

	MIN	MAX	UNIT
Power supply voltage, VM	-0.3	11	V
Power supply voltage, VCC	-0.3	7.0	V
Digital input pin voltage	-0.5	VCC	V
Peak motor drive output current	Internally limited		A
T_J Operating junction temperature	-40	150	C°
T_{stg} Storage temperature	-60	150	C°

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS – 001[1]	±4000	V
	Charge-device model (CDM), per JEDEC specification JESD22 – C101[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5. 3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
V_{CC} Device power supply voltage	1.6		7.0	V
V_M Motor power supply voltage	0		10	V
V_{IN} Logic level input voltage	0		V_{CC}	V
I_{OUT} Continuous motor drive output current	0		1.0	A
f_{pwm} Externally applied PWM frequency	0		250	kHz
T_A Operating ambient temperature	-40		85	C°

5.4 Thermal Information

THERMAL METRIC	VALUE	UNIT
R_{JA} Junction-to-ambient thermal resistance	75.6	C°/W
R_{JC} Junction-to-thermal resistance	48.3	C°/W

5.5 Electrical Characteristics

T_A = 25 ℃, V_M = 5 V, V_{CC} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{VM}	VM operating supply current	No PWM, no load		40	100	µA
		50 kHz PWM, no load		0.15	1.0	mA
I_{VCC}	VCC operating supply current	No PWM, no load		100	200	µA
		50 kHz PWM, no load		0.18	1.0	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP=0		30	95	nA
I_{VCCQ}	VCC sleep mode supply current	nSLEEP=0		5	25	nA
V_{UVLO}	VCC undervoltage lockout voltage	V_{CC} rising			1.6	V
		V_{CC} falling			1.5	V
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage				$0.25 \times V_{CC}$	V
V_{IH}	Input high voltage		$0.5 \times V_{CC}$			V
I_{IL}	Input low current	V_{IN}=0	-5		5	µA
I_{IH}	Input high current	V_{IN}=3.3V			50	µA
P_{PD}	Pulldown resistance			100		KΩ
H-BRIDGE FETS						
$R_{DS(ON)}$	HS+LS FET on resistance	V_M=5V, V_{CC}=3.3V,I_O=200mA,T_j=25C°		850		mΩ
I_{OFF}	OFF-state leakage current	V_{OUTx}=0V			±200	nA
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		1.2			A
t_{DEG}	Overcurrent de-glitch time			1		µs
t_{OCR}	Overcurrent protection retry time			1		ms
t_{TSD} (1)	Thermal shutdown temperature	Die temperature	150	160	190	C°

(1) Not tested in production;limits are based on characterization data

5.6 Timing Requirements

T_A = 25 ℃, V_M = 5 V, V_{CC} = 3 V, R_L = 20 Ω

NO.			MIN	MAX	UNIT
1	t_1	Output enable time		300	ns
2	t_2	Output disable time		300	ns
3	t_3	Delay time, INx high to OUTx high		160	ns
4	t_4	Delay time, INx low to OUTx low		160	ns
5	t_5	Output rise time		188	ns
6	t_6	Output fall time		188	ns
–	t_{wake}	Wake time, nSLEEP rising edge to part active		30	µs

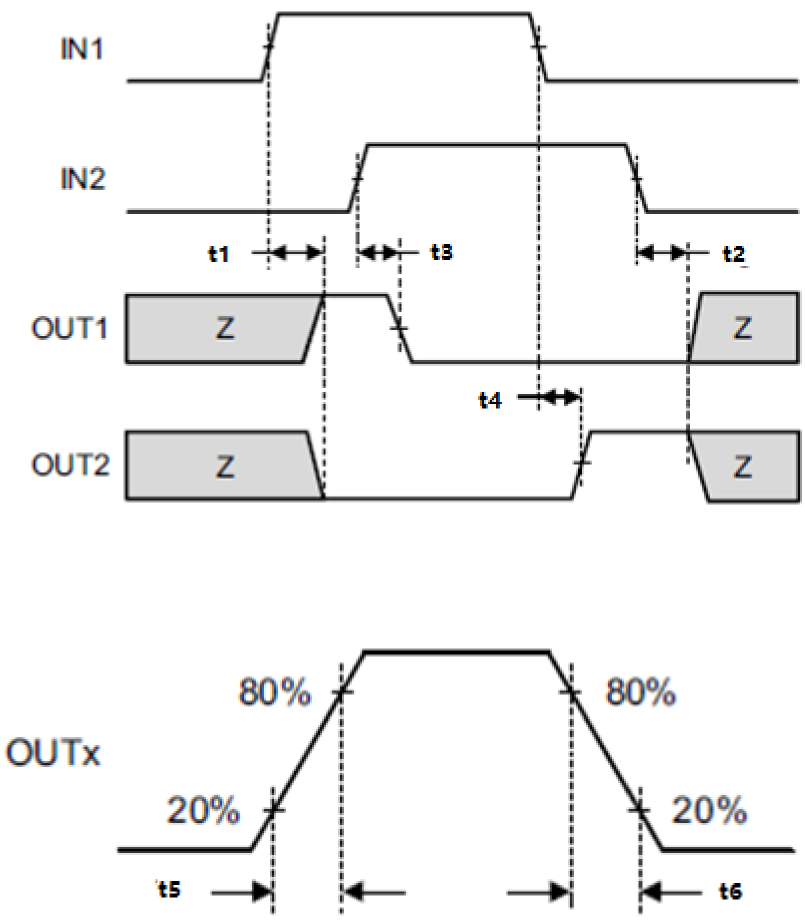


Figure 1. Input and Output Timing for SC8837C

6 Detailed Description

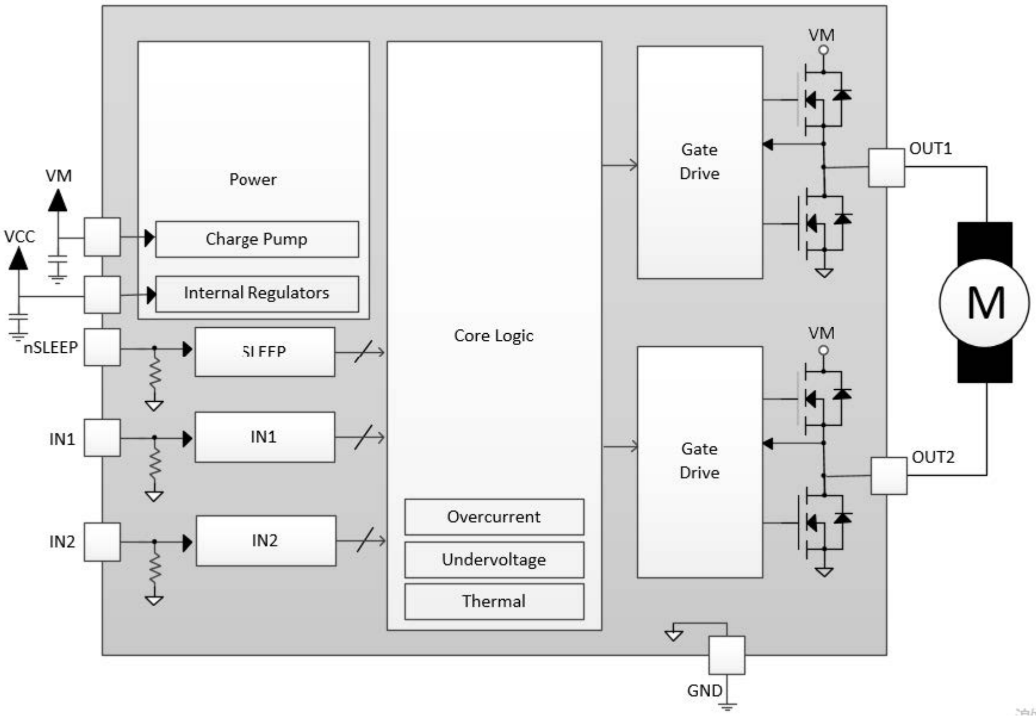
6.1 Overview

The SC8837C device is an H-bridge driver that can drive one DC motor or other devices like solenoids. The outputs are controlled using a PWM interface (IN1/IN2).

A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

This device greatly reduces the component count of motor driver systems by integrating the necessary driver FETs and FET control circuitry into a single device. In addition, the SC8837C device adds protection features beyond traditional discrete implementations: undervoltage lockout, overcurrent protection, and thermal shutdown.

6.2 Functional Black Diagram



6.3 Feature Description

6.3.1 Bridge Control

The SC8837C device is controlled using a PWM input interface, also called an IN/IN interface. Each output is controlled by a corresponding input pin.

Table 1 shows the logic for the SC8837C device.

Table 1. SC8837C Device Logic

nSLEEP	IN1	IN2	OUT1	OUT2	FUNCTION (DC MOTOR)
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

6.3.2 Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the SC8837C device enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

6.3.3 Power Supplies and Input Pins

The input pins can be driven within the recommended operating conditions with or without the VCC, VM, or both power supplies present. No leakage current path exists to the supply. Each input pin has a weak pulldown resistor (approximately 100 kΩ) to ground.

The VCC and VM supplies can be applied and removed in any order. When the VCC supply is removed, the device enters a low-power state and draws very little current from the VM supply. The VCC and VM pins can be connected together if the supply voltage is between 1.6 and 7.0 V.

The VM voltage supply does not have any undervoltage-lockout protection (UVLO). As long as $V_{CC} > 1.6$ V, the internal device logic remains active which means that the VM pin voltage can drop to 0 V, however, the load may not be sufficiently driven at low VM voltages.

6.3.4 Protection Circuits

The SC8837C is fully protected against VCC undervoltage, overcurrent, and overtemperature events.

VCC undervoltage lockout

If at any time the voltage on the VCC pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when the VCC pin voltage rises above the UVLO threshold.

Overcurrent protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than tDEG, all FETs in the H-bridge are disabled. Operation resumes automatically after tRETRY has elapsed. Overcurrent conditions are detected on both the high-side and low-side devices. A short to the VM pin, GND, or from the OUT1 pin to the OUT2 pin results in an overcurrent condition.

Thermal shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level, operation automatically resumes.

Table 2. Fault Behavior

FAULT	CONDITION	H-BRIDGE	INTERNAL CIRCUIT	RECOVERY
VCC undervoltage(UVLO)	V_{CC}<1.5V	**Disabled**	**Disabled**	V_{CC}>1.6V
Overcurrent(OCP)	I_{OUT}>1.2A(MIN)	**Disabled**	**Operating**	t_{OCR}
Thermal Shutdown(TSD)	T_J>150°C(MIN)	**Disabled**	**Operating**	T_J<150°C

6.4 Device Functional Modes

The SC8837C device is active unless the nSLEEP pin is brought logic low. In sleep mode the H-bridge FETs are disabled Hi-Z. The SC8837C device is brought out of sleep mode automatically if nSLEEP is brought logic high.

The H-bridge outputs are disabled during undervoltage lockout, overcurrent, and overtemperature fault conditions.

Table 3. Device Operating Modes

OPERATING MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Operating	**nSLEEP high**	**Operating**	**Operating**
Sleep mode	**nSLEEP low**	**Disabled**	**Disabled**
Fault encountered	**Any fault condition met**	**Disabled**	**See Table2**

7 Application and Implementation

NOTE

Information in the following applications sections is not part of the SteadiChips Component specification, and SteadiChips does not warrant its accuracy or completeness. SteadiChips's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The SC8837C device is device is used to drive one DC motor or other devices like solenoids. The following design procedure can be used to configure the SC8837C device.

7.2 Typical Application

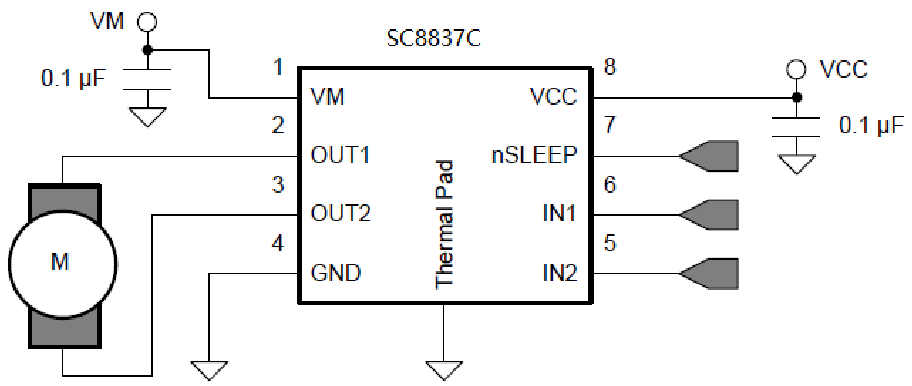


Figure 2. Schematic of SC8837C Application

8 Power Supply Recommendations

8.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power-supply capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless dc, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate size of bulk capacitor.

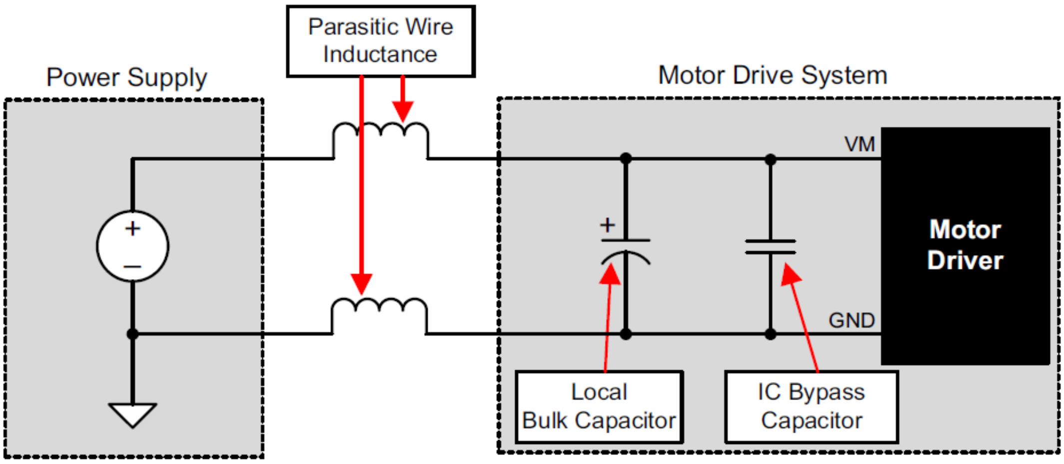


Figure 3. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply

9 Layout

9.1 Layout Guidelines

The VM and VCC pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 µF rated for the VM and VCC supplies. These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin. In addition bulk capacitance is required on the VM pin.

9.2 Layout Example

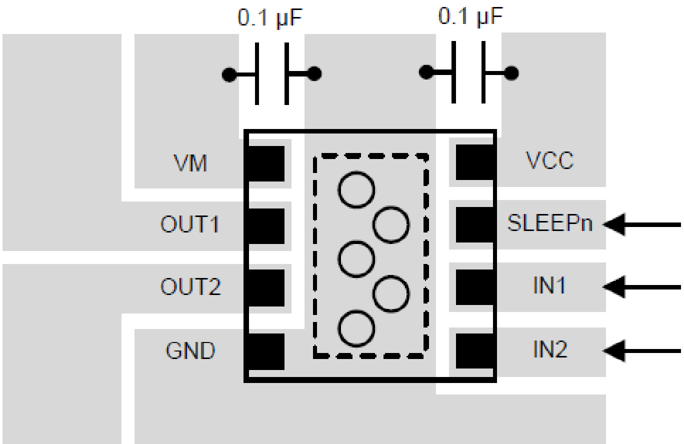


Figure 4. Simplified Layout Example

9.3 Power Dissipation

Power dissipation in the SC8837C is dominated by the power dissipated in the output FET resistance, or $R_{DS(on)}$. Average power dissipation when running both H-bridges can be roughly estimated by Equation 1:

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2 \tag{1}$$

where

- P_{TOT} is the total power dissipation
- $R_{DS(ON)}$ is the resistance of the HS plus LS FETs
- $I_{OUT(RMS)}$ is the RMS or DC output current being supplied to the load

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

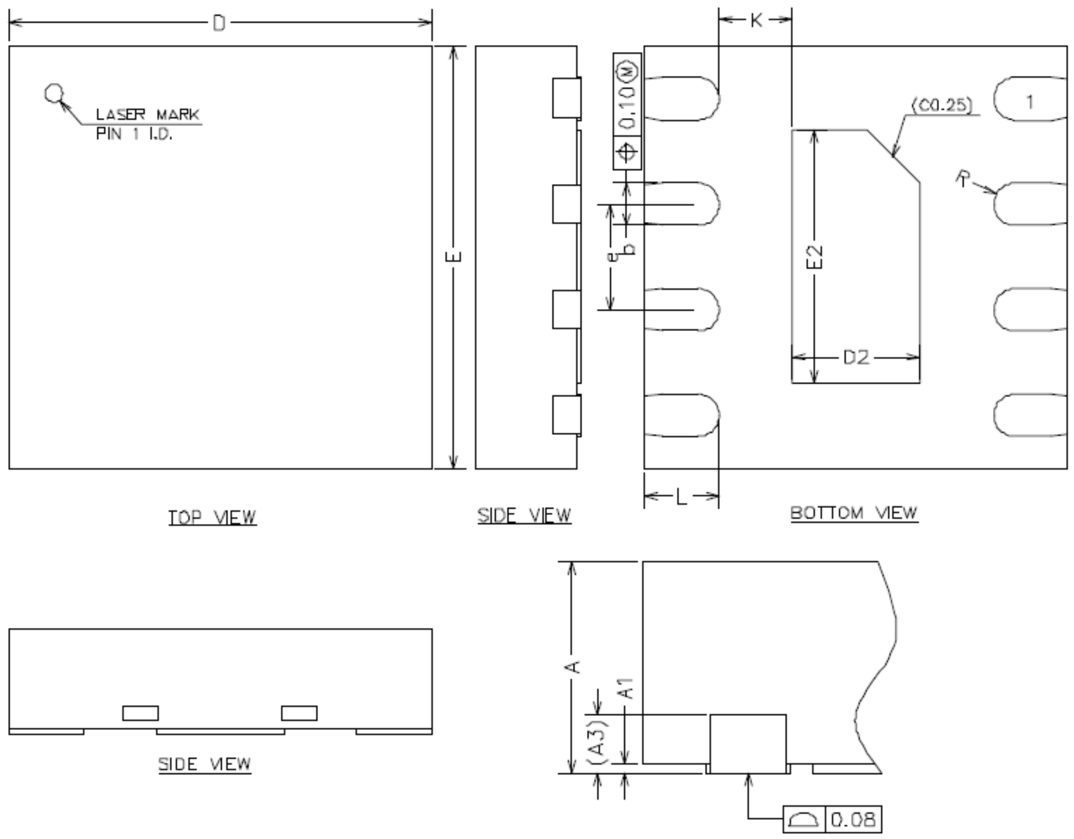
NOTE

The value of $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases.

The SC8837C device has thermal shutdown protection. If the die temperature exceeds approximately 150℃, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10 Package Outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.50	0.60	0.70
E2	1.10	1.20	1.30
e	0.40	0.50	0.60
K	0.20	—	—
L	0.30	0.35	0.40
R	0.09	—	—