

**P-Channel 30-V (D-S) MOSFET**

**GENERAL DESCRIPTION**

The ME7839S P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

**FEATURES**

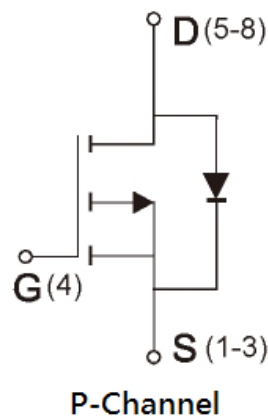
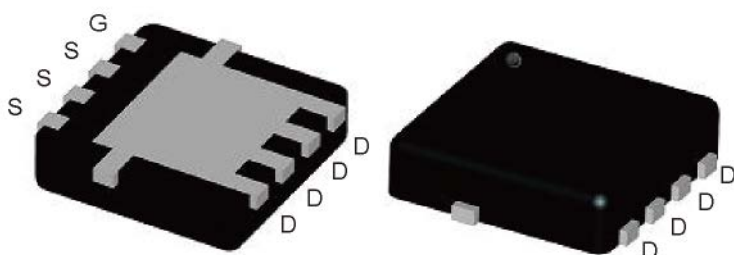
- $R_{DS(ON)} \leq 12m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 19m\Omega @ V_{GS} = -4.5V$

**APPLICATIONS**

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

**PIN CONFIGURATION**

(DFN(S) 3X3)  
Top View



Ordering Information: ME7839S-G (Green product-Halogen free)

**Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)**

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V <sub>DS</sub>	-30	V
Gate-Source Voltage	V <sub>GS</sub>	±25	V
Continuous Drain Current	I <sub>D</sub>	TA=25°C	36.1
		TA=70°C	28.9
Pulsed Drain Current	I <sub>DM</sub>	144	A
Maximum Power Dissipation	P <sub>D</sub>	TA=25°C	25
		TA=70°C	16
Operating Junction Temperature	T <sub>J</sub>	-55 to 150	°C
Thermal Resistance-Junction to Ambient*	R <sub>θJA</sub>	5	°C/W

\*The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper



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**Electrical Characteristics** ( $T_A=25^{\circ}\text{C}$  Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1		-2.5	V
$I_{GSS}$	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 25V$			$\pm 100$	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-24V, V_{GS}=0V$			-1	$\mu A$
$R_{DS(ON)}$	Drain-Source On-State Resistance <sup>a</sup>	$V_{GS}=-10V, I_D=-12A$		8	12	m $\Omega$
		$V_{GS}=-4.5V, I_D=-9A$		12	19	
$V_{SD}$	Diode Forward Voltage	$I_S=-1A, V_{GS}=0V$			-1	V
<b>DYNAMIC</b>						
$Q_g$	Total Gate Charge	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-15A$		27.6		nc
$Q_{gs}$	Gate-Source Charge			14.1		
$Q_{gd}$	Gate-Drain Charge			16.3		
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$		2690		pF
$C_{oss}$	Output Capacitance			371		
$C_{rss}$	Reverse Transfer Capacitance			293		
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$		6.5		$\Omega$
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=-15V, R_L=15\Omega$ $R_{GEN}=3.3\Omega, V_{GS}=-10V$		45.5		ns
$t_r$	Turn-On Rise Time			19.3		
$t_{d(off)}$	Turn-Off Delay Time			152		
$t_f$	Turn-Off Fall Time			40.8		

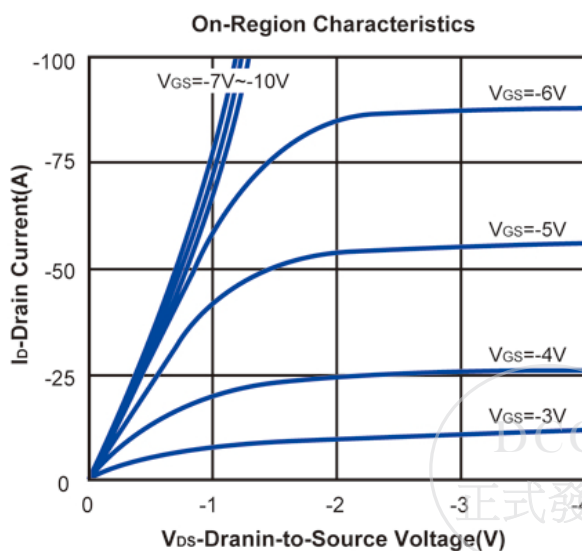
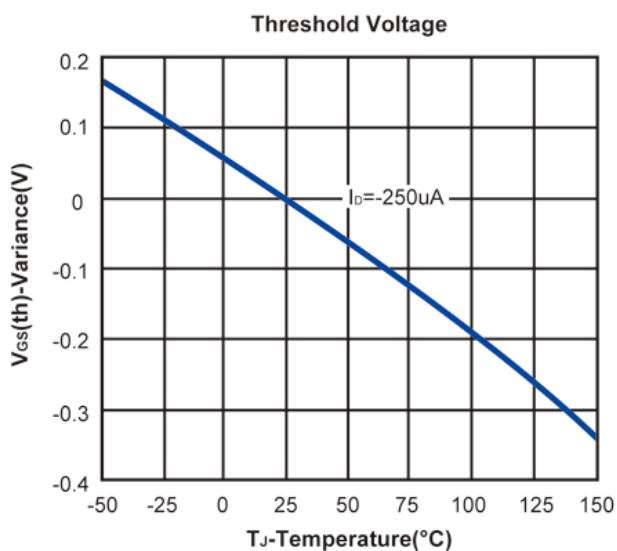
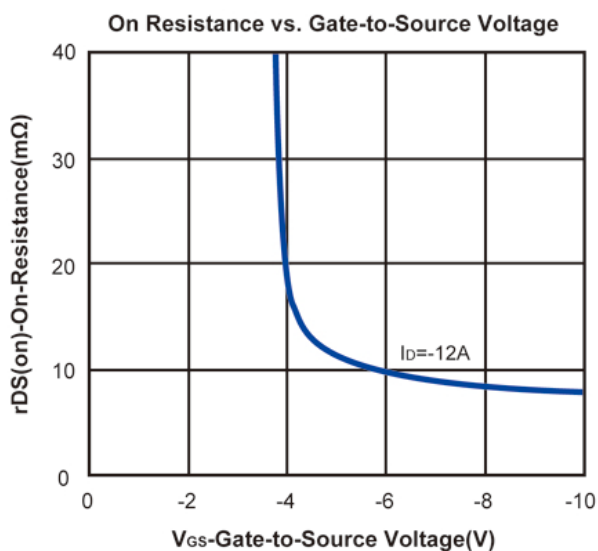
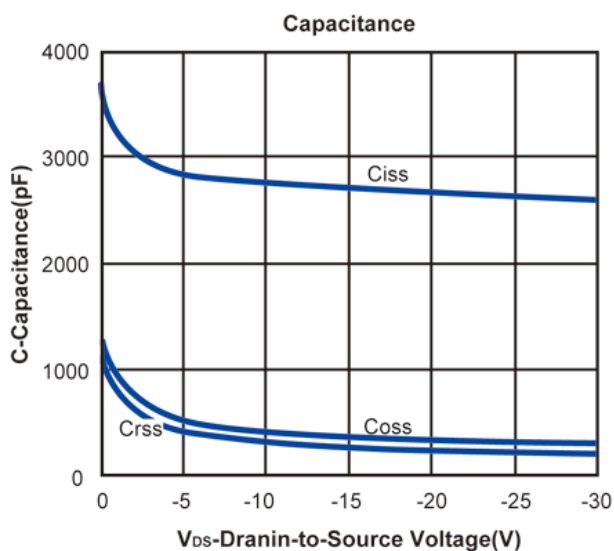
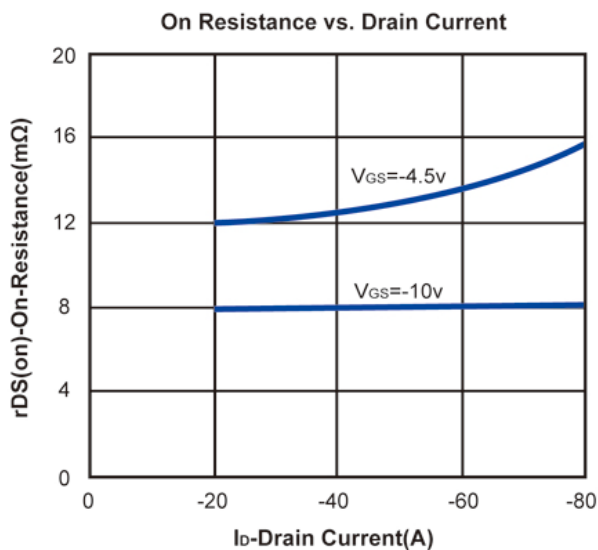
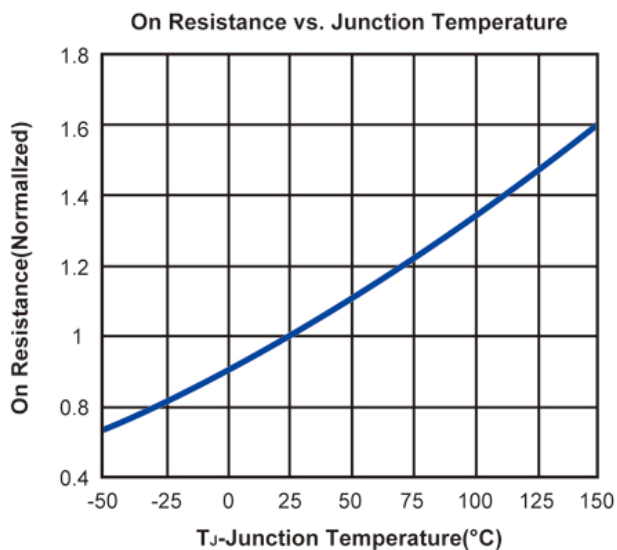
 Note:a. Pulse test: pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ 

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



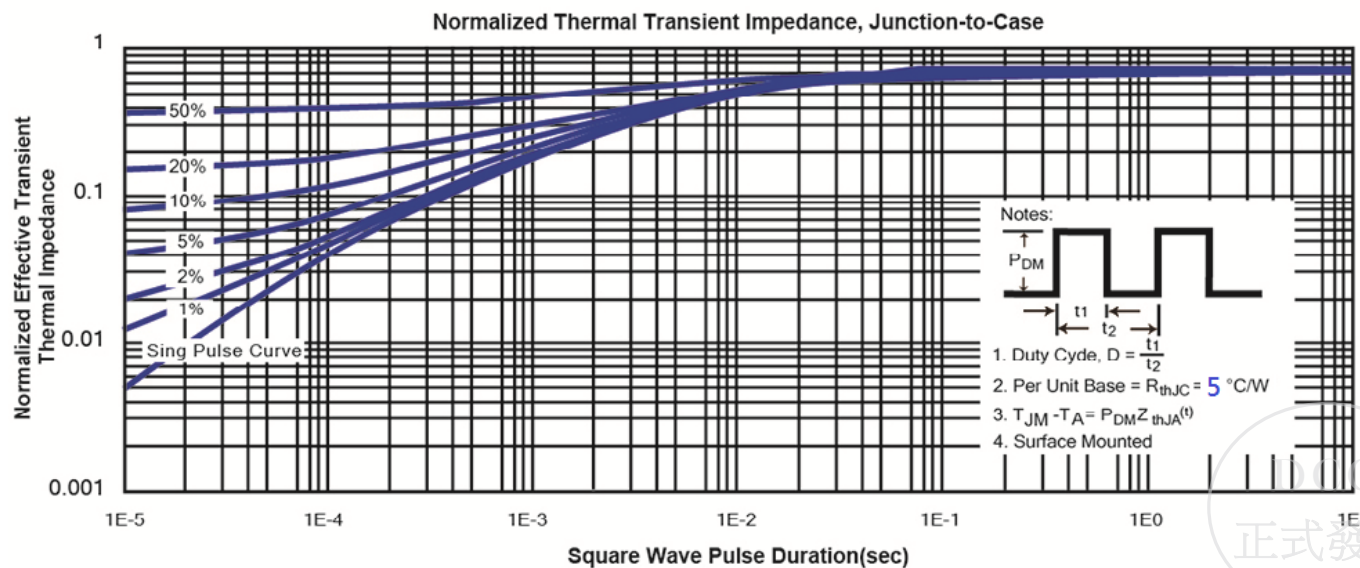
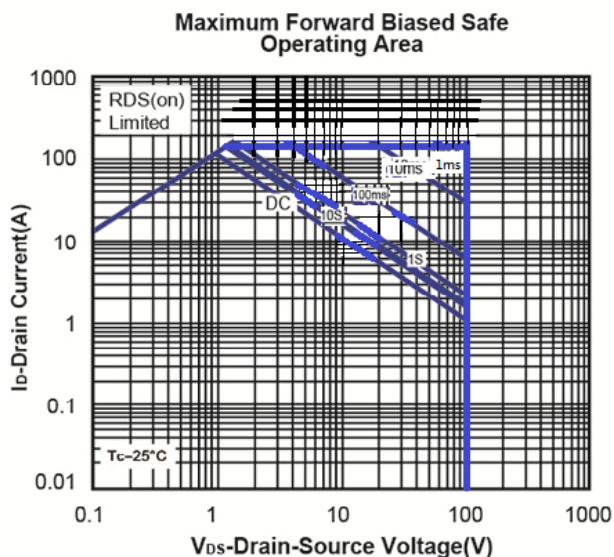
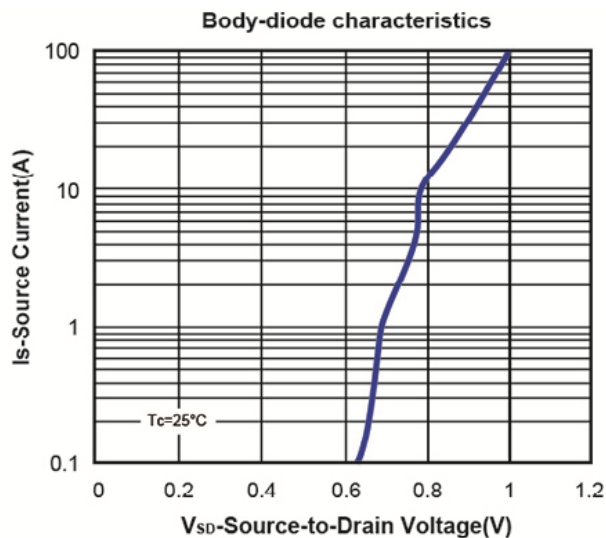
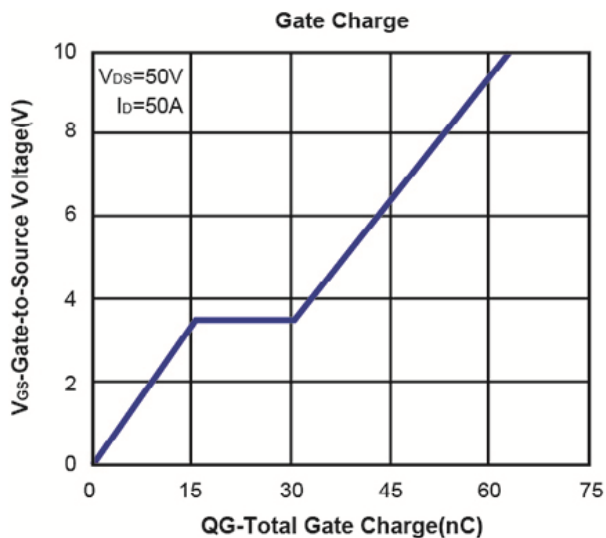
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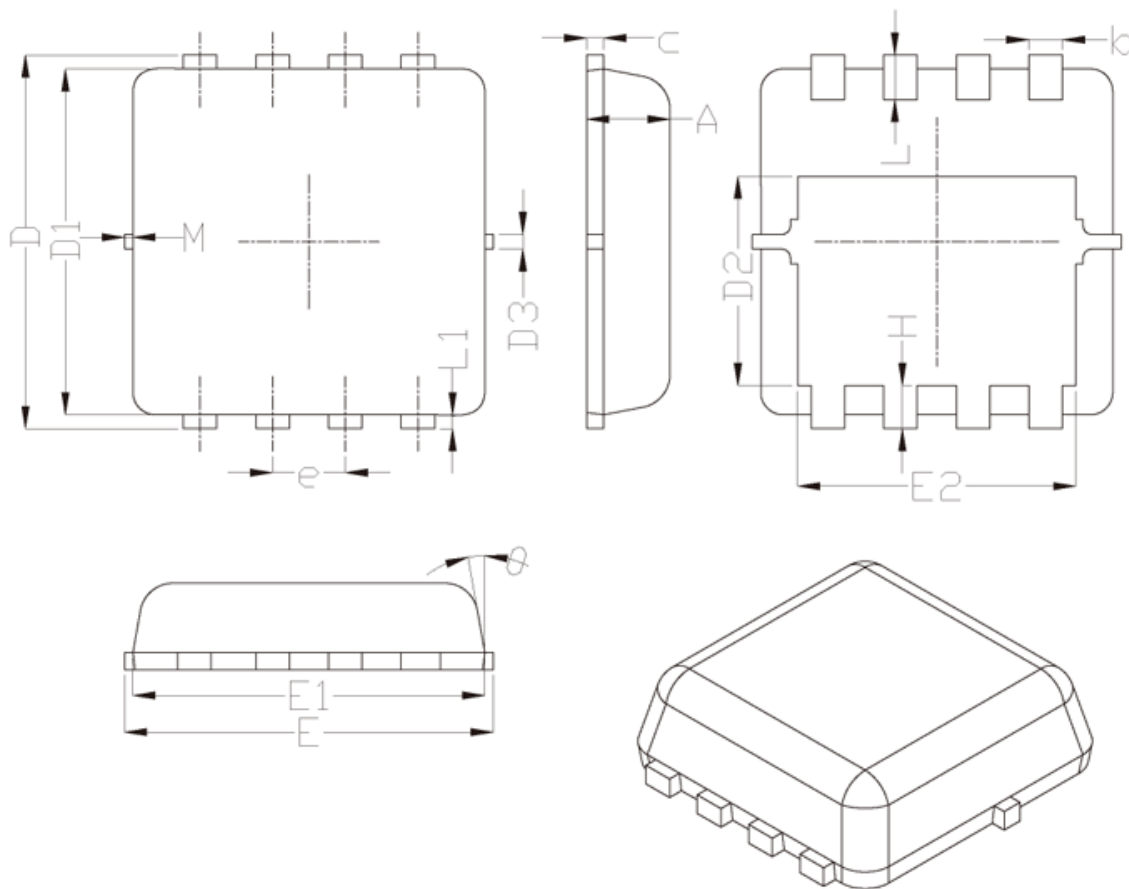
**Typical Characteristics (T<sub>J</sub> =25°C Noted)**



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**Typical Characteristics (T<sub>J</sub> =25°C Noted)**





SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
θ	---	10°	12°
M	*	*	0.15
* Not specified			

