

P-Channel Enhancement Mode Mosfet , ESD Protection

GENERAL DESCRIPTION

The ME4413D is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where low in-line power loss are needed in a very small outline surface mount package.

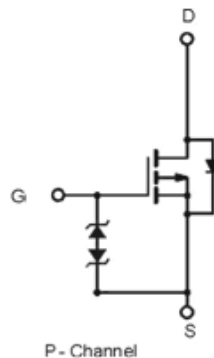
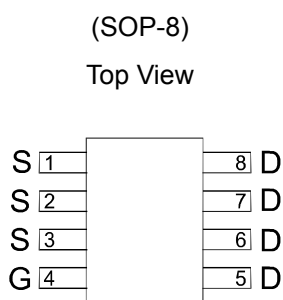
FEATURES

- $R_{DS(ON)} \leq 13m\Omega @ V_{GS} = -4.5V$
- $R_{DS(ON)} \leq 17m\Omega @ V_{GS} = -2.5V$
- $R_{DS(ON)} \leq 26m\Omega @ V_{GS} = -1.8V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- ESD protection

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System

PIN CONFIGURATION



Ordering Information: ME4413D (Pb-free)
 ME4413D-G (Green product)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	-12	V
Gate-Source Voltage		V_{GSS}	± 8	V
Continuous Drain Current ($T_j = 150^\circ C$)*	$T_A = 25^\circ C$	I_D	-11.5	A
	$T_A = 70^\circ C$		-9.2	
Pulsed Drain Current		I_{DM}	-46	A
Maximum Power Dissipation	$T_A = 25^\circ C$	P_D	2.78	W
	$T_A = 70^\circ C$		1.78	
Operating Junction Temperature		T_J	-55 to 150	$^\circ C$
Storage Temperature Range		T_{stg}	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	Steady state 45	$^\circ C/W$

* The device mounted on 1in² FR4 board with 2 oz copper

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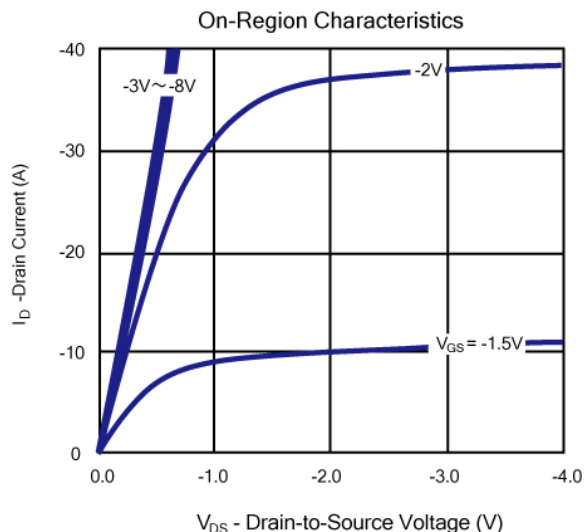
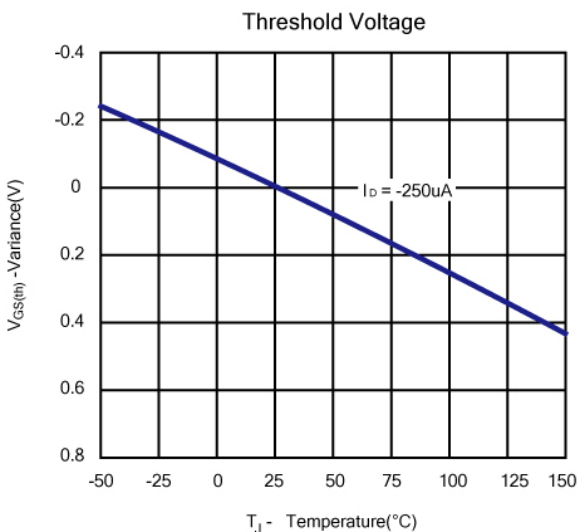
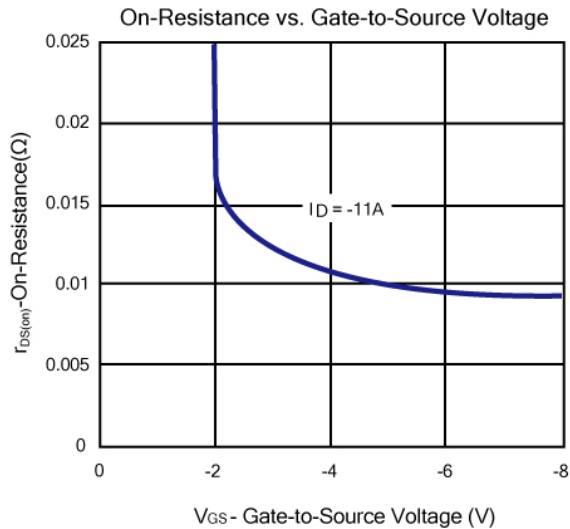
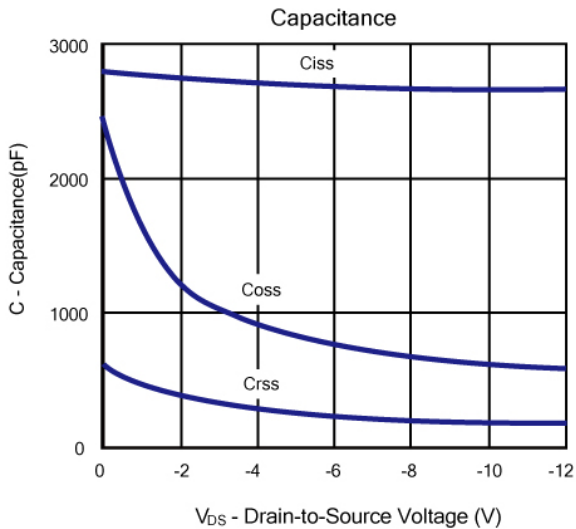
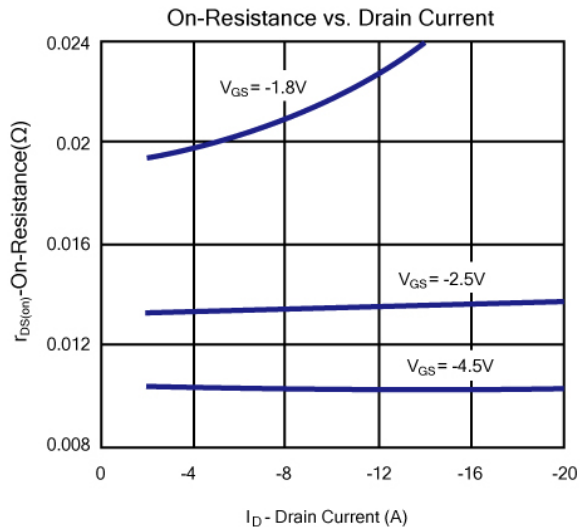
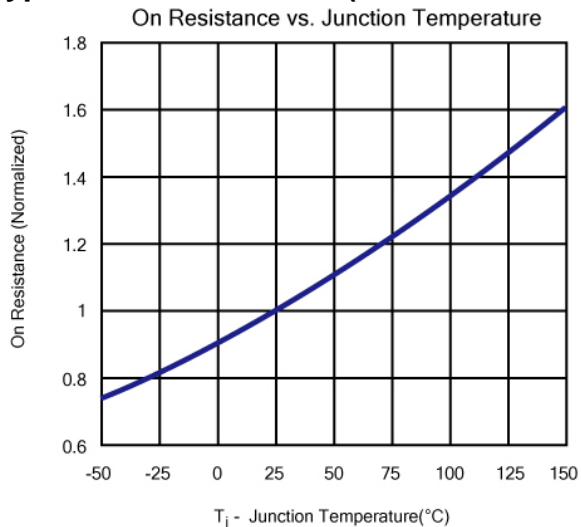
Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μA	-12			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-0.4		-1	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±8V			±10	μA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-12V, V _{GS} =0V			-1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =-4.5V, I _D = -11A		10.5	13	mΩ
		V _{GS} =-2.5V, I _D = -10A		13.5	17	
		V _{GS} =-1.8V, I _D = -6A		20.5	26	
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.6	-1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-6V, V _{GS} =-4.5V, I _D =-11A		39		nC
Q _{gs}	Gate-Source Charge			8.1		
Q _{gd}	Gate-Drain Charge			14		
R _g	Gate resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		5.5		Ω
C _{iss}	Input Capacitance	V _{DS} =-6V, V _{GS} =0V, f=1MHz		2700		pF
C _{oss}	Output Capacitance			760		
C _{rss}	Reverse Transfer Capacitance			240		
t _{d(on)}	Turn-On Delay Time	V _{DS} =-6V, R _L =6Ω R _{GEN} =3Ω, V _{GS} =-4.5V		74		ns
t _r	Turn-On Rise Time			40		
t _{d(off)}	Turn-Off Delay Time			140		
t _f	Turn-Off Fall time			250		

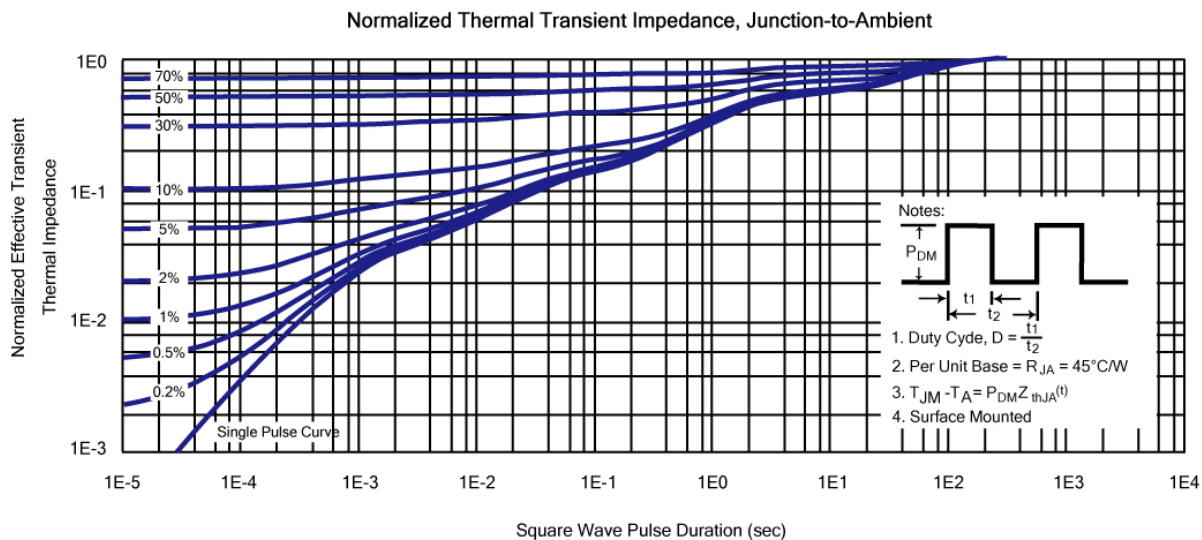
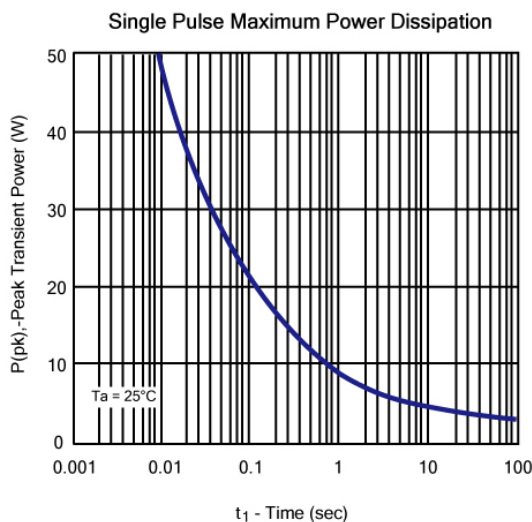
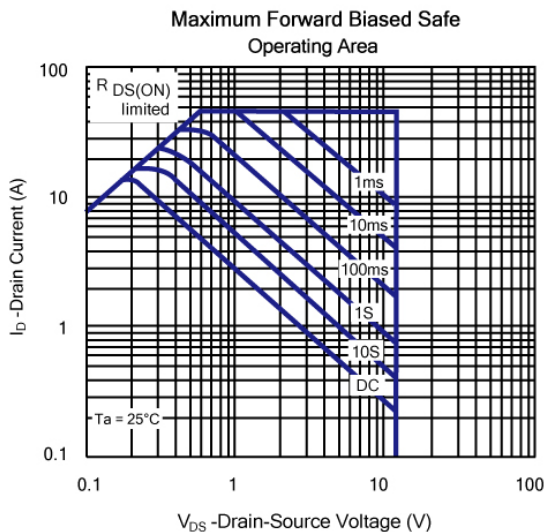
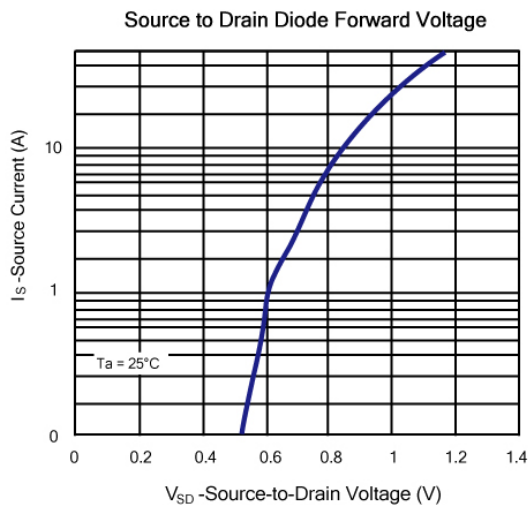
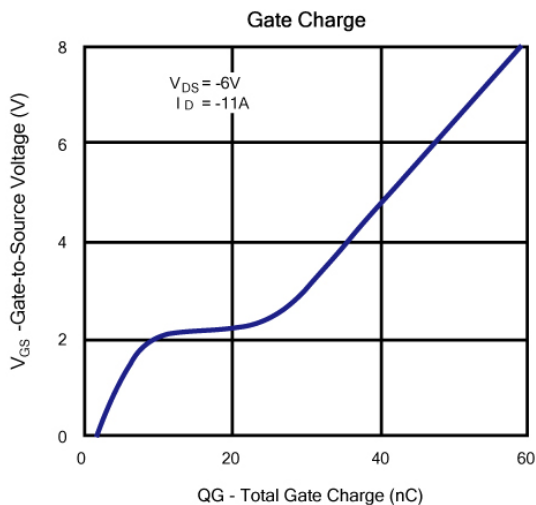
Notes: Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

Matsuki reserves the right to improve product design, functions and reliability without notice.

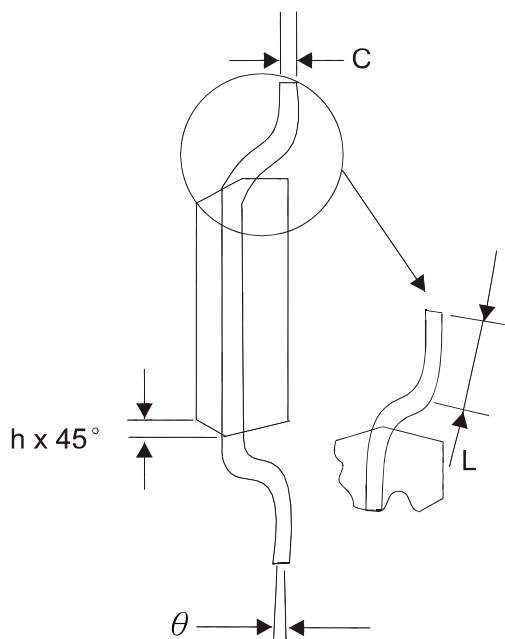
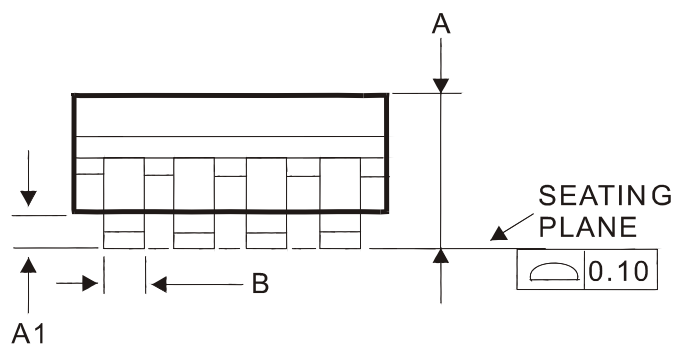
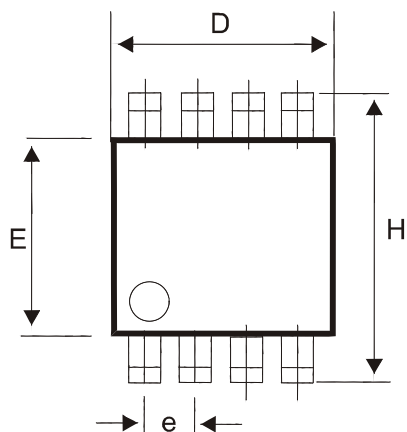
Typical Characteristics (T_J =25°C Noted)



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SOP-8 Package Outline



DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.