

**N-Channel 60V (D-S) MOSFET**

**GENERAL DESCRIPTION**

The ME3205T is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

**FEATURES**

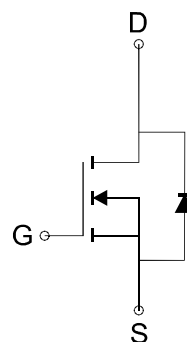
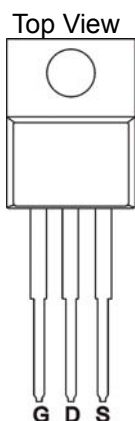
- $R_{DS(ON)} \leq 6.5m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

**APPLICATIONS**

- Power Management
- DC/DC Converter

**PIN CONFIGURATION**

(TO-220)



N-Channel MOSFET

Ordering Information: ME3205T (Pb-free)

ME3205T-G (Green product-Halogen free)

**Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)**

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current*	$I_D$	$T_C=25^\circ C$	105
		$T_C=70^\circ C$	88
Pulsed Drain Current	$I_{DM}$	419	A
Maximum Power Dissipation	$P_D$	$T_C=25^\circ C$	150
		$T_C=70^\circ C$	105
Operating Junction Temperature	$T_J$	-55 to 175	°C
Thermal Resistance-Junction to Case**	$R_{\theta JC}$	1	°C/W

\*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 80A.

\*\* The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper.

## N-Channel 60V (D-S) MOSFET

Electrical Characteristics (T<sub>c</sub> =25°C Unless Otherwise Specified)

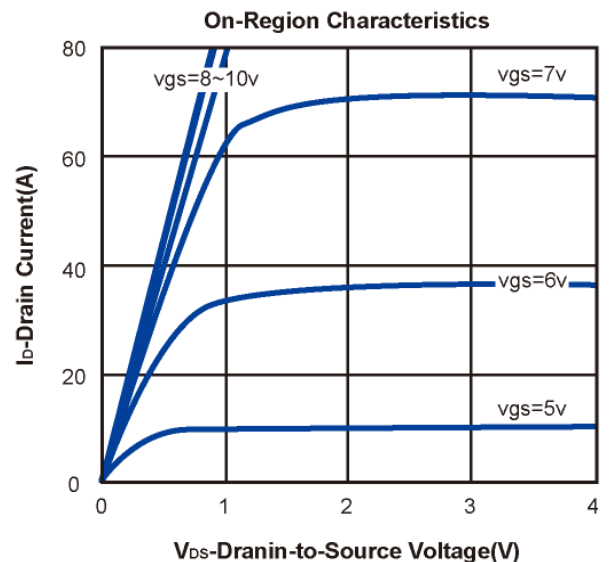
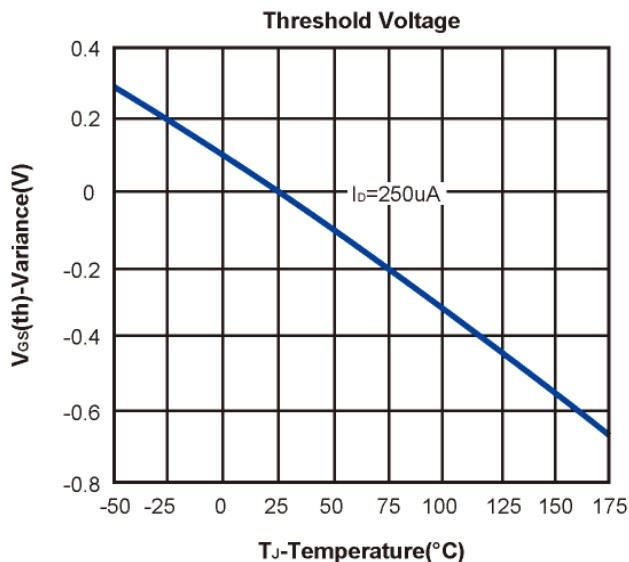
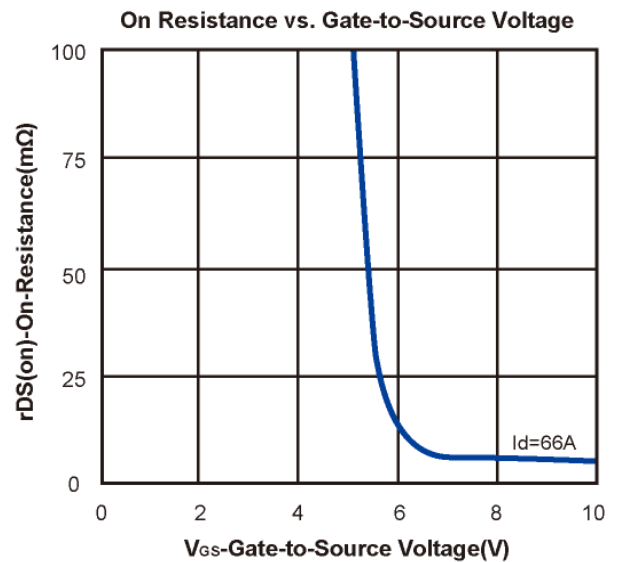
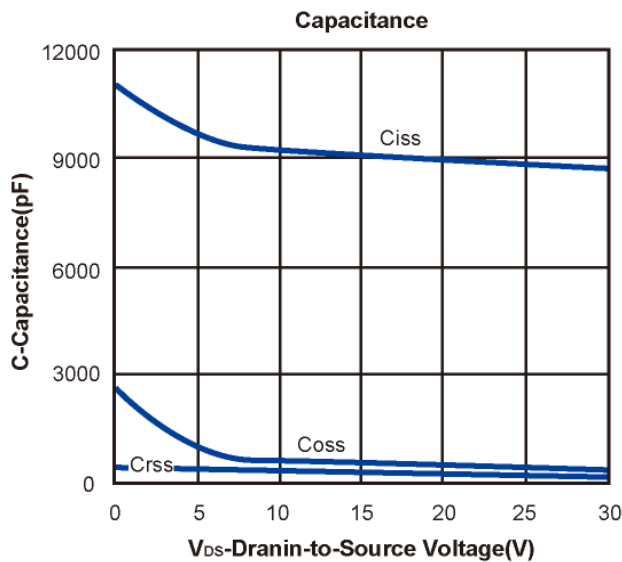
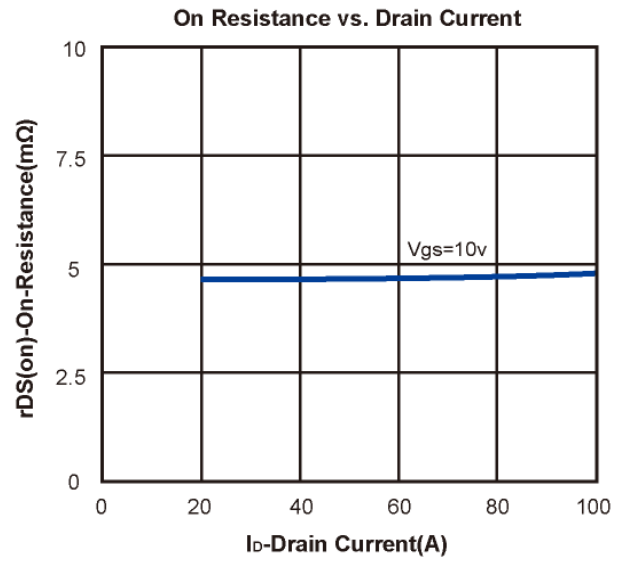
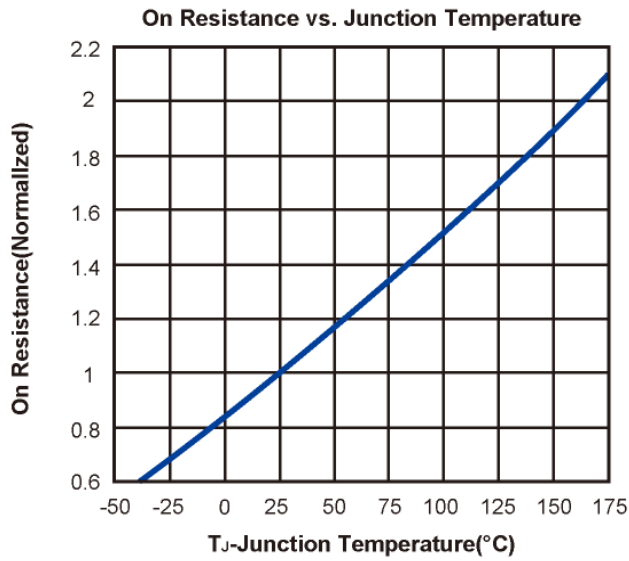
Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA	60			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	2		4	V
I <sub>GSS</sub>	Gate-Body Leakage	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60, V <sub>GS</sub> =0V			1	μA
R <sub>DS(ON)</sub>	Drain-Source On-Resistance*	V <sub>GS</sub> =10V, I <sub>D</sub> =66A		4.9	6.5	mΩ
V <sub>SD</sub>	Diode Forward Voltage*	I <sub>S</sub> =66A, V <sub>GS</sub> =0V			1.3	V
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> =44V, V <sub>GS</sub> =10V, I <sub>D</sub> =66A		133		nc
Q <sub>gs</sub>	Gate-Source Charge			42.5		
Q <sub>gd</sub>	Gate-Drain Charge			40.5		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		8793		pF
C <sub>oss</sub>	Output Capacitance			361		
C <sub>rss</sub>	Reverse Transfer Capacitance			193		
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz		1		Ω
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =28V, I <sub>D</sub> =66A, V <sub>GS</sub> =10V, R <sub>G</sub> =6.8Ω, R <sub>L</sub> =0.5Ω		60.9		ns
t <sub>r</sub>	Turn-On Rise Time			219		
t <sub>d(off)</sub>	Turn-Off Delay Time			114		
t <sub>f</sub>	Turn-Off Fall Time			34.3		

Notes: a, pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b, Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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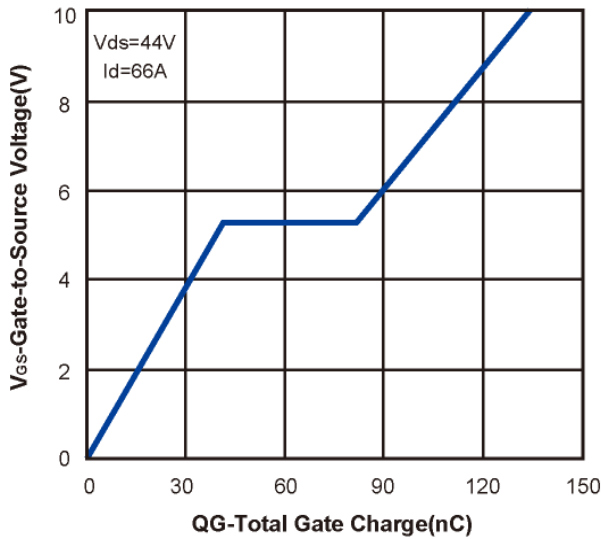
**Typical Characteristics (T<sub>J</sub> = 25°C Noted)**



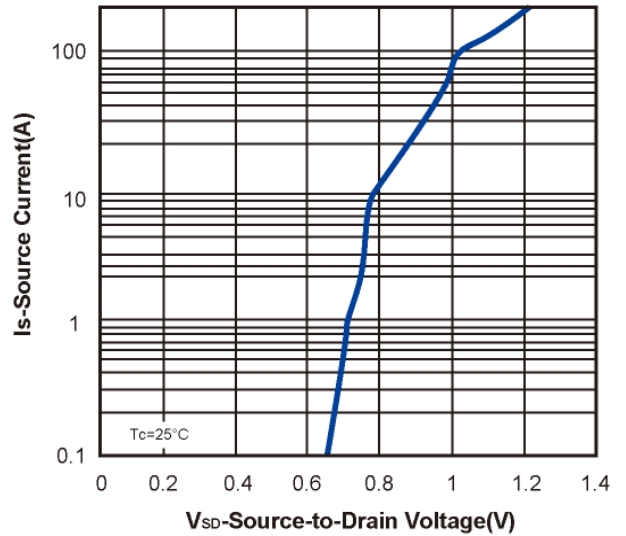
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**Typical Characteristics (T<sub>J</sub> = 25°C Noted)**

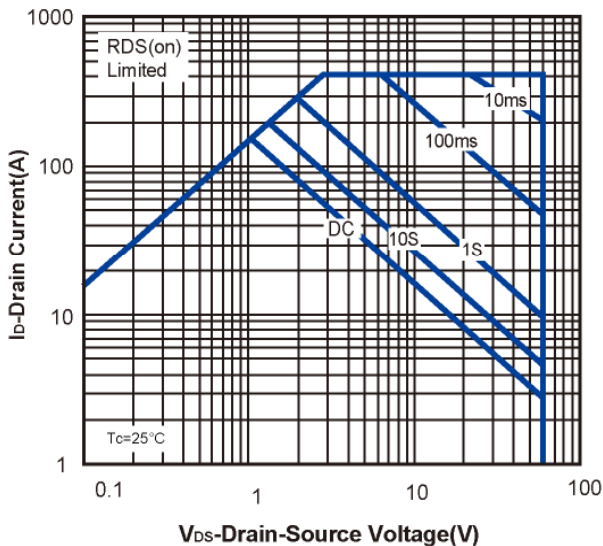
Gate Charge



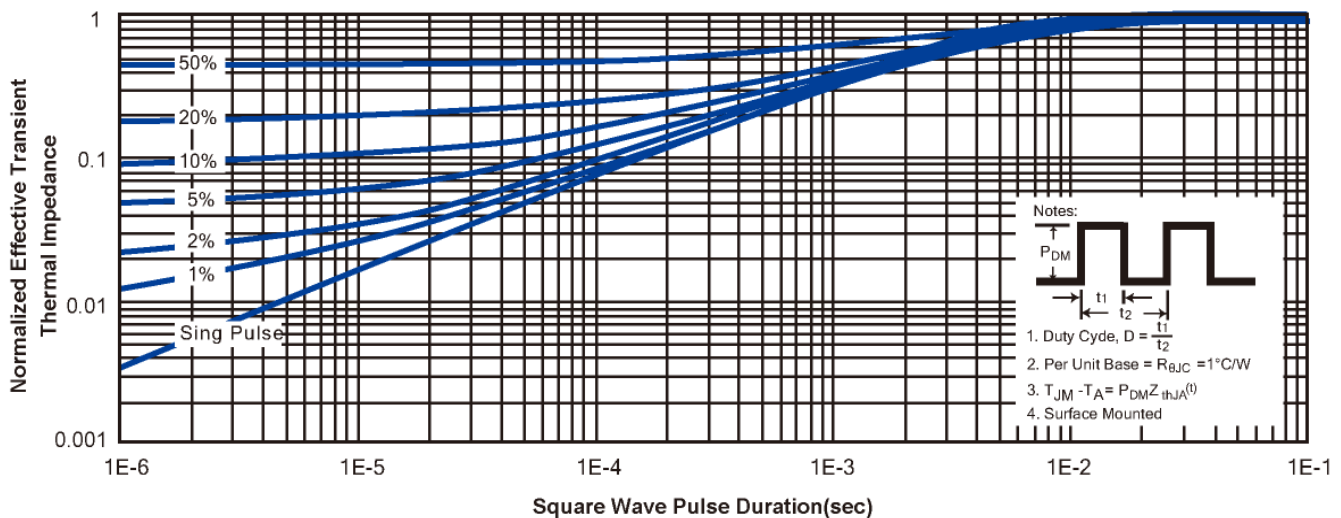
Body-diode characteristics



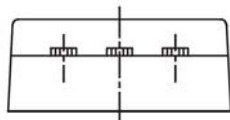
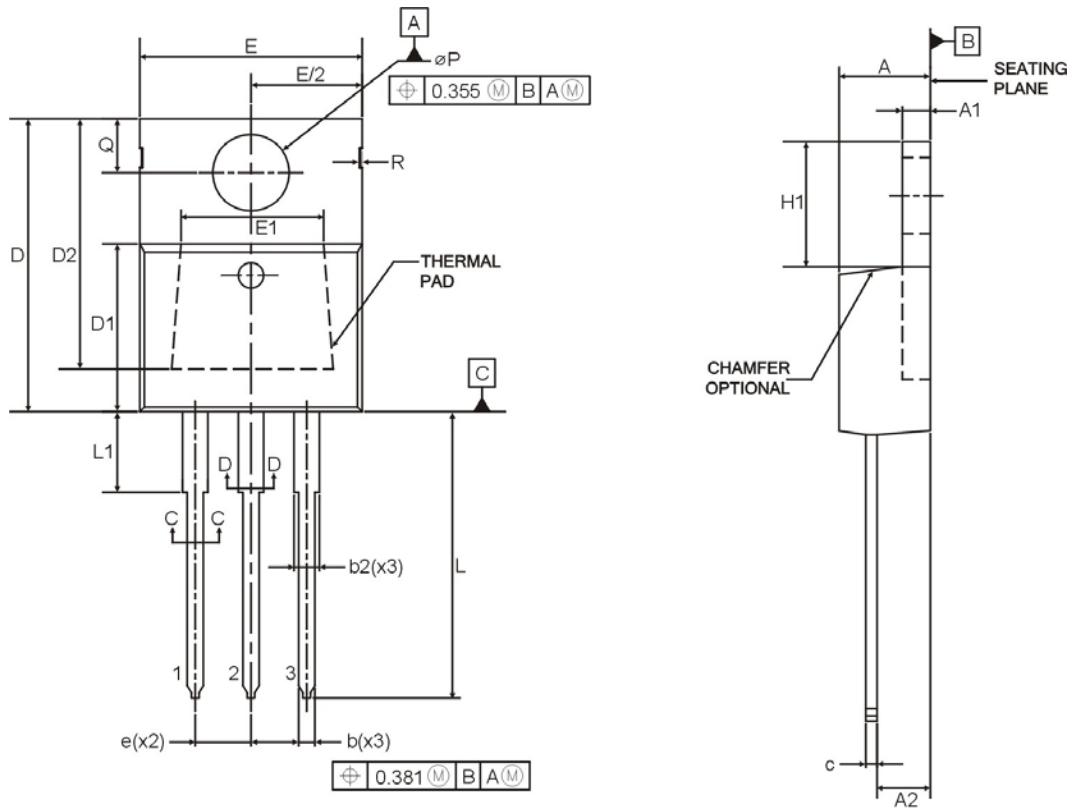
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



**TO-220 Package Outline**



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	3.500	4.90
A1	1.000	1.40
A2	2.000	3.00
b	0.500	1.00
c	0.350	0.65
D	14.00	16.50
D1	8.382	9.017
D2	12.00	13.00
E	9.600	10.70
E1	6.858	8.890
e	2.540 BSC	
H1	5.500	7.50
L	12.50	15.00
$\varnothing P$	3.810	3.860
Q	2.540	3.048
b2	1.100	1.80
L1	-	7.00