

## 600mA Linear Regulator for DC Fan Speed Control

### Features

- **Low Dropout Voltage: 220mV (Typical) @ 600mA**
- **Low Quiescent Current: 140mA**
- **Enable/Shutdown Function**
- **Output Voltage / VSET Voltage: 1.6 Times**
- **Stable with Low ESR Ceramic Capacitors**
- **Over-Temperature Protection**
- **Current-Limit Protection with Foldback Current**
- **Internal Soft-Start**
- **SOP-8 and TDFN3x3-8 Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

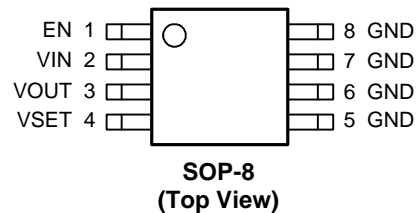
### General Description

The APL5607/A is a low quiescent current and low dropout linear regulator which is designed to power a DC fan and deliver up to 600mA output current. The output voltage follows the 1.6 times of VSET voltage and typical dropout voltage is only 220mV (typical) at 600mA output current. The APL5607/A with low 140µA quiescent current is ideal for battery-powered system appliances and stable with a 2.2µF ceramic output capacitor. The features of current-limit (with foldback current) and over-temperature protection protect the device against current over-loads and over temperature. The APL5607/A is available in SOP-8 and TDFN3x3-8 packages.

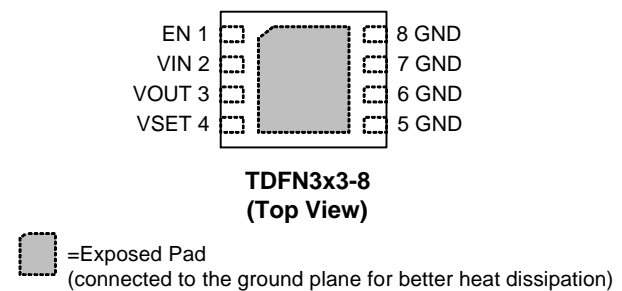
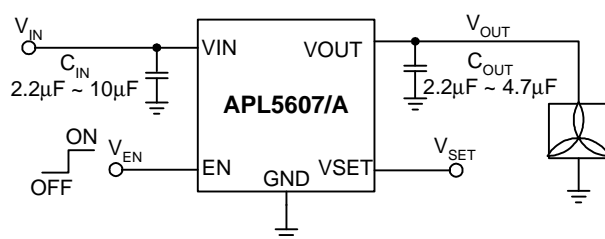
### Applications

- **Notebook Fan Driver**
- **Motherboards**
- **PC Peripherals**
- **Battery-Powered System**

### Pin Configuration

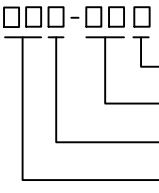


### Simplified Application Circuit



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

## Ordering and Marking Information

APL5607/A 	Package Code K : SOP-8    QB : TDFN3x3-8 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device			
APL5607/A K :	<table border="1"> <tr> <td>APL5607 •XXXXX</td> <td>APL5607A •XXXXX</td> <td>XXXXX - Date Code</td> </tr> </table>	APL5607 •XXXXX	APL5607A •XXXXX	XXXXX - Date Code
APL5607 •XXXXX	APL5607A •XXXXX	XXXXX - Date Code		
APL5607/A QB :	<table border="1"> <tr> <td>APL 5607 •XXXXX</td> <td>APL 5607A •XXXXX</td> <td>XXXXX - Date Code</td> </tr> </table>	APL 5607 •XXXXX	APL 5607A •XXXXX	XXXXX - Date Code
APL 5607 •XXXXX	APL 5607A •XXXXX	XXXXX - Date Code		

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
$V_{IN}$	VIN to GND	-0.3 ~ 6.5	V
$V_{EN}$	EN to GND	-0.3 ~ $V_{IN}+0.3$	V
$V_{OUT}$	VOUT to GND	-0.3 ~ $V_{IN}+0.3$	V
$T_J$	Maximum Junction Temperature	150	°C
$P_D$	Power Dissipation	Internally Limited	
$T_{STG}$	Storage Temperature Range	-65 ~ 150	°C
$T_{SDR}$	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
$\theta_{JA}$	Junction to Ambient Thermal Resistance <sup>(Note 2)</sup>		°C/W
	SOP-8	80	
	TDFN3x3-8	70	

Note 2:  $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air.

## Recommended Operating Conditions

Symbol	Parameter	Range	Unit
$V_{IN}$	VIN to GND	4.5 ~ 6	V
$V_{EN}$	EN to GND	0 ~ $V_{IN}$	V
$V_{OUT}$	VOUT to GND	0 ~ $V_{IN}-V_{DROP}$	V
$V_{SET}$	VSET to GND	0 ~ 3.3	V

**Recommended Operating Conditions (Cont.)**

Symbol	Parameter	Range	Unit
I <sub>OUT</sub>	Output Current	0 ~ 0.6	A
C <sub>IN</sub>	Input Capacitor	2.2 ~ 470	μF
C <sub>OUT</sub>	Output Capacitor	2.2 ~ 330	
T <sub>J</sub>	Junction Temperature	-40 ~ 125	°C
T <sub>A</sub>	Ambient Temperature	-40 ~ 85	°C

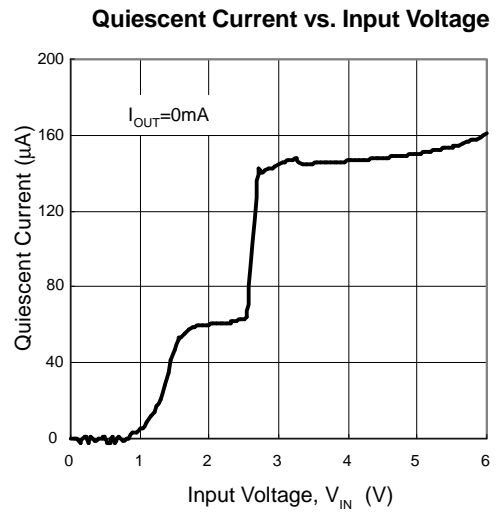
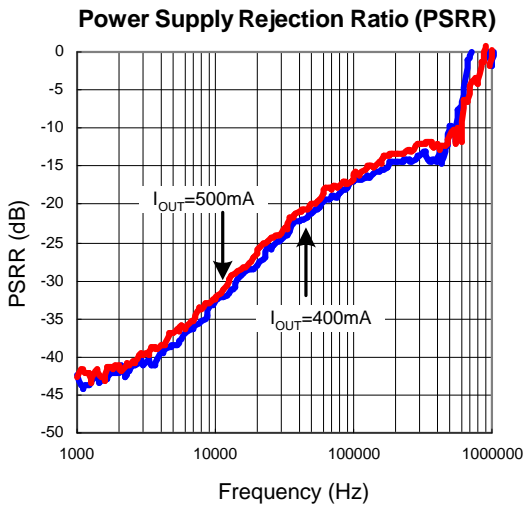
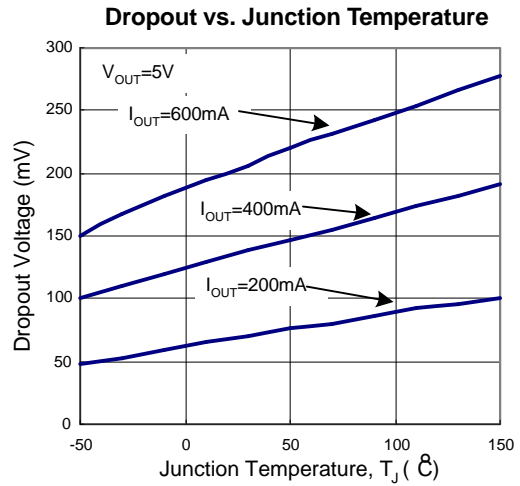
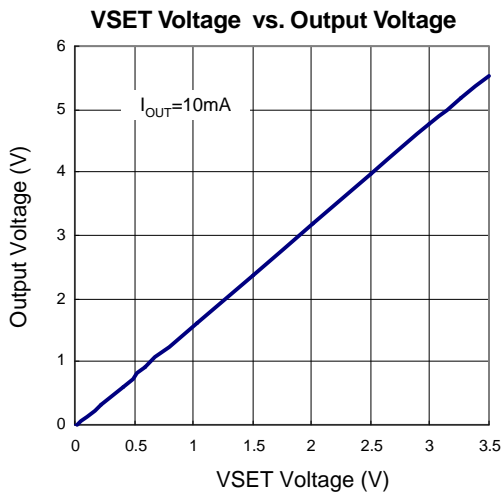
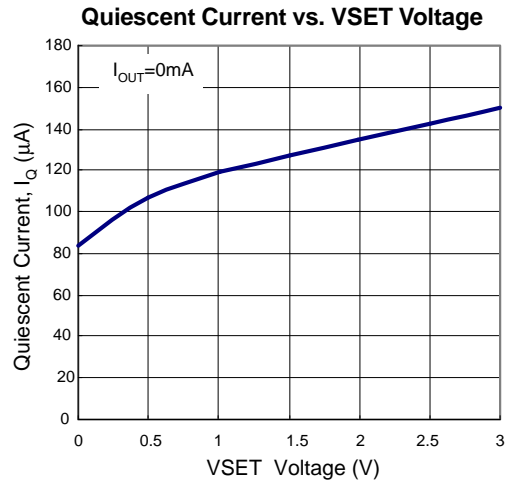
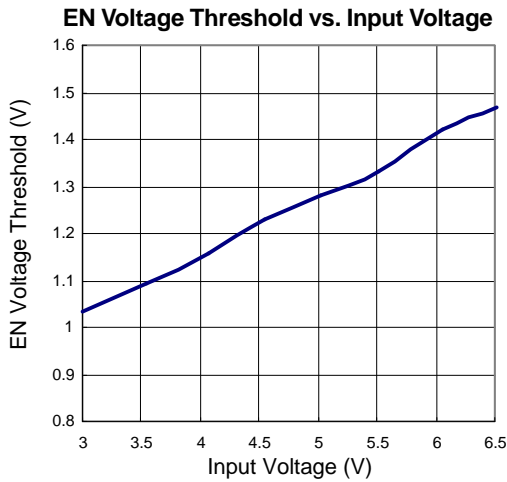
**Electrical Characteristics**

Refer to the typical application circuit. V<sub>IN</sub>=5V, V<sub>EN</sub>=V<sub>IN</sub>, I<sub>OUT</sub>=1mA~600mA, T<sub>J</sub>= -40 to 125°C, T<sub>A</sub>= -40 to 85°C, unless otherwise specified. Typical values are at T<sub>A</sub>=25°C.

Symbol	Parameter	Test Conditions	APL5607/A			Unit
			Min.	Typ.	Max.	
<b>SUPPLY CURRENT</b>						
I <sub>Q</sub>	Quiescent Current	V <sub>EN</sub> = 0V	-	-	1	μA
		V <sub>EN</sub> = 5V, I <sub>OUT</sub> = 0A	-	140	200	μA
<b>UNDER-VOLTAGE-LOCKOUT (UVLO)</b>						
	VIN UVLO Threshold	V <sub>IN</sub> rising	2.5	2.9	3.3	V
	VIN UVLO Hysteresis		-	0.15	-	V
<b>OUTPUT VOLTAGE</b>						
	VOUT Voltage / VSET Voltage	T <sub>J</sub> =25°C, V <sub>IN</sub> =5.5V, I <sub>OUT</sub> =1mA, V <sub>SET</sub> =3.3V	1.552	1.6	1.648	V/V
	VOUT Voltage / VSET Voltage	T <sub>J</sub> =40 ~ 125°C, V <sub>IN</sub> =5.5V, I <sub>OUT</sub> =1mA, V <sub>SET</sub> =1 ~ 3.3V	1.504	1.6	1.696	V/V
	VSET Pin Current	V <sub>SET</sub> =5V	-	0.05	1	μA
	Load Regulation	I <sub>OUT</sub> =1mA to 600mA	-	60	100	mV
V <sub>DROP</sub>	Dropout Voltage	I <sub>OUT</sub> =600mA, V <sub>OUT</sub> =5V	-	200	320	mV
<b>PROTECTION AND SOFT-START</b>						
	Output Current-Limit		700	-	-	mA
	Thermal Shutdown Temperature		-	150	-	°C
	Thermal Shutdown Hysteresis		-	40	-	°C
	Foldback Current-Limit	V <sub>OUT</sub> < 0.6V	-	250	-	mA
T <sub>SS</sub>	Soft-Start Time	V <sub>IN</sub> =0 to 5V, V <sub>EN</sub> =V <sub>IN</sub>	-	130	300	μs
	VOUT Pull Low Resistance	V <sub>EN</sub> =0V, V <sub>OUT</sub> =0.5V	-	60	-	Ω
<b>LOGIC INPUT</b>						
	EN Logic Input-High Level		1.6	-	-	V
	EN Logic Input-Low Level		-	-	0.4	V
	EN Pull-Low Resistance	APL5607, V <sub>EN</sub> <3V	-	2	-	MΩ
	EN Pull-High Resistance	APL5607A	-	390	-	kΩ

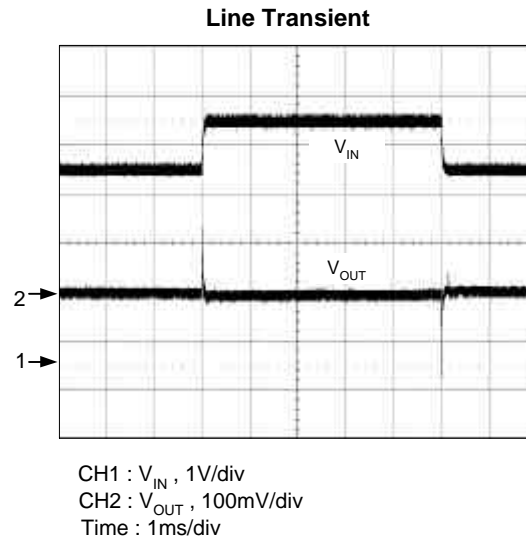
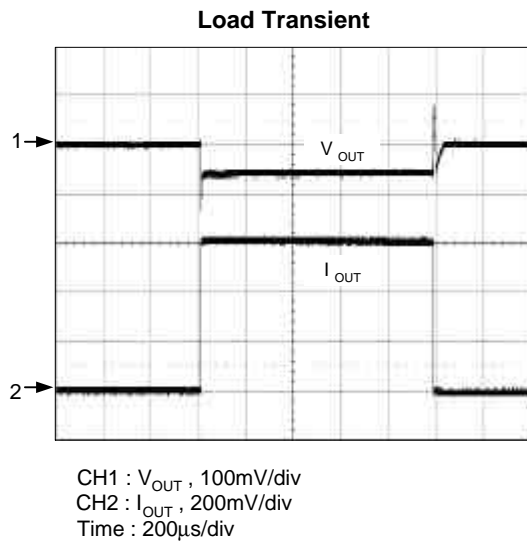
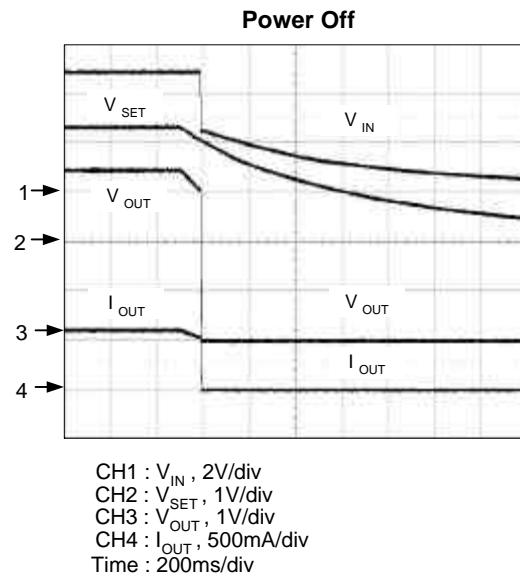
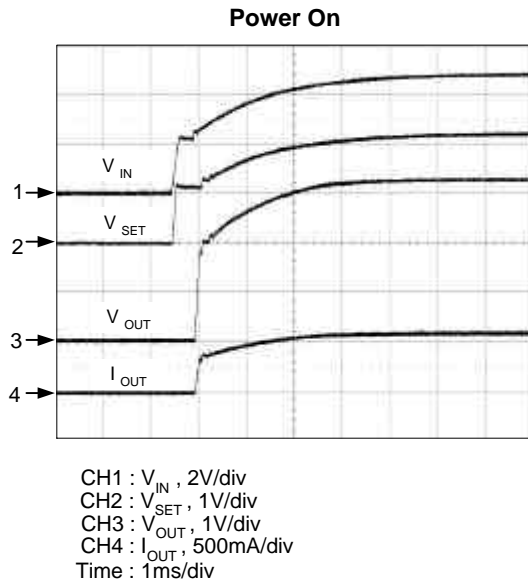
### Typical Operating Characteristics

$V_{IN}=5V$ ,  $V_{SET}=2V$ ,  $V_{OUT}=3.2V$ ,  $C_{IN}=2.2\mu F$ ,  $C_{OUT}=2.2\mu F$ , unless otherwise specified.



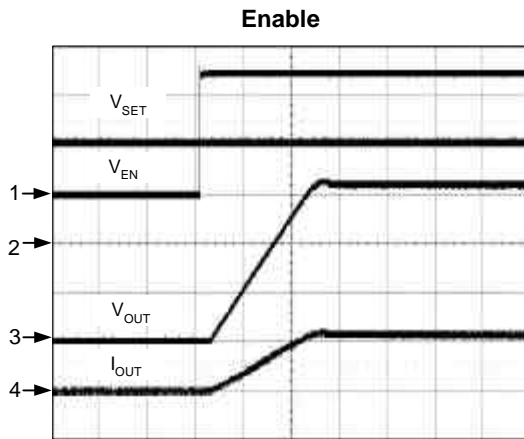
### Operating Waveforms

$V_{IN}=5V$ ,  $V_{SET}=2V$ ,  $V_{OUT}=3.2V$ ,  $C_{IN}=2.2\mu F$ ,  $C_{OUT}=2.2\mu F$ , unless otherwise specified.

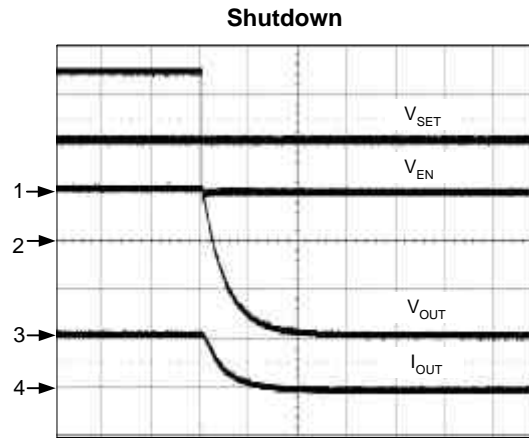


### Operating Waveforms (Cont.)

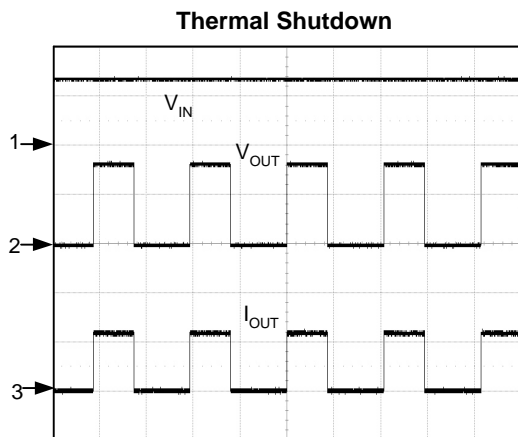
$V_{IN}=5V$ ,  $V_{SET}=2V$ ,  $V_{OUT}=3.2V$ ,  $C_{IN}=2.2\mu F$ ,  $C_{OUT}=2.2\mu F$ , unless otherwise specified.



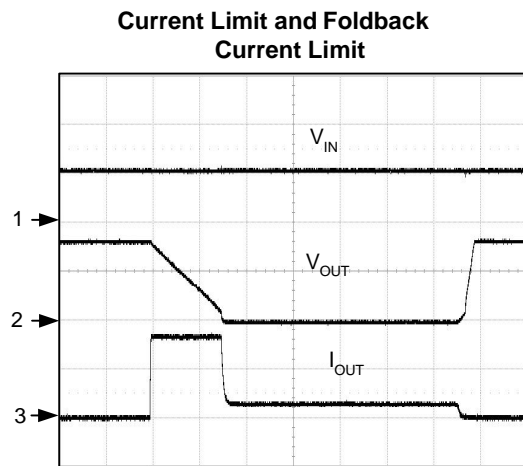
CH1 :  $V_{EN}$ , 2V/div  
 CH2 :  $V_{SET}$ , 1V/div  
 CH3 :  $V_{OUT}$ , 1V/div  
 CH4 :  $I_{OUT}$ , 500mA/div  
 Time : 200 $\mu$ s/div



CH1 :  $V_{EN}$ , 2V/div  
 CH2 :  $V_{SET}$ , 1V/div  
 CH3 :  $V_{OUT}$ , 1V/div  
 CH4 :  $I_{OUT}$ , 500mA/div  
 Time : 10 $\mu$ s/div



CH1 :  $V_{IN}$ , 5V/div  
 CH2 :  $V_{OUT}$ , 2V/div  
 CH3 :  $I_{OUT}$ , 500mA/div  
 Time : 500ms/div

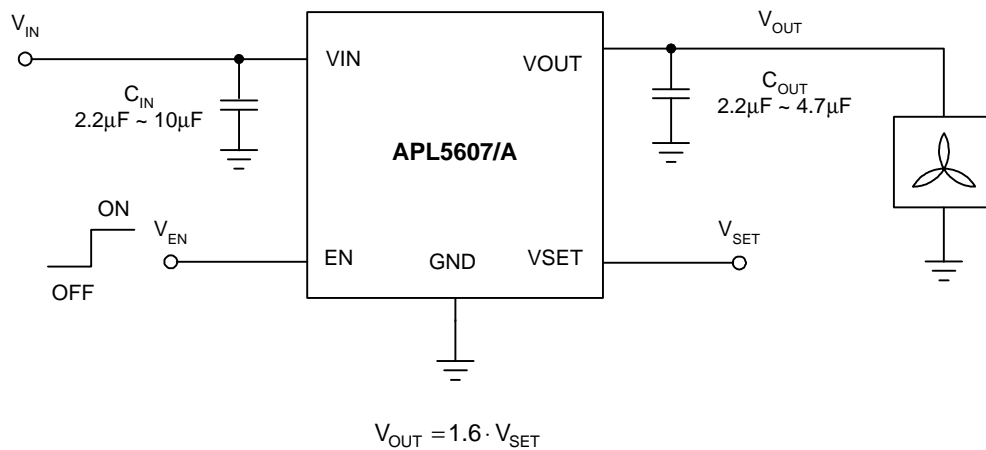


CH1 :  $V_{IN}$ , 5V/div  
 CH2 :  $V_{OUT}$ , 2V/div  
 CH3 :  $I_{OUT}$ , 1A/div  
 Time : 2ms/div

### Pin Description

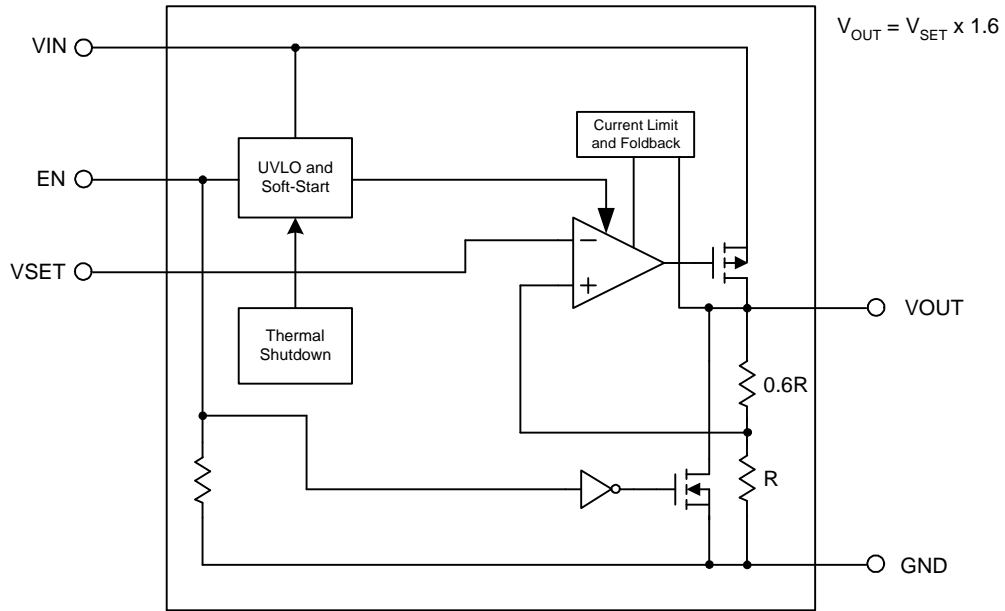
PIN		FUNCTION
NO.	NAME	
1	EN	Enable Control Input. Driving the EN high turns on the regulator. Pulling the EN low turns the regulator into shutdown mode. The EN is pulled low by an internal resistor.
2	VIN	Supply Voltage Input Pin. Supply voltage can range from 4.5V to 6V. Bypass with a 2.2μF (typical) capacitor to GND
3	VOUT	Regulator Output. Sources up to 600mA. A small capacitor is needed from this pin to ground to assure stability.
4	VSET	Output Voltage-Set Input. The output voltage follows the 1.6 times of the VSET voltage.
5,6,7,8	GND	Ground. These pins are internally connected with the internal leadframe. Connect these pins to a wide ground plane for good heat dissipation.

### Typical Application Circuit

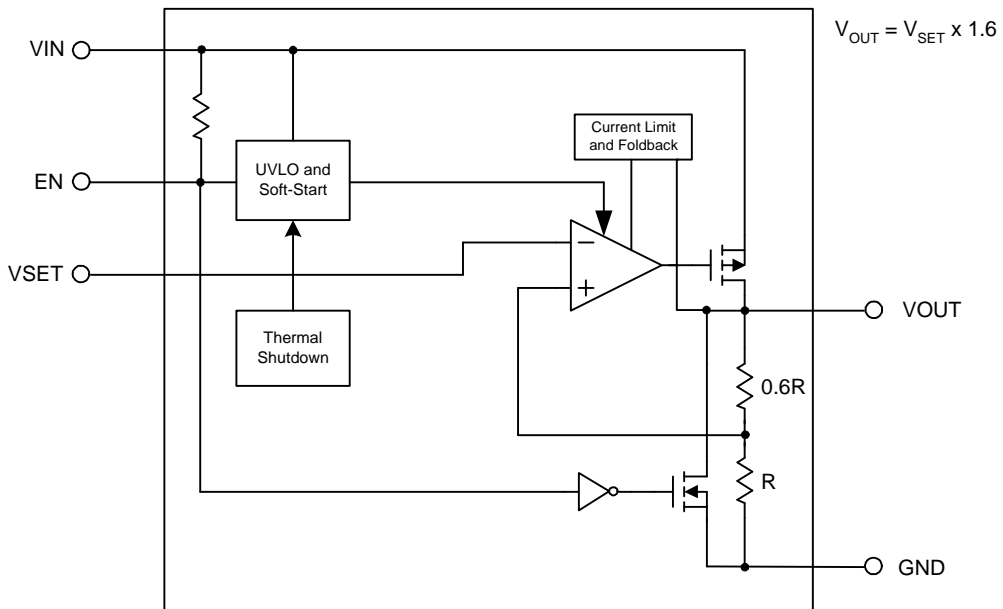


Block Diagram

APL5607



APL5607A





## Function Description

### Under-Voltage Lock-Out (UVLO)

The APL5607/A has a built-in under-voltage lock-out circuit to keep the output off until the internal circuitry is operating properly. The UVLO function initiates a soft-start process after input voltage exceeds its rising UVLO threshold during power on. Typical UVLO threshold is 2.9V with 0.15V hysteresis.

### Soft-Start

The APL5607/A provides two internal soft-start circuitries to control rise rate of the output voltage and limit the current surge during start-up. Approximate 20 $\mu$ s delay time after the  $V_{IN}$  is over the UVLO threshold, the IC starts a soft-start. The typical soft-start interval is about 130 $\mu$ s.

### Enable/Shutdown

Driving the EN high turns on the regulator, driving the EN low puts the regulator into shutdown mode. A logic low also causes the output voltage to discharge to the GND. The EN pin is pulled low by an internal resistor in APL5607, while it is pulled high by an internal resistor in APL5607A.

### Current Limit

The APL5607/A provides a current-limit circuitry, which monitors the output current and controls P-MOS's gate voltage to limit the output current at 700mA.

### Foldback Current Limit

When the output voltage drops below 0.6V (typical), which is caused by the over load or the short circuit, the foldback current-limit circuitry limits the output current to 250mA. The foldback current limit is used to reduce the power dissipation during short circuit condition. The foldback current limits is disabled for 0.8ms (typical) after UVLO threshold is reached, therefore, the IC has normal 700mA (typical) current limit level during start-up.

### Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APL5607/A. When the junction temperature exceeds +150°C, the thermal shutdown circuitry disables the output, allowing the device to cool down. The output circuitry is enabled again after the junction temperature cools down by 40°C, resulting in a pulsed output during continuous thermal overload conditions.

## Application Information

### Input Capacitor

The APL5607/A requires proper input capacitors to supply surge current during stepping load transients to prevent the input rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN limits the slew rate of the surge current, place the Input capacitors near VIN as close as possible. Input capacitors should be larger than 2.2μF.

### Output Capacitor

The APL5607/A needs a proper output capacitor to maintain circuit stability and to improve transient response over temperature and current. In order to insure the circuit stability, the proper output capacitor value should be larger than 1μF. With X5R and X7R dielectrics, 2.2μF is sufficient at all operating temperatures. Maximum output capacitor should be less than 330μF to insure the system can be powered on effectively.

### Operation Region and Power Dissipation

The APL5607/A maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The power dissipation  $P_D$  across the device is:

$$P_D = \frac{(T_J - T_A)}{\theta_{JA}}$$

where  $(T_J - T_A)$  is the temperature difference between the junction and ambient air.  $\theta_{JA}$  is the thermal resistance between junction and ambient air. Assuming the  $T_A = 25^\circ\text{C}$  and maximum  $T_J = 150^\circ\text{C}$  (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$P_{D(max)} = (150 - 25) / 80 = 1.56(W)$$

For normal operation, do not exceed the maximum junction temperature rating of  $T_J = 125^\circ\text{C}$ . The calculated power dissipation should less than:

$$P_D = (125 - 25) / 80 = 1.25(W)$$

The GND provides an electrical connection to the ground and channels heat away. Connect the GND to the ground by using a large pad or ground plane.

### PCB Layout Consideration

Figure 1 illustrates the layout. Below is a checklist for your layout:

1. Please place the input capacitors close to the VIN .
2. Ceramic capacitors for load must be placed near the load as close as possible.
3. To place APL5607/A and output capacitors near the load is good for performance.
4. Large current paths, the bold lines in figure 1, must have wide tracks. 40mil layout trace is recommended.

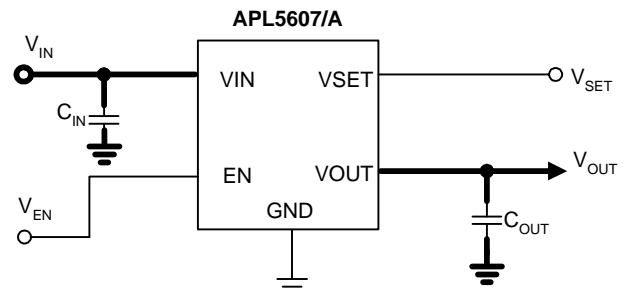


Figure 1

Optimum performance can only be achieved when the device is mounted on a PC board according to the SOP-8 Board Layout diagram.

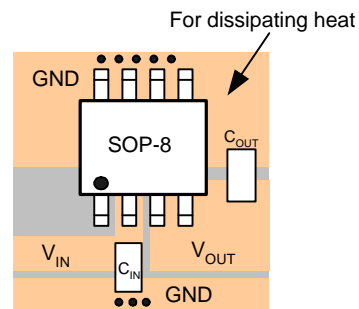
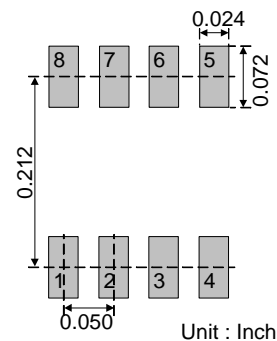


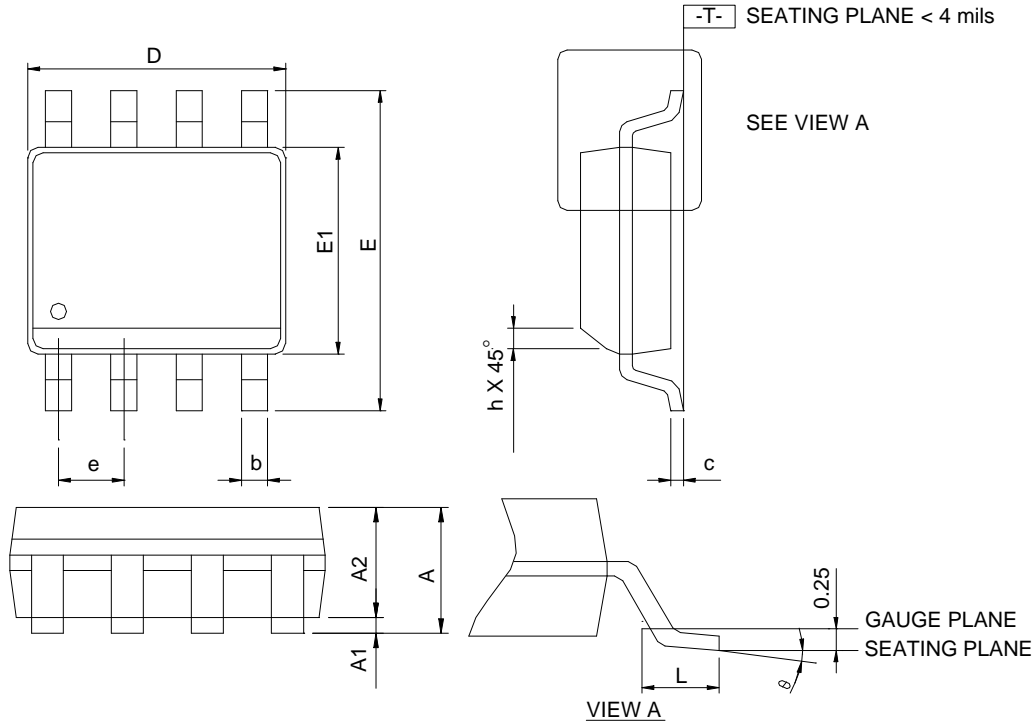
Figure 2

### Recommended Minimum Footprint



Package Information

SOP-8

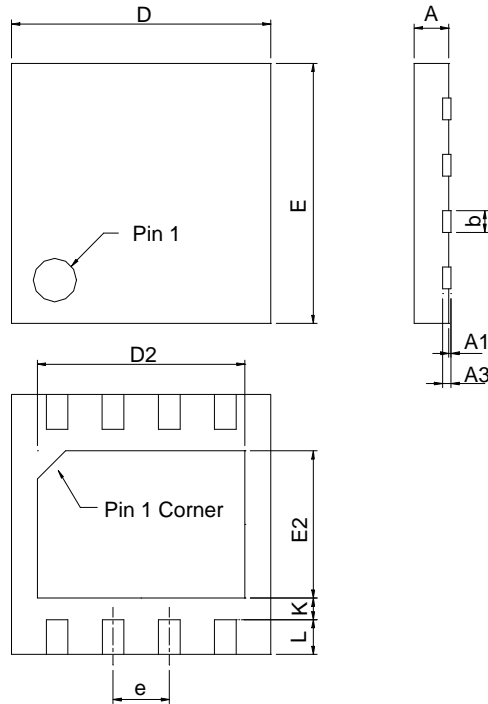


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

- Note: 1. Follow JEDEC MS-012 AA.  
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.  
 3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

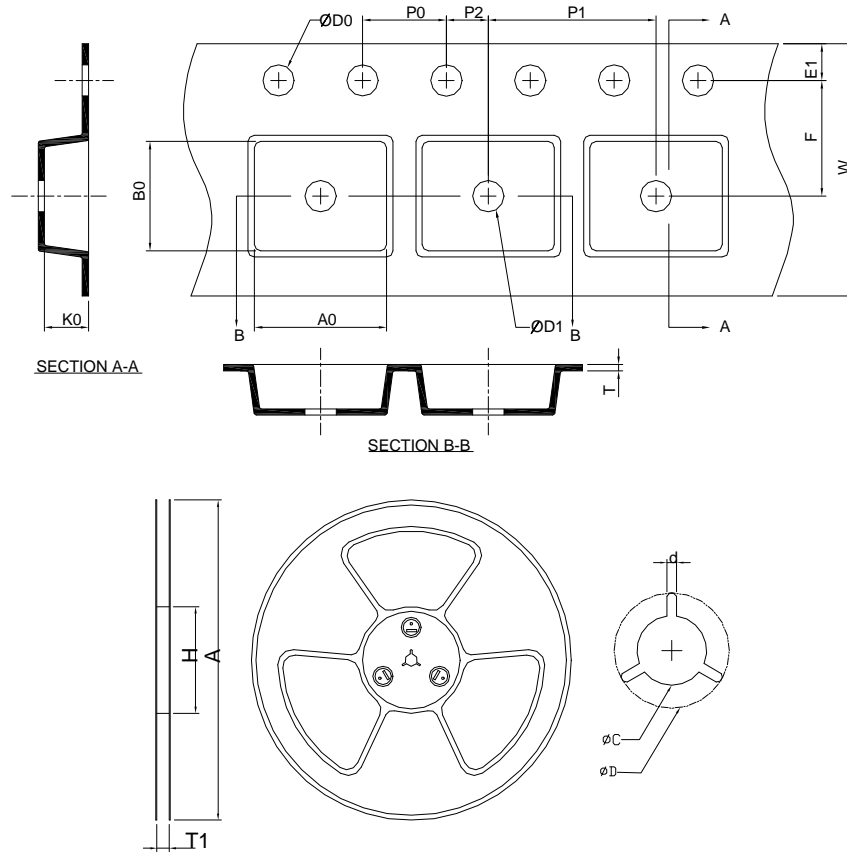
Package Information

TDFN3x3-8



SYMBOL	TDFN3x3-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.25	0.35	0.010	0.014
D	2.90	3.10	0.114	0.122
D2	1.90	2.40	0.075	0.094
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.65 BSC		0.026 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

### Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0 ±0.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40 ±0.20	5.20 ±0.20	2.10 ±0.20
Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-8	330.0 ±0.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30 ±0.20	3.30 ±0.20	1.30 ±0.20

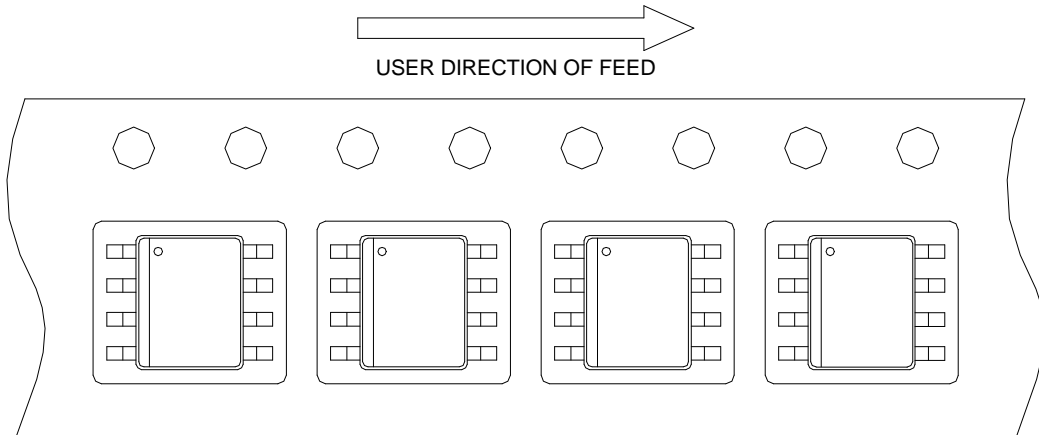
(mm)

### Devices Per Unit

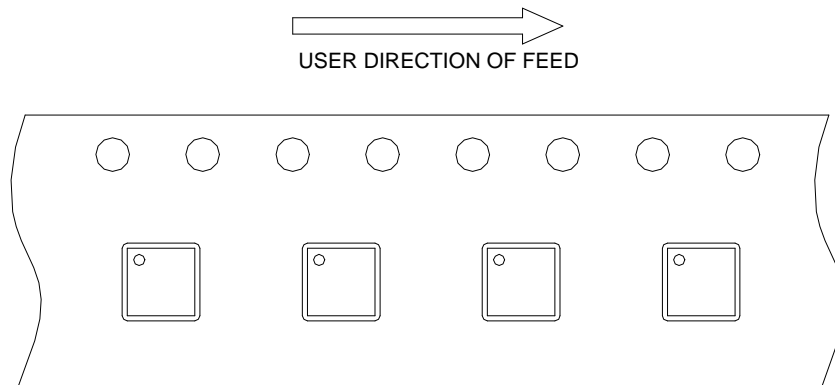
Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500
TDFN3x3-8	Tape & Reel	3000

### Taping Direction Information

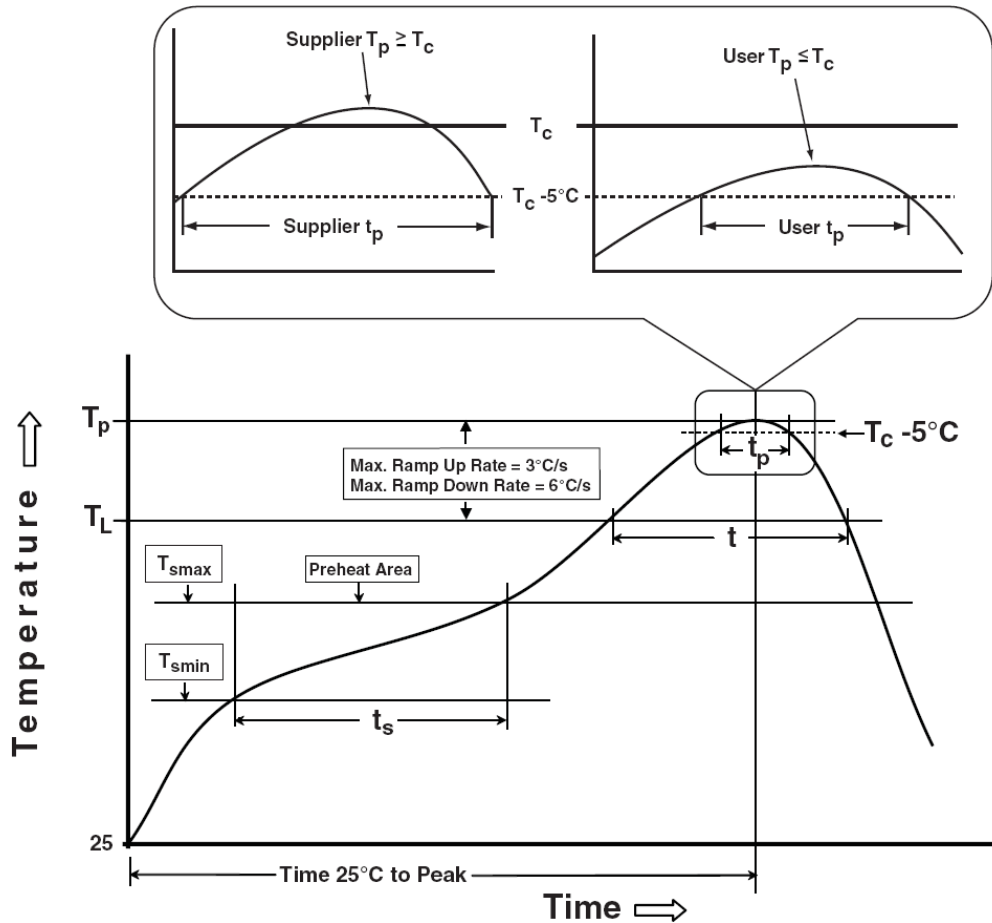
SOP-8



TDFN3x3-8



**Classification Profile**



**Classification Reflow Profiles**

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
<b>Preheat &amp; Soak</b>		
Temperature min ( $T_{smin}$ )	100 °C	150 °C
Temperature max ( $T_{smax}$ )	150 °C	200 °C
Time ( $T_{smin}$ to $T_{smax}$ ) ( $t_s$ )	60-120 seconds	60-120 seconds
Average ramp-up rate ( $T_{smax}$ to $T_p$ )	3 °C/second max.	3°C/second max.
Liquidous temperature ( $T_L$ )	183 °C	217 °C
Time at liquidous ( $t_L$ )	60-150 seconds	60-150 seconds
Peak package body Temperature ( $T_p$ )*	See Classification Temp in table 1	See Classification Temp in table 2
Time ( $t_p$ )** within 5°C of the specified classification temperature ( $T_c$ )	20** seconds	30** seconds
Average ramp-down rate ( $T_p$ to $T_{smax}$ )	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature ( $t_p$ ) is defined as a supplier minimum and a user maximum.		

**Classification Reflow Profiles (Cont.)**

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

**Reliability Test Program**

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T <sub>j</sub> =125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM 2KV
MM	JESD-22, A115	VMM 200V
Latch-Up	JESD 78	10ms, 1 <sub>tr</sub> 100mA

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